KU LEUVEN

Principles and Limits of Nyquist ADCs

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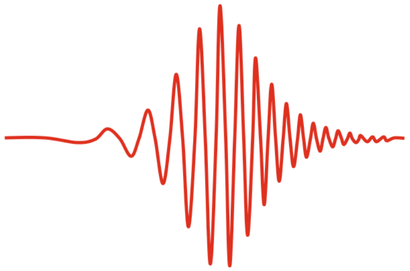
Outline

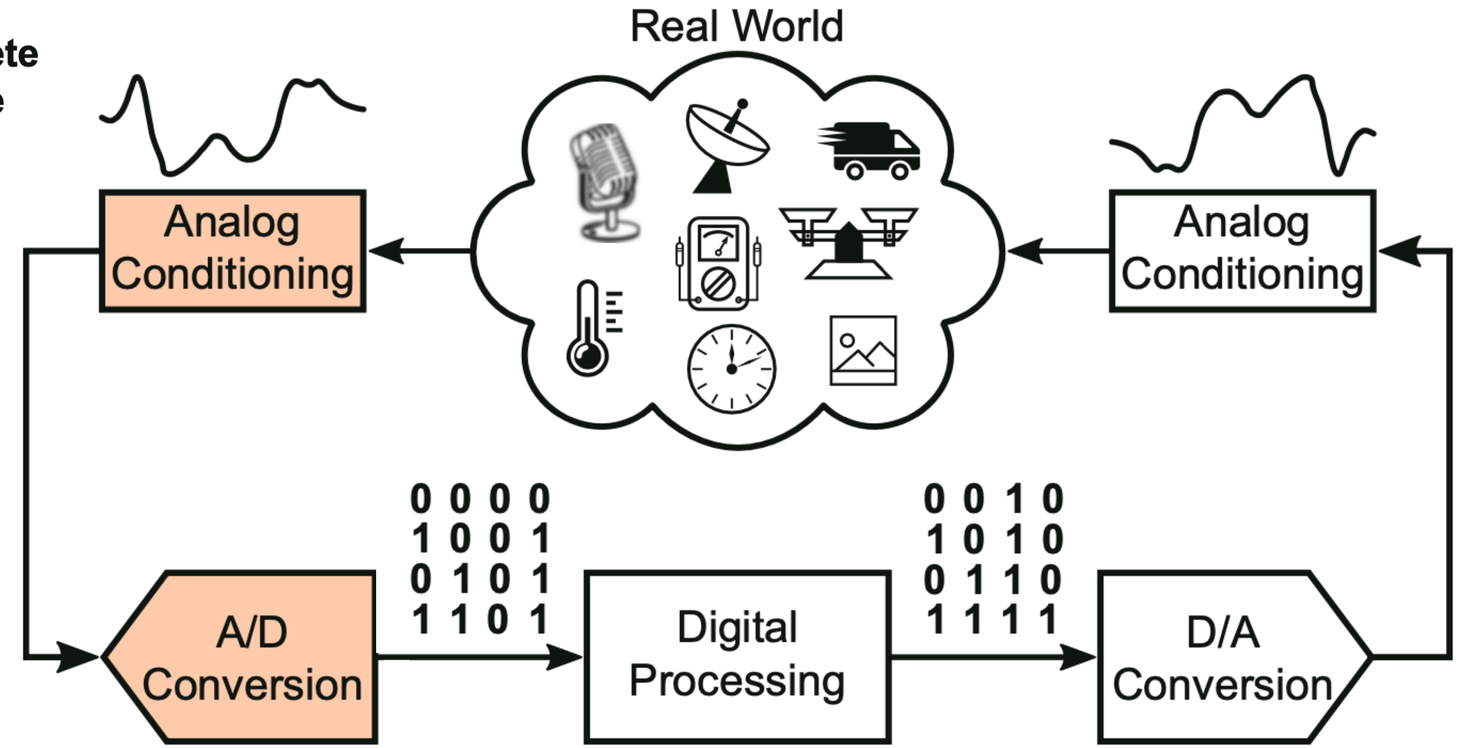
- **Introduction**
- Principles of Nyquist ADCs
- Limits of Nyquist ADCs
- Conclusion

Data conversion in a digital world

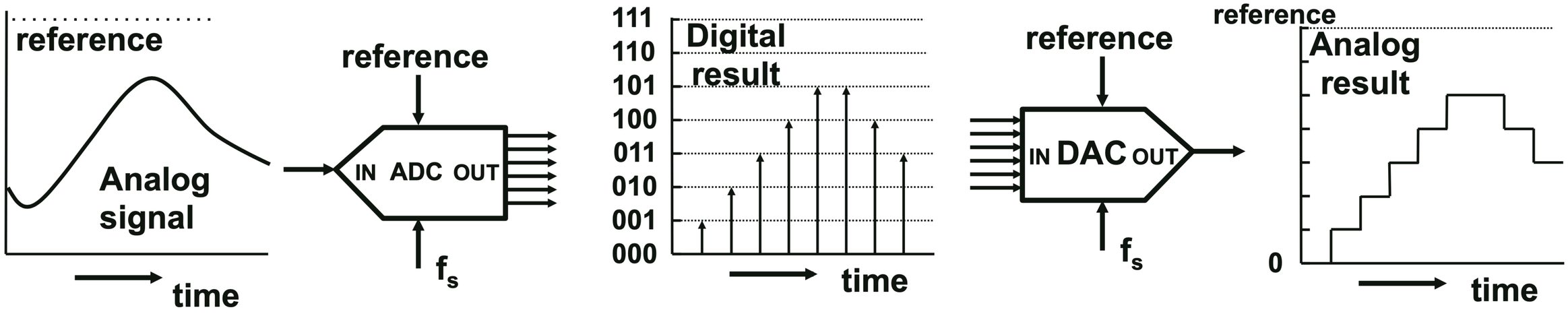


Time continuous
Amplitude continuous
Physical quantity

Time discrete
Amplitude discrete
Numerical value



Analog-to-digital-to-analog conversion



Analog-to-digital conversion:

1. Time discretization = sampling
2. Amplitude discretization = quantization

Digital-to-analog conversion:

1. Amplitude restoration
2. Holding the signal

Digital result = number describing fraction of **reference**

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  - Analog-to-digital conversion
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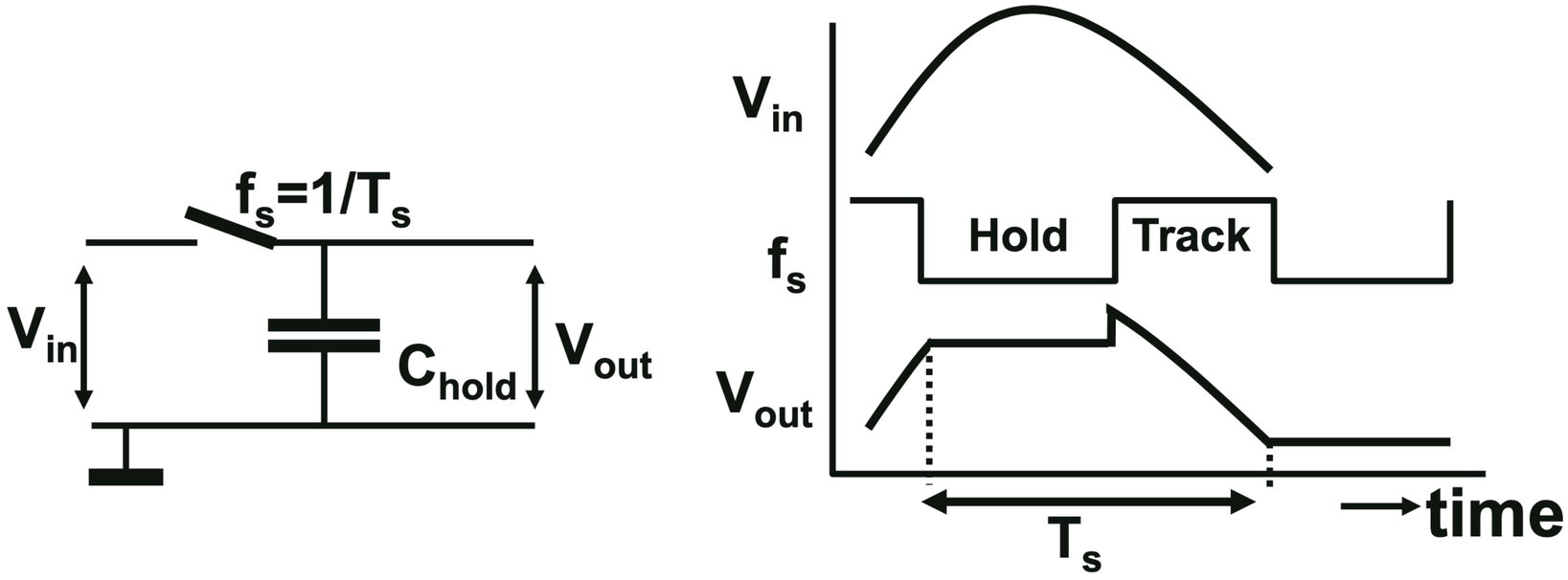
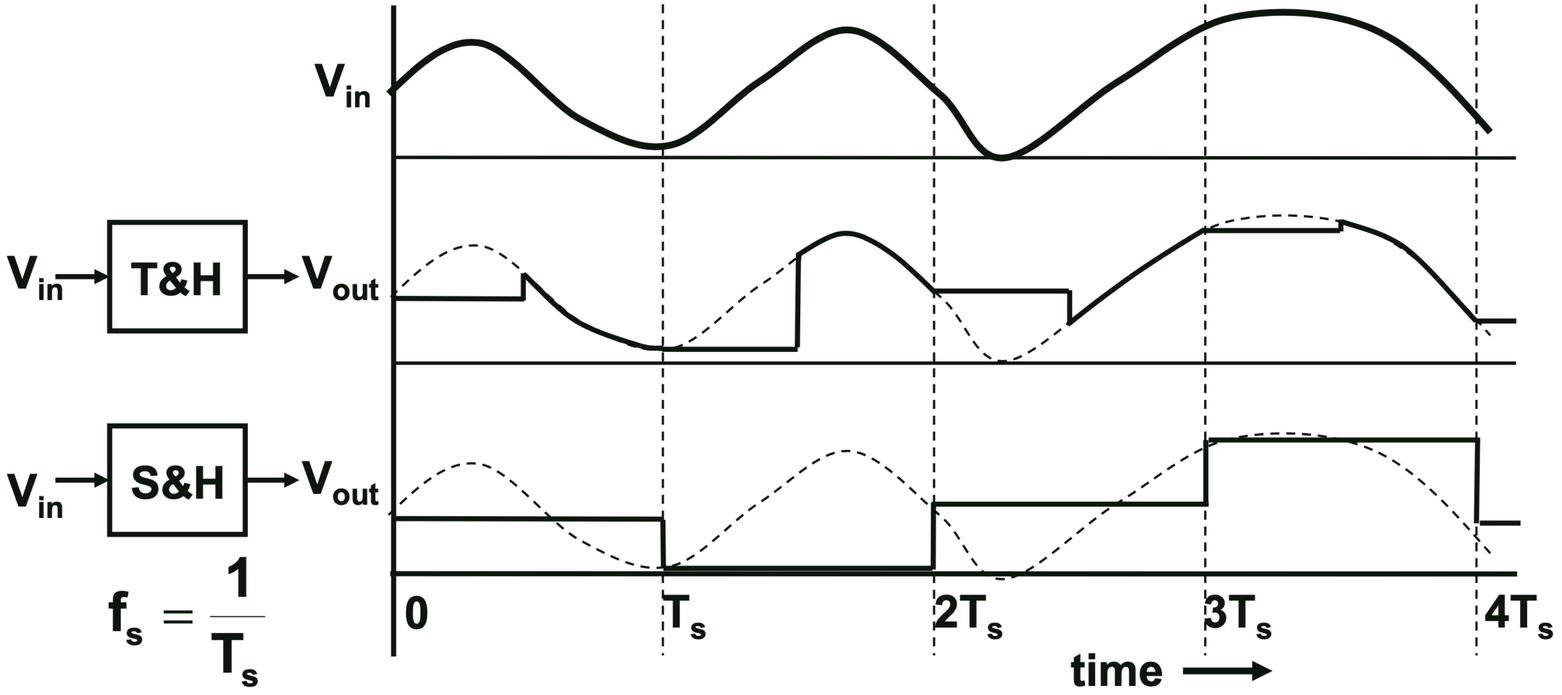
Basic operation principle



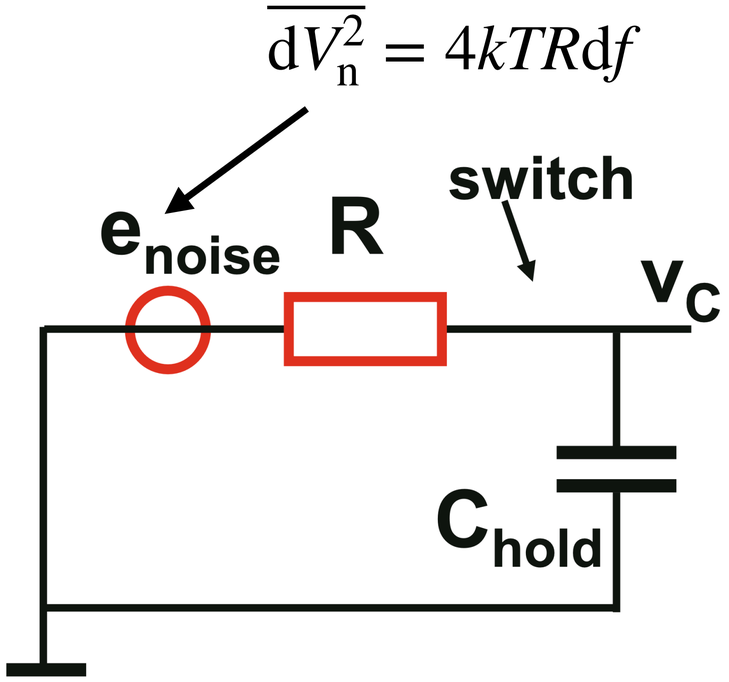
- Switch and capacitor form the most basic track-and-hold circuit (T&H)
- Sampling moment is at end of track phase/beginning of hold phase
- Many passive and active T&H implementations exist

Track-and-hold or sample-and-hold?



- S&H are two cascaded T&H circuits with inverted clocks
- S&H provides sampled signal for the full clock period
- Clock duty cycle doesn’t need to be 50%

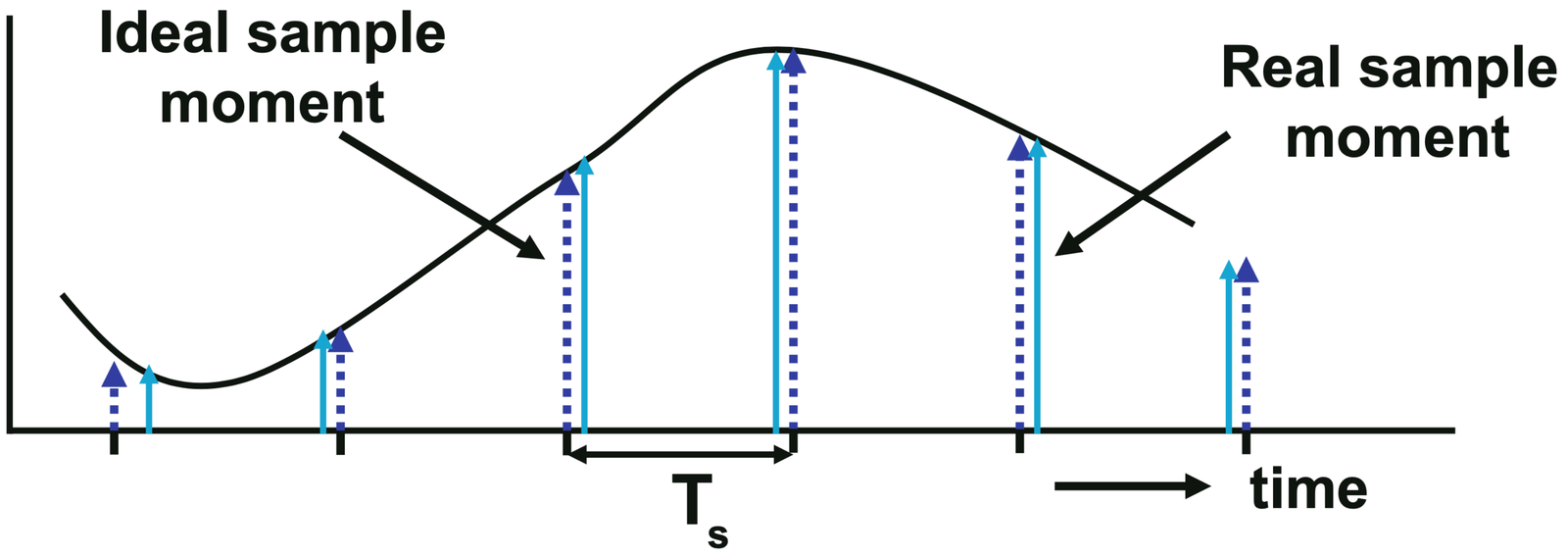
Sampling noise



C_{hold}	$V_{kTC} = \sqrt{kT/C_{hold}}$ at $T = 300\,°C$
10 fF	650 μV_{rms}
100 fF	204 μV_{rms}
1 pF	65 μV_{rms}
3 pF	35 μV_{rms}
10 pF	20.4 μV_{rms}
30 pF	11.8 μV_{rms}

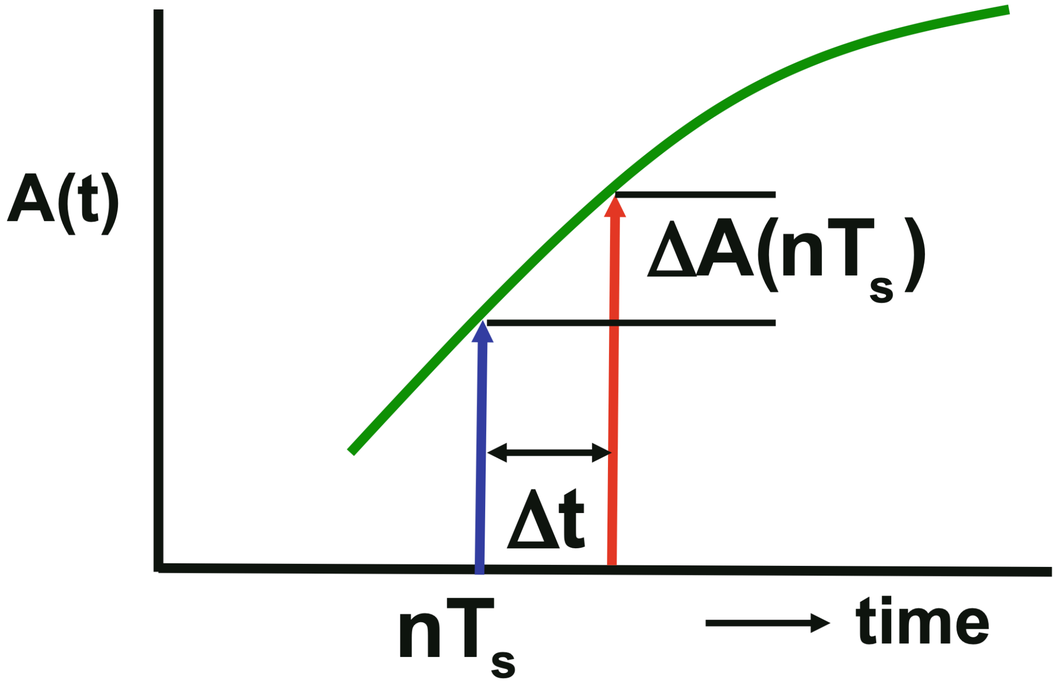
$$v_{C,noise}^2 = \int_{f=0}^{f=\infty} \frac{4kTR\,df}{1+(2\pi f)^2R^2C^2} = \frac{kT}{C} \quad \Rightarrow v_{C,noise} = \sqrt{\frac{kT}{C}} \rightarrow \mathrm{SNR} = \frac{P_{signal}}{P_{noise}} = \frac{\hat{A}^2/2}{kT/C}$$

Jitter of the sampling pulse



- Sampling pulse is derived from a noisy clock generator
- Noise in the time domain is random jitter resulting in error on the sampled signal
- Jitter can also be deterministic resulting in tones in the spectrum or distortion for signal-dependent jitter

Jitter noise



For sinusoidal input $A(t) = \hat{A}\sin(\omega t)$

$$A(nT_s + \Delta t(t)) = \hat{A}\sin(\omega \times (nT_s + \Delta t(t))$$

$$\Delta A(nT_s) = \frac{d\hat{A}\sin(\omega t)}{dt} \times \Delta t(nT_s) = \omega\hat{A}\cos(\omega nT_s)\Delta t(nT_s)$$

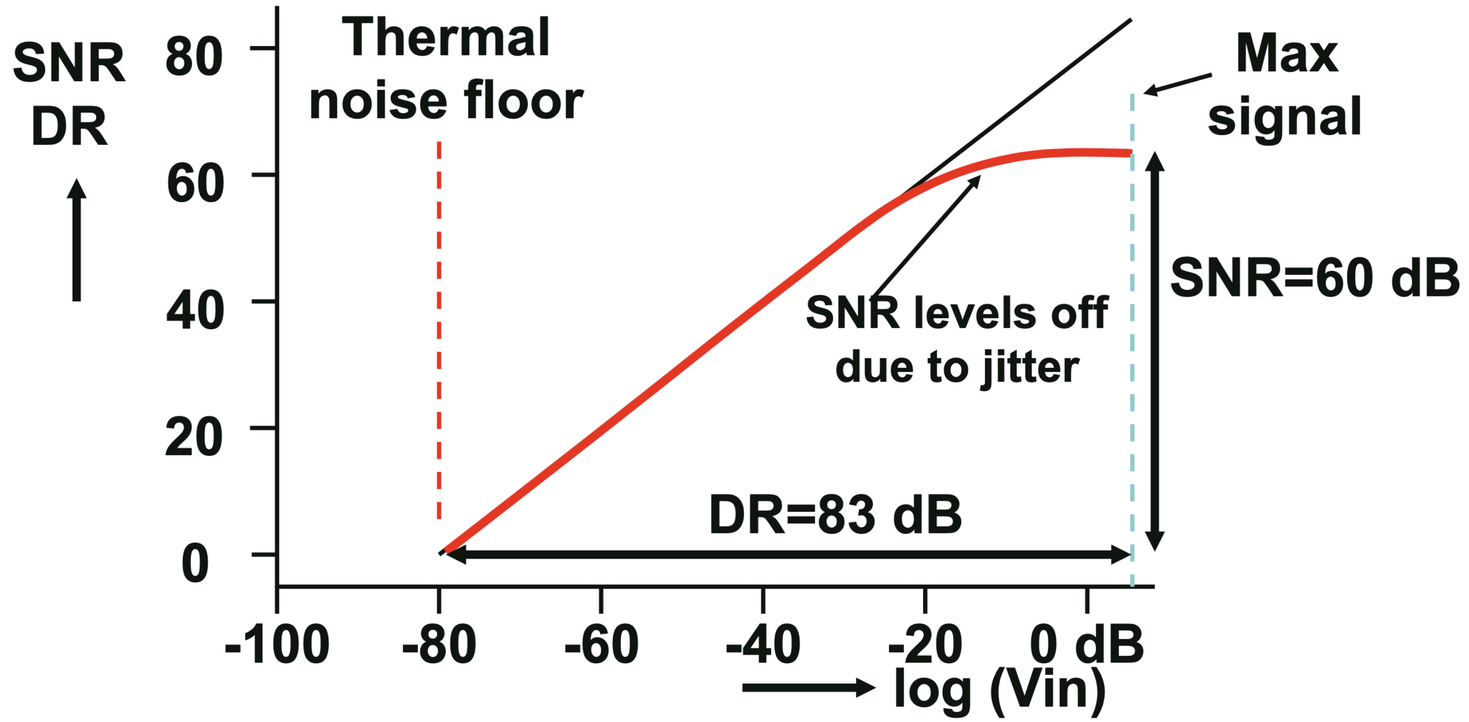
$$\sigma_A^2(nT_s) = \left(\frac{dA(nT_s)}{dt}\right)^2 \sigma_t^2 = \omega^2\hat{A}^2\cos^2(\omega nT_s)\sigma_t^2$$

jitter variance

averaged

$$\boxed{\sigma_A^2 = \frac{\omega^2\hat{A}^2\sigma_t^2}{2}}$$ = white if σ_t is white

SNR limitation due to jitter

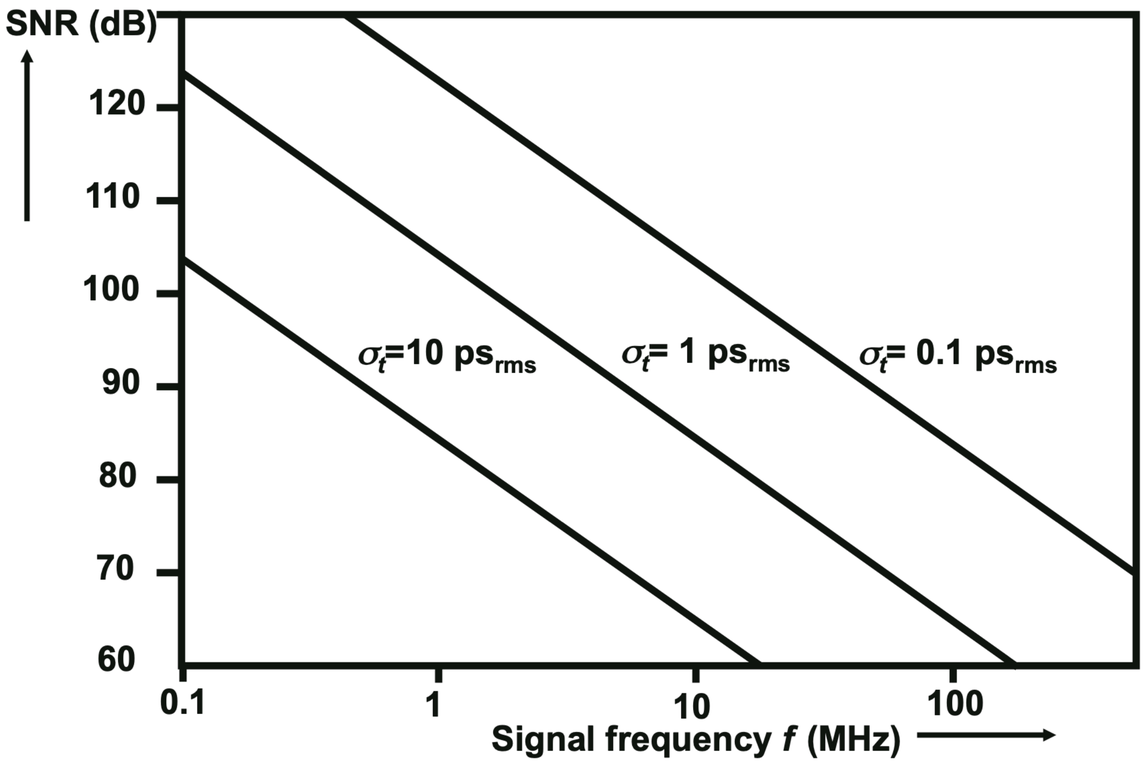


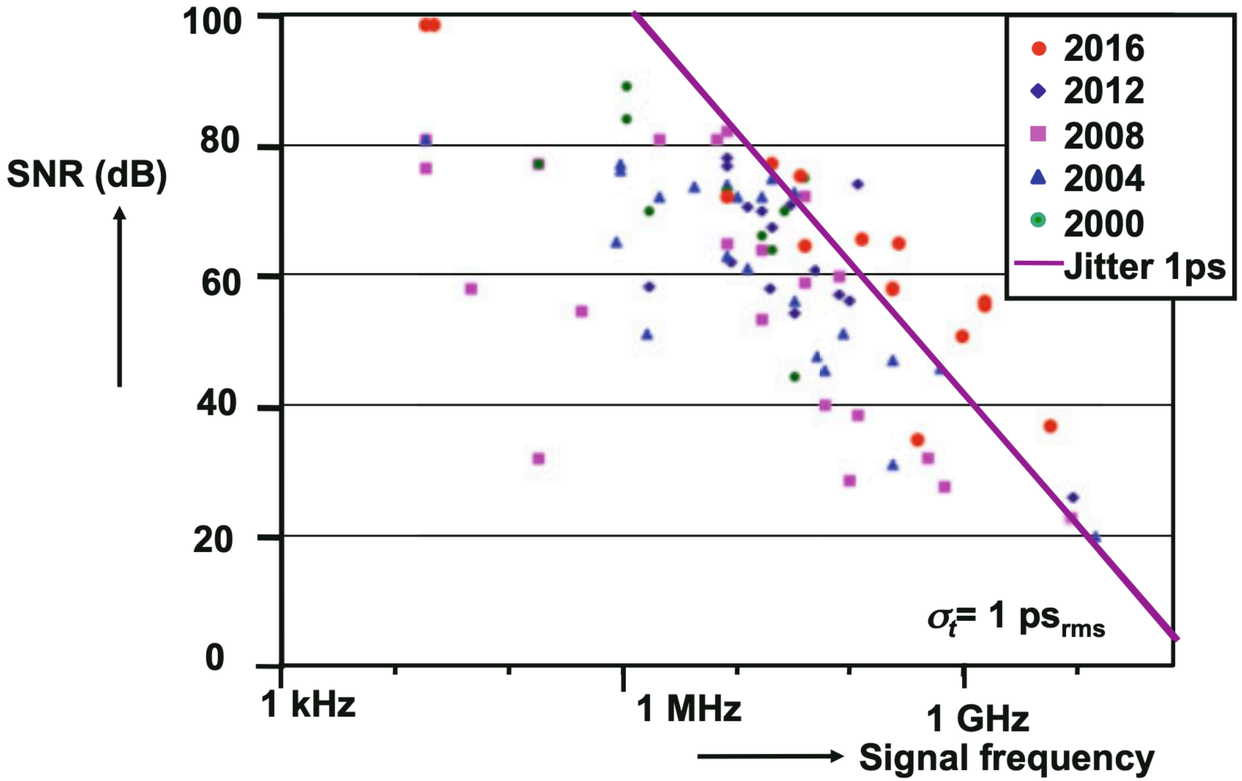
$$\mathrm{SNR} = \frac{\mathrm{P_{signal}}}{\mathrm{P_{jitter}}} = \frac{\widehat{A}^2/2}{\sigma_A^2} = \left(\frac{1}{\omega\sigma_t}\right)^2 = \left(\frac{1}{2\pi f\sigma_t}\right)^2$$

$$\mathrm{SNR} = 20\,{}^{10}\log\left(\frac{1}{\omega\sigma_t}\right) = 20\,{}^{10}\log\left(\frac{1}{2\pi f\sigma_t}\right)$$

- depends on signal frequency
- depends NOT on signal amplitude!
- depends NOT on sample rate
  → jitter power density ~ $1/f_s$

Jitter SNR versus frequency





data from 'ADC Performance Survey' by B. Murmann
http://web. stanford.edu/~murmann/adcsurvey.html

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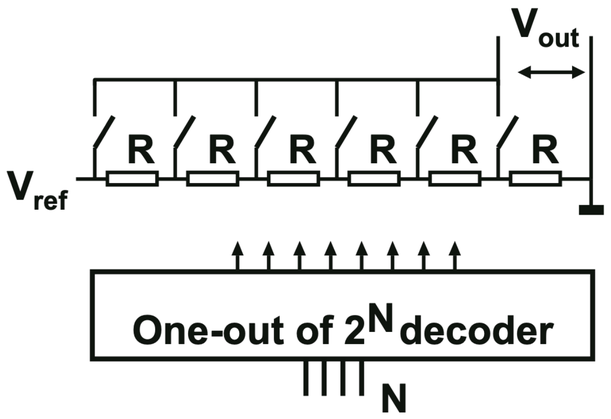
The need for DACs

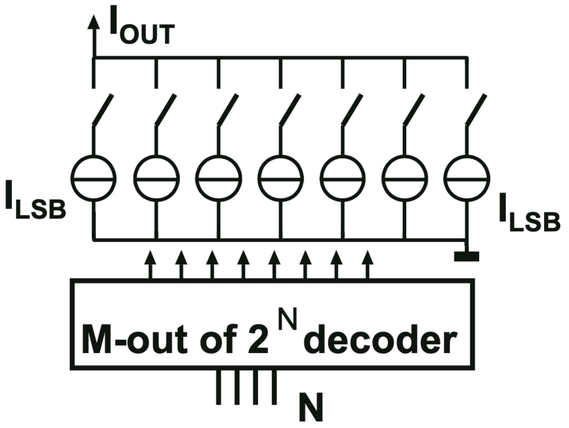
Digital-to-analog converters are required in two types of applications:

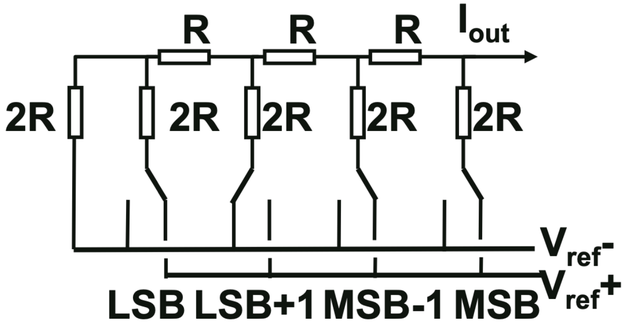
1. To convert a signal to the physical domain
   - High quality signal at every time instant
   - Some power must be delivered to a load impedance
2. To generate an analog reference value, ex. in an ADC
   - Signal only required at specific time instants
   - Very limited drive capabilities

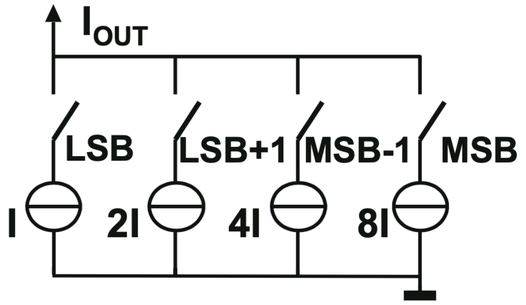
Possible DAC architectures

	Unary	Binary
Voltage	Resistor string *Flash ADC*	R-2R *Low-performance DAC*
Current	Current matrix *High bandwidth DAC*	Current splitting
Charge/capacitor	Capacitor bank *Low power DAC*	Capacitor bank
Time	PWM, ΣΔ mod *Low bandwidth DAC*	Limited by distortion

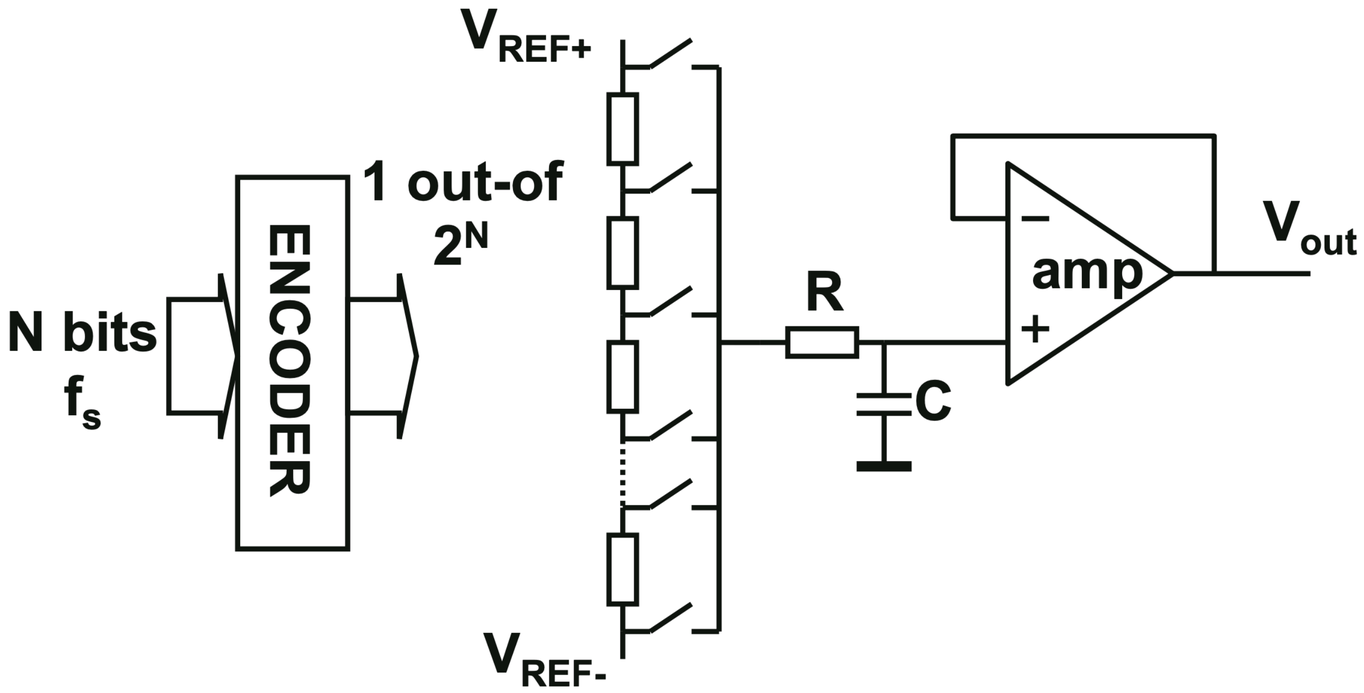






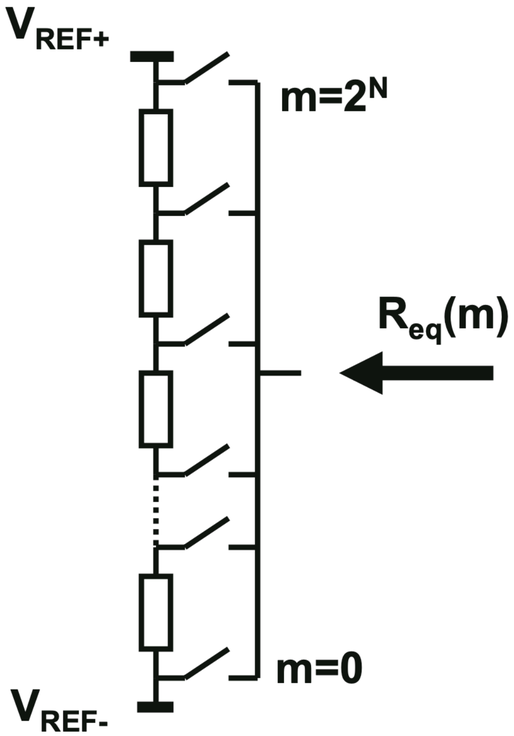


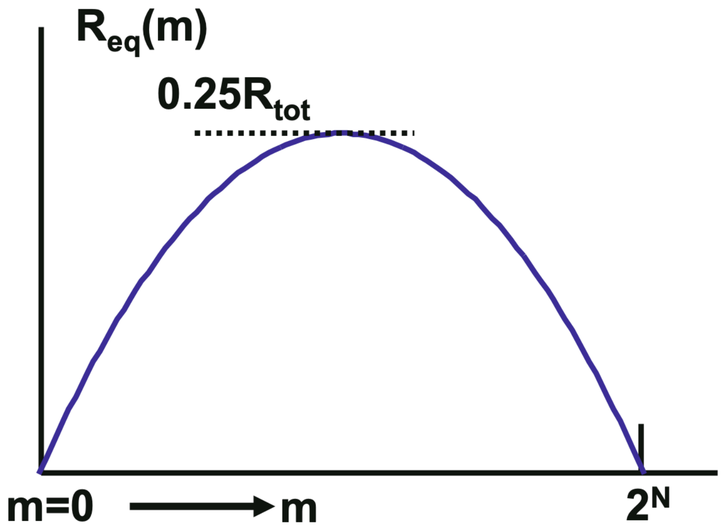
Resistor ladder



- Unary structure
- 2^N resistors between V_{REF+} and V_{REF-}
- Selection and switching network
- Buffer to drive a load
- Also used to generate quantization levels in flash ADCs

Resistor ladder impedance

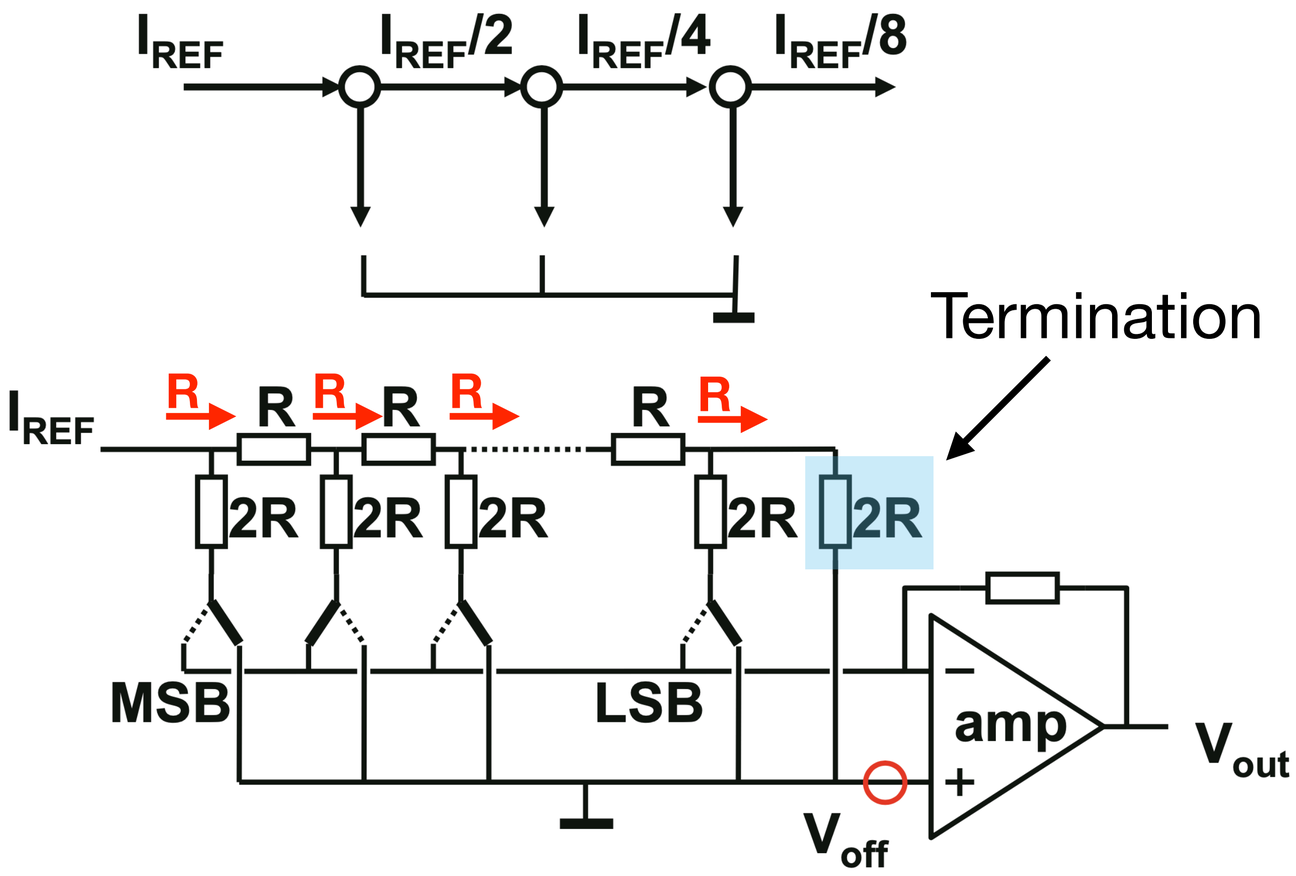




$$R_{eq}(m) = \frac{\frac{m}{2^N}R_{tot} \times \frac{2^N - m}{2^N}R_{tot}}{\frac{m}{2^N}R_{tot} + \frac{2^N - m}{2^N}R_{tot}} = \frac{m(2^N - m)}{2^{N+1}}R_{tot}$$

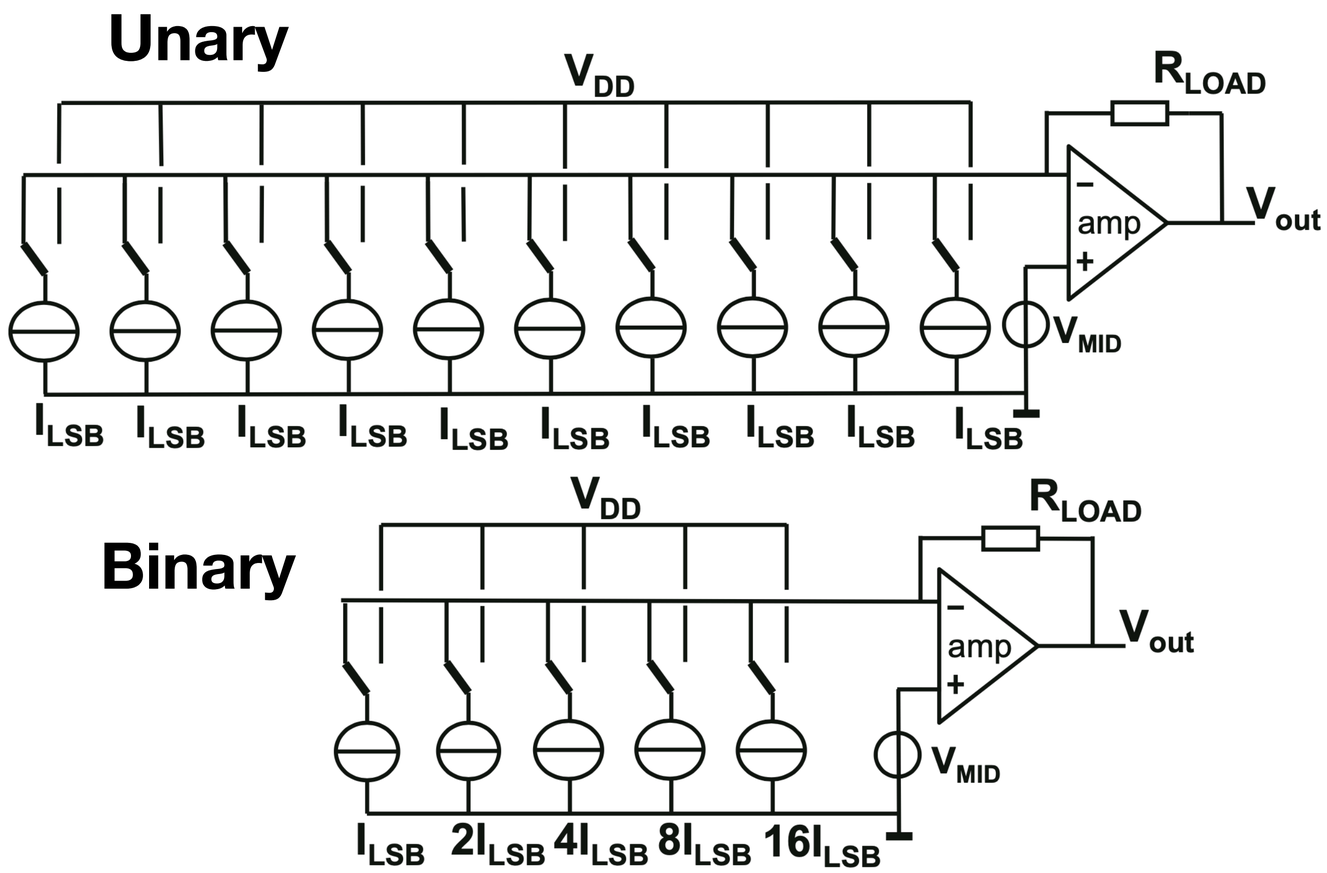
- Parabolic variation of impedance
- Signal-dependent current delivery
- Signal-dependent time constant for fixed capacitive load
- Distortion at high frequencies

R-2R ladders



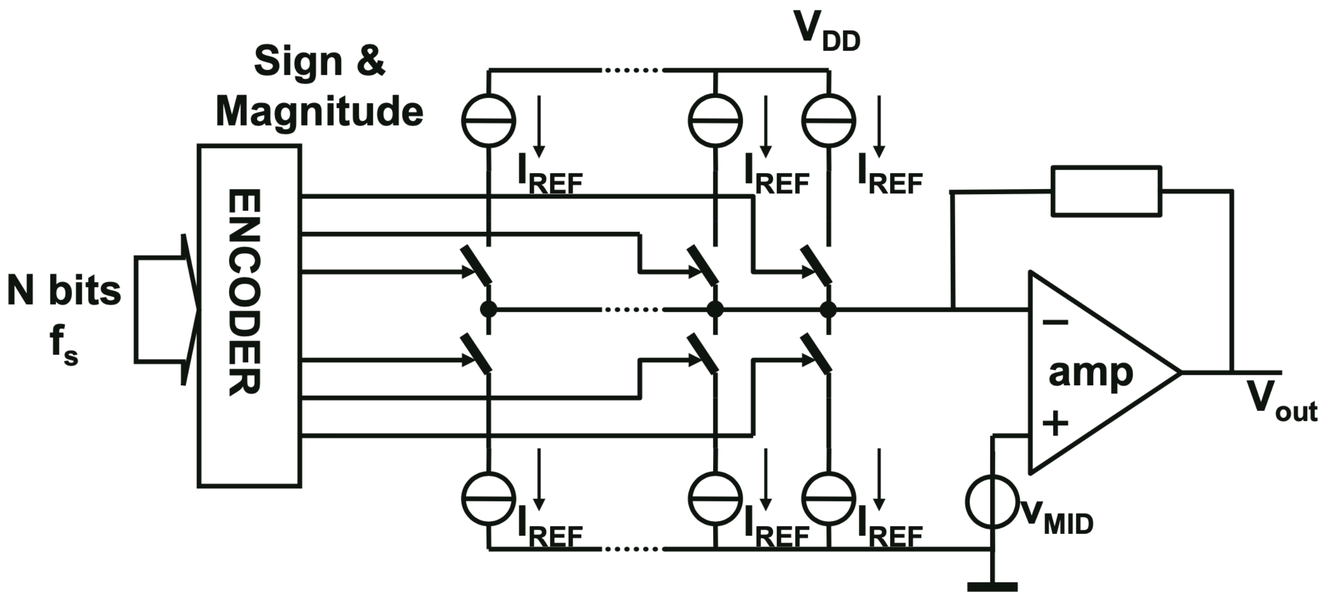
- Binary structure
- 2N resistors to create binary weighted currents
- Resistance ‘looking right’ always R
- No decoder required
- Currents added in feedback resistor
- OK for low resolution, low cost applications

Buffered current DAC



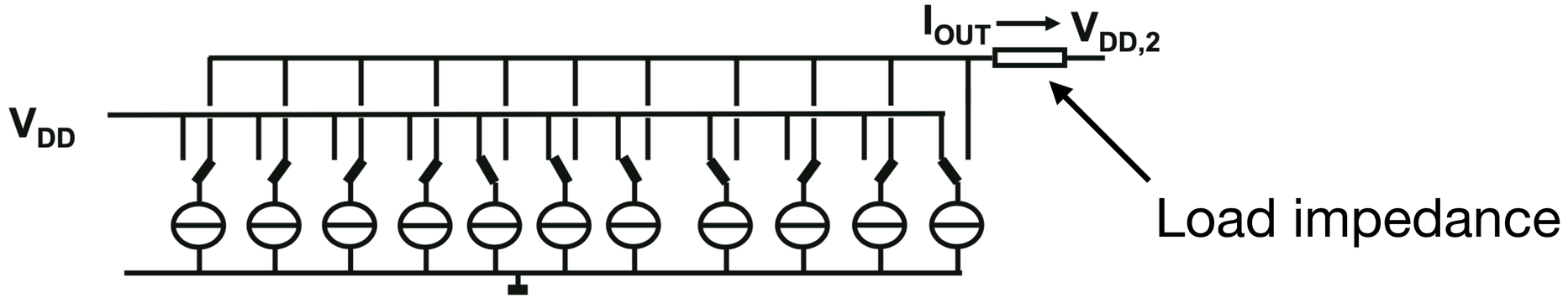
- Sequential acces in unary structure, but decoder required
- Large switching transients in binary structure, but no decoder required
- Current source matching determines accuracy
- Unused current sources should not be switched off → current dump
- Current sensed by transimpedance amplifier (TIA):
  → low input impedance to limit swing
  → low output impedance to drive load

Symmetrical buffered current DAC



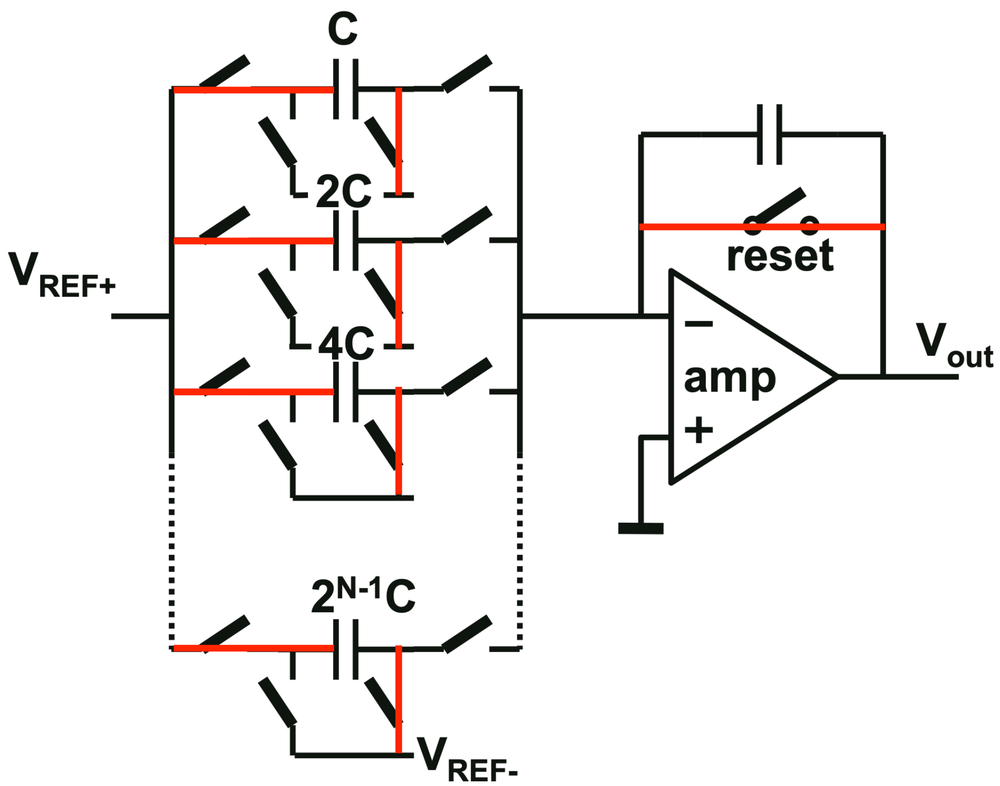
- Many signals are symmetrical around zero level
- Previous topology would require zero-signal at $V_{MID} + R_{LOAD}I_{total}/2$
  → 1/f and thermal noise pollution!
- Symmetrical signal requires current **sourcing** and current **sinking**
- Only noise of buffer for zero level
  → better SNR for low levels
- Inherent inequality between current sources (PMOS) and sinks (NMOS)
  → calibration

Buffer-less current-DAC



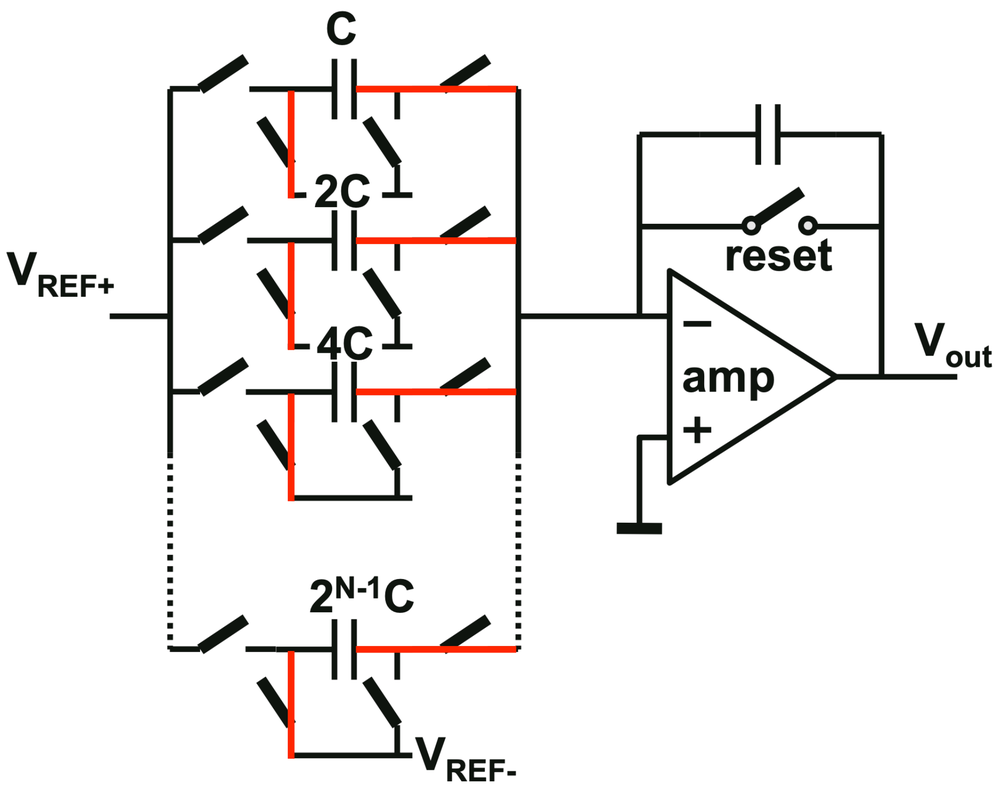
- No bandwidth-limiting buffer required, current flows directly through load
- Bandwidth limited by pole at the output node determined by:
  1. load impedance
  2. parasitic capacitance of current source array
- Well-suited for high-performance time-continuous signals in 50-75 Ω

Capacitive DAC



Reset phase:

- Capacitors recharged
- Opamp in unity feedback

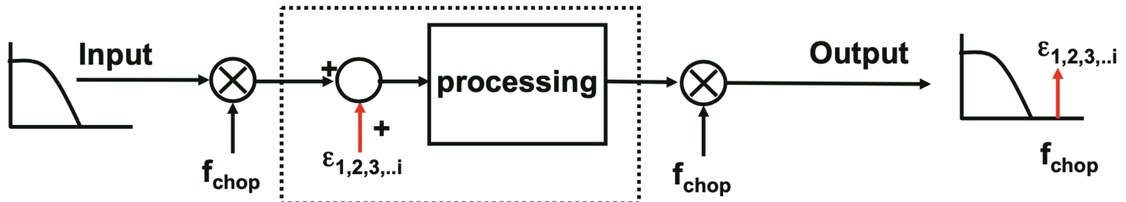


Signal phase:

- Capacitors discharged
- Opamp transfers charge of all capacitors to feedback capacitor

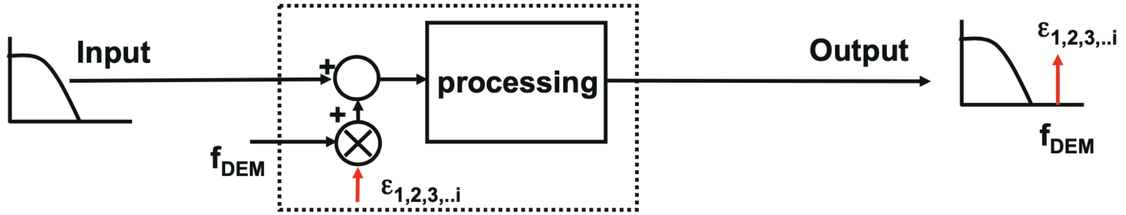
Techniques to mitigate additive errors

Chopping



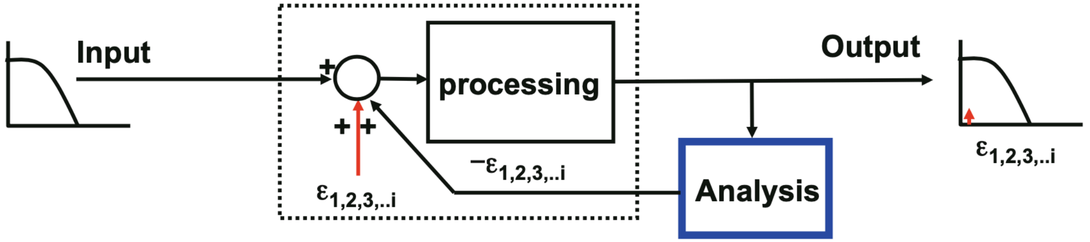
- Good mixers required
- Processing at high frequency
- Error energy still present

Dynamic element matching
Data-weighted averaging



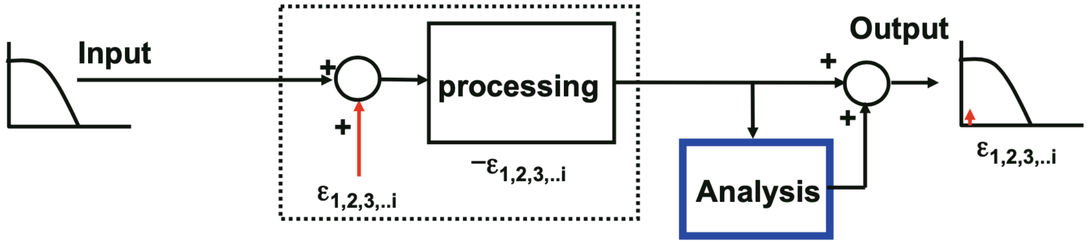
- No mixers required
- Processing at signal frequency
- Error energy still present

Feedback calibration



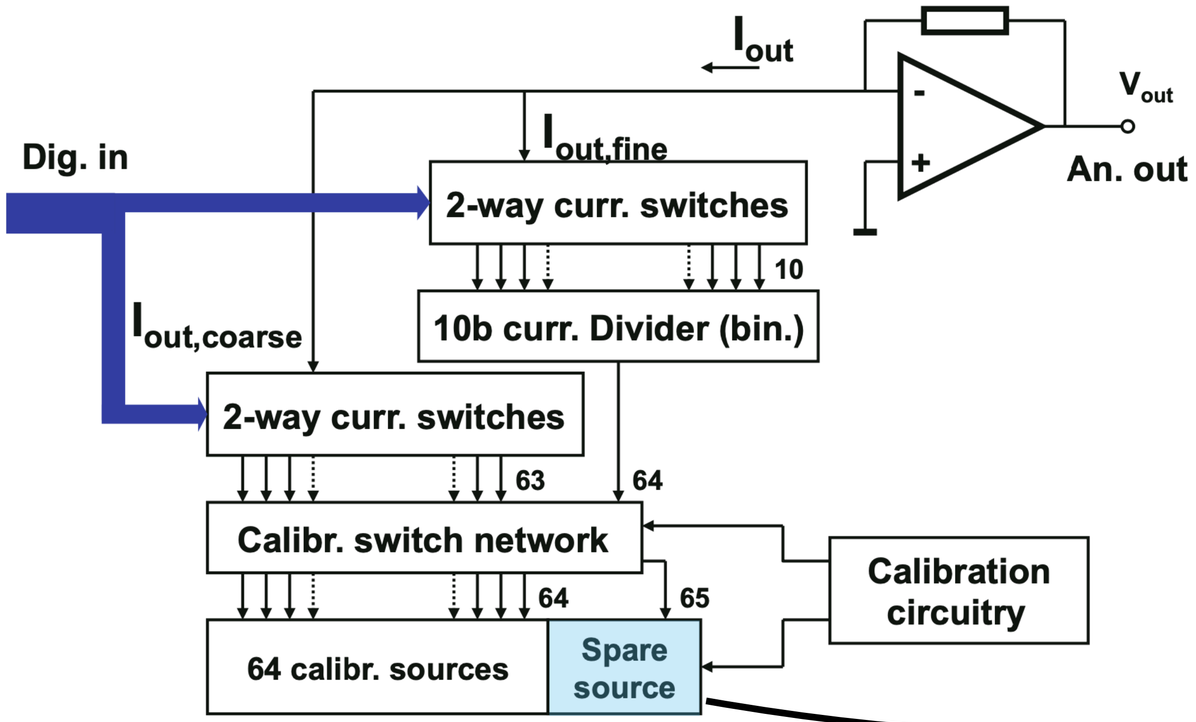
- Error energy removed
- Can be during production or with regular on-chip measurements

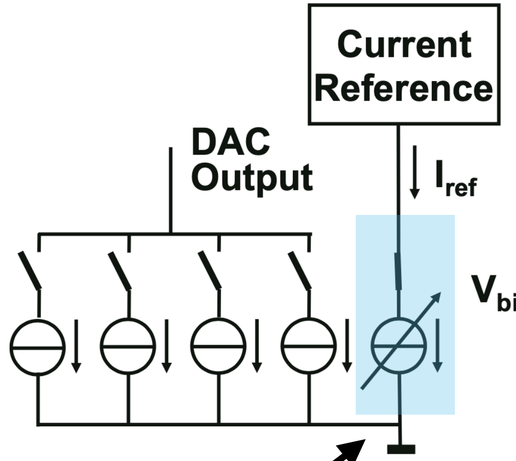
Feedforward calibration

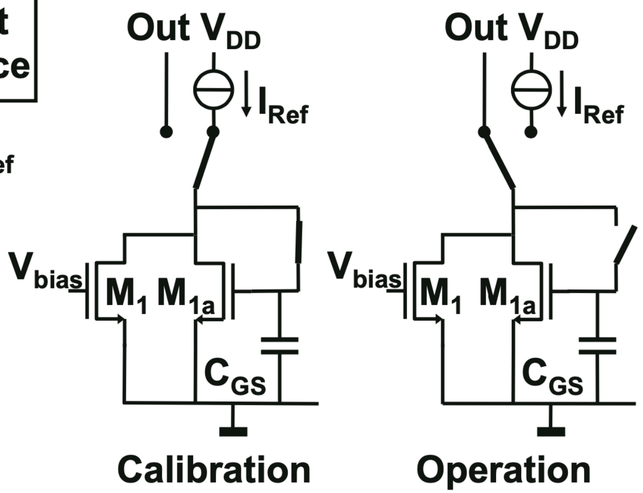


- Can be in the foreground (not during signal processing) or in the background (during signal processing)

Current calibration





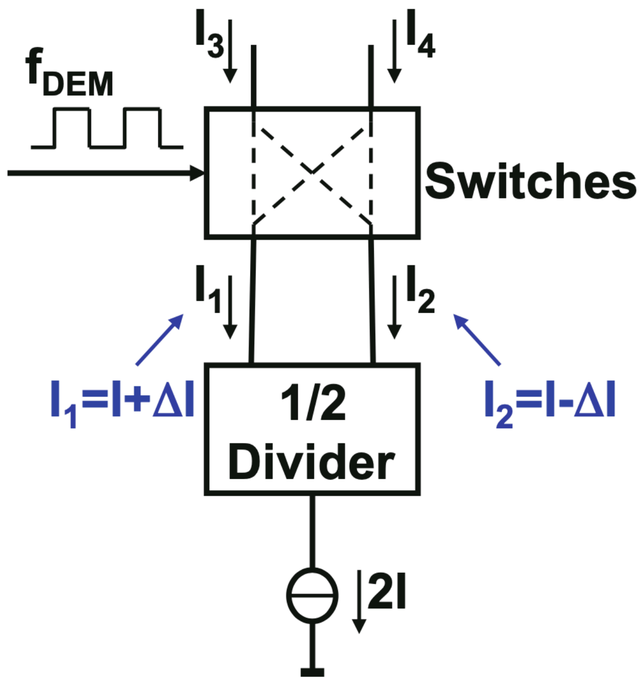


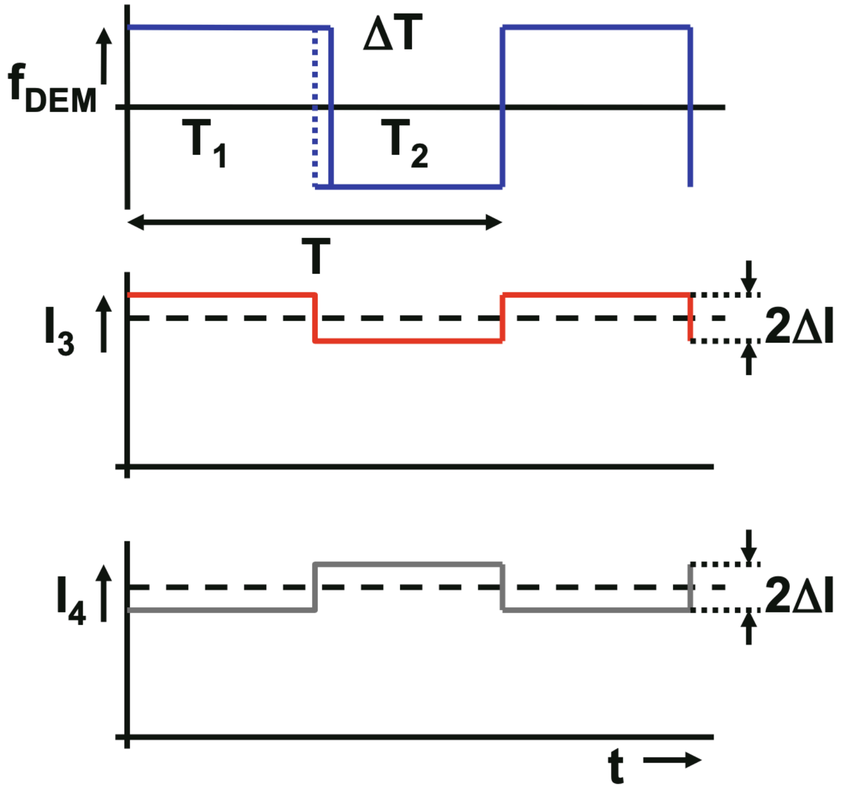
Groeneveld DWJ, Schouwenaars HJ, Termeer HAH, Bastiaansen CAA (1989) A self-calibration technique for monolithic high-resolution D/A converters. IEEE J Solid-State Circuits 24:1517–1522

- Extra cell to enable current source rotation
- DC error and low-frequency noise removed
- High-frequency noise during calibration influence current
  → M_1 conducts majority of current

Dynamic element matching

Idea: swap identically designed voltages or currents regularly





$$\frac{I_3 - I_4}{I_3 + I_4} = \frac{I_1 - I_2}{I_1 + I_2} \times \frac{t_1 - t_2}{t_1 + t_2}$$

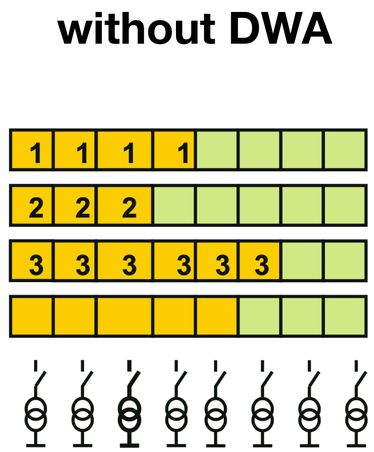
= 0 if $T_1 = T_2$

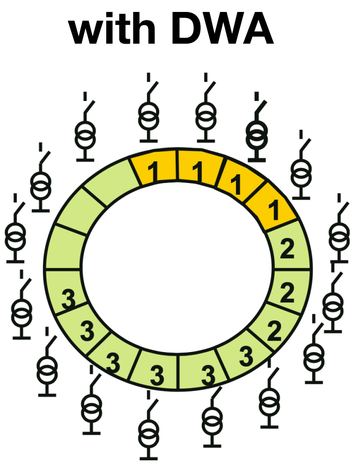
Data-weighted averaging

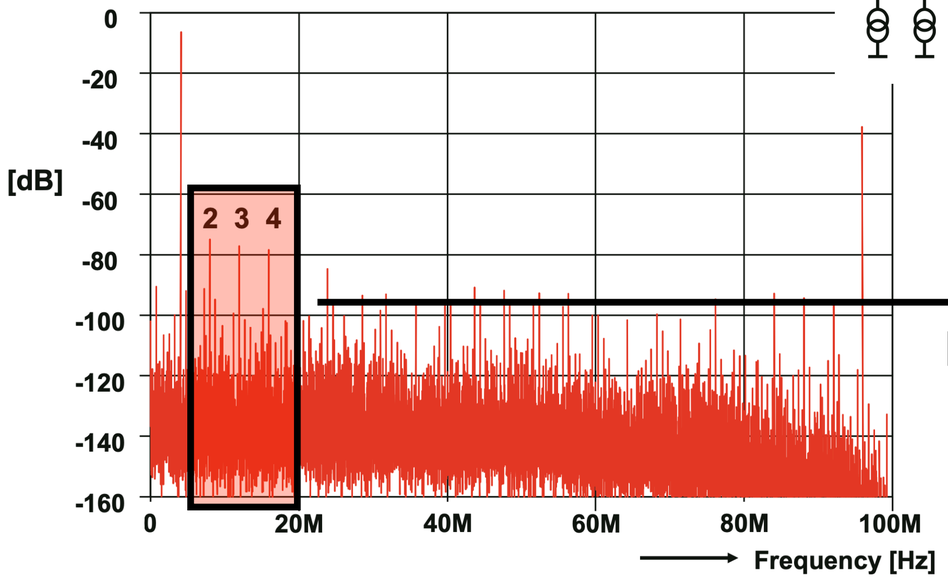
Idea: change the starting point of the array for every sample

DWA is a noise shaping technique

→ oversampling applications

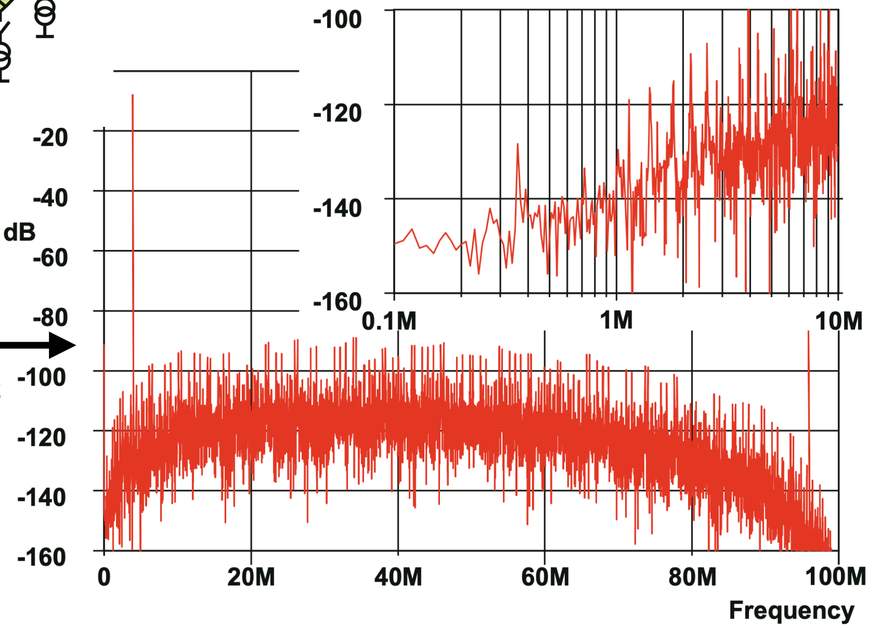






Much lower HD!

Much cleaner spectrum at DC



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  - **Analog-to-digital conversion**
- Limits of Nyquist ADCs
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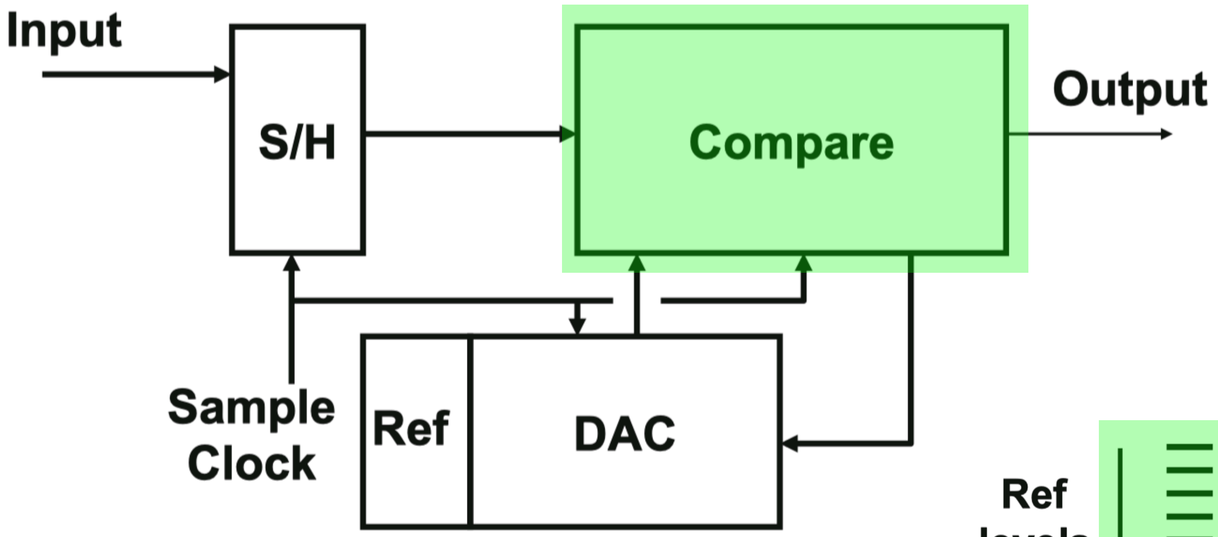
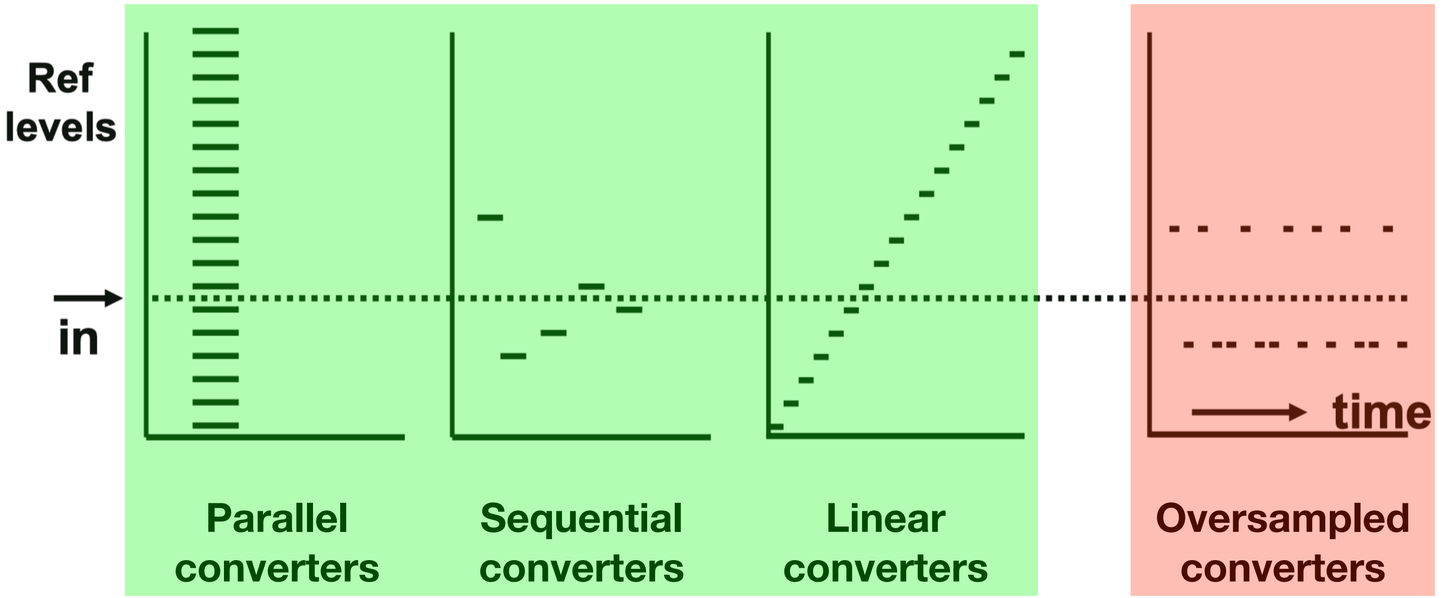
A generalized ADC architecture



Required functionality:

1. Sampling
2. Reference generation
3. Comparison
4. Search algorithm



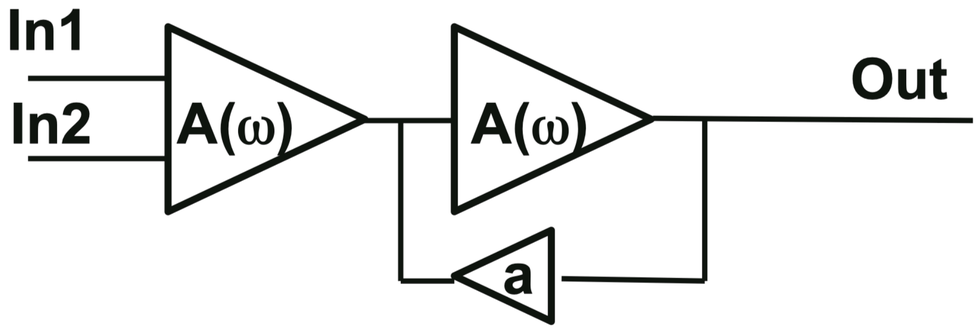
Comparator requirements

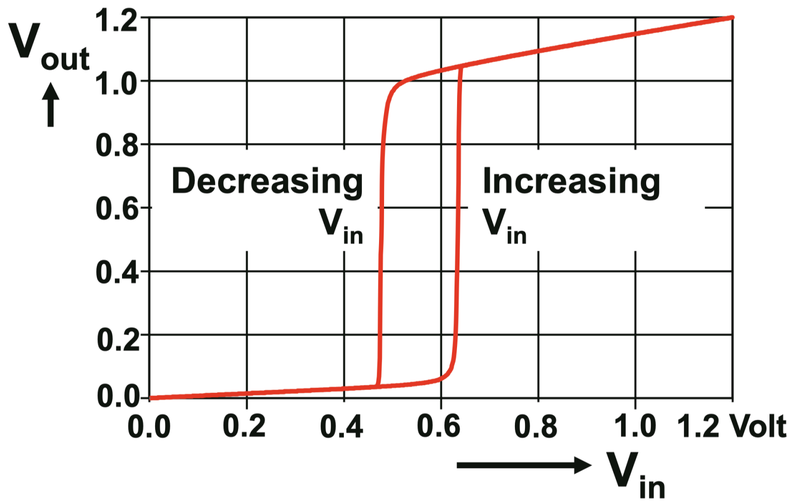
- Simple functionality: **‘Amplify (small) input signal into a digital level’**
- Many requirements:
  - Large amplification → from µV-mV to V
  - Large bandwidth → fast decisions, especially in sequential and linear converters
  - High accuracy → low offset and low noise to not add uncertainty
  - Low power → especially for parallel (flash) converters
  - Wide input range → to cover the complete input signal range
  - No memory effect → to make independent decisions
  - No metastability → to always have a decision

Extremely challenging building block

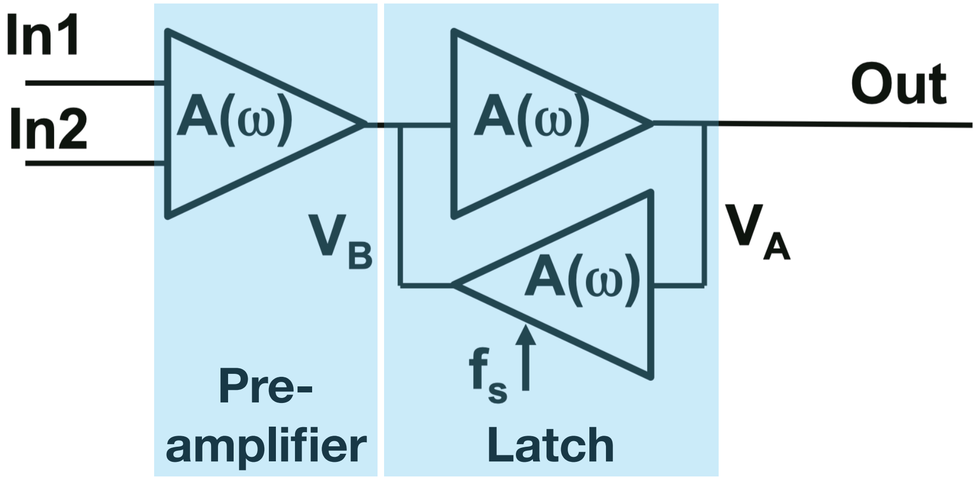
Comparators with hysteresis

Small positive feedback path:





Large positive feedback path:

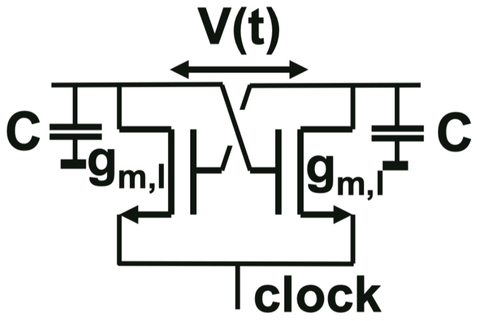


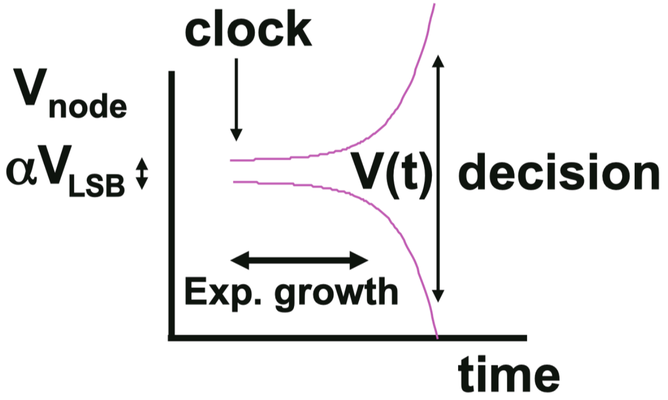
Two-phase operation:

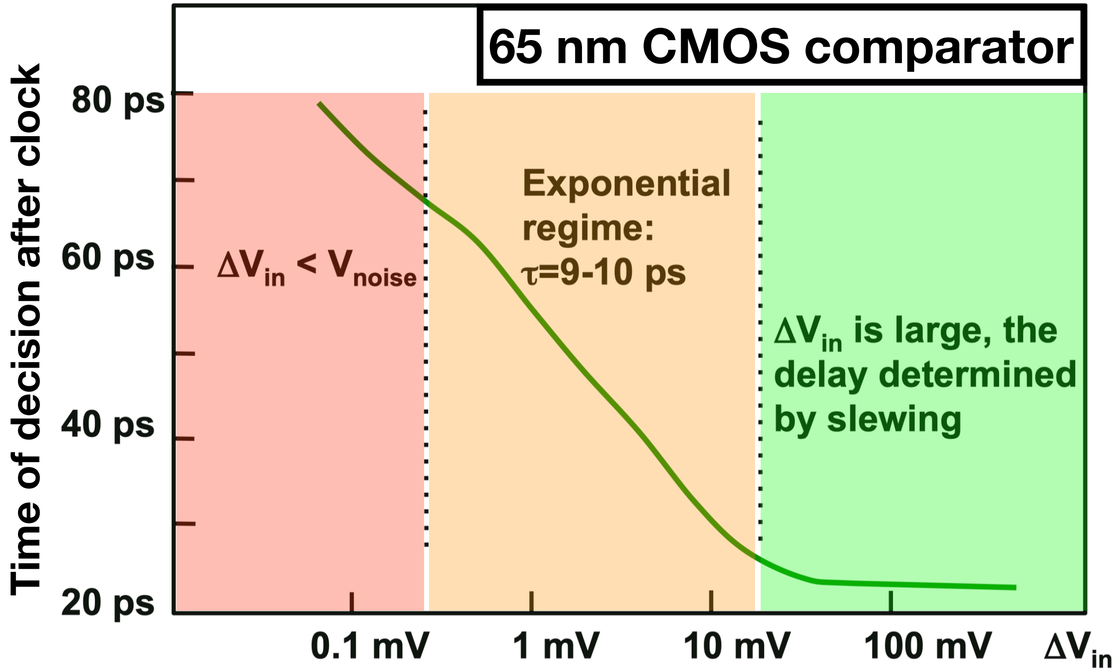
1. Pre-amplifier amplifies small input signal
2. Positive feedback stage is activated to quickly regenerate already build-up signal

Reset required to allow new signal build-up

Latch behavior





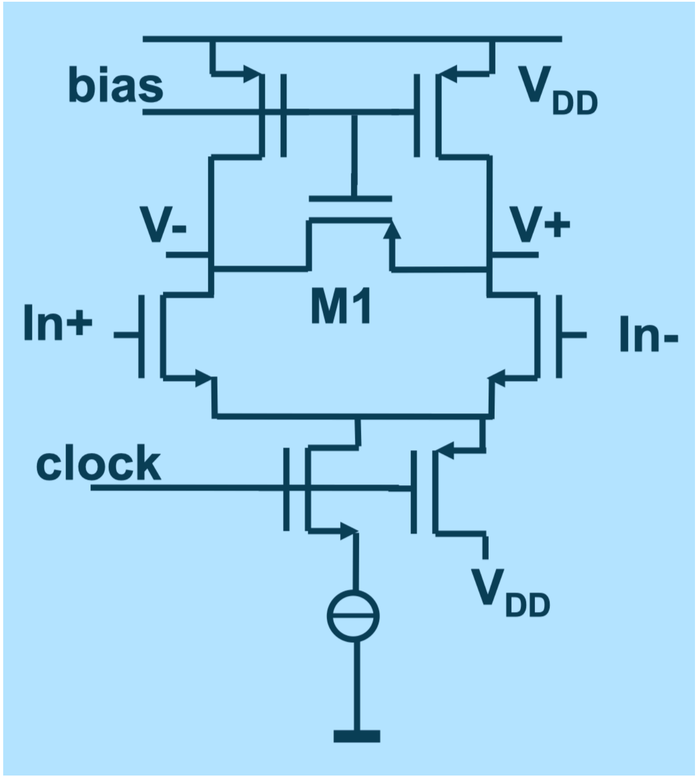


$$V(t) = \alpha V_{LSB} e^{+t/\tau} \qquad \tau = C/g_{m,l}$$

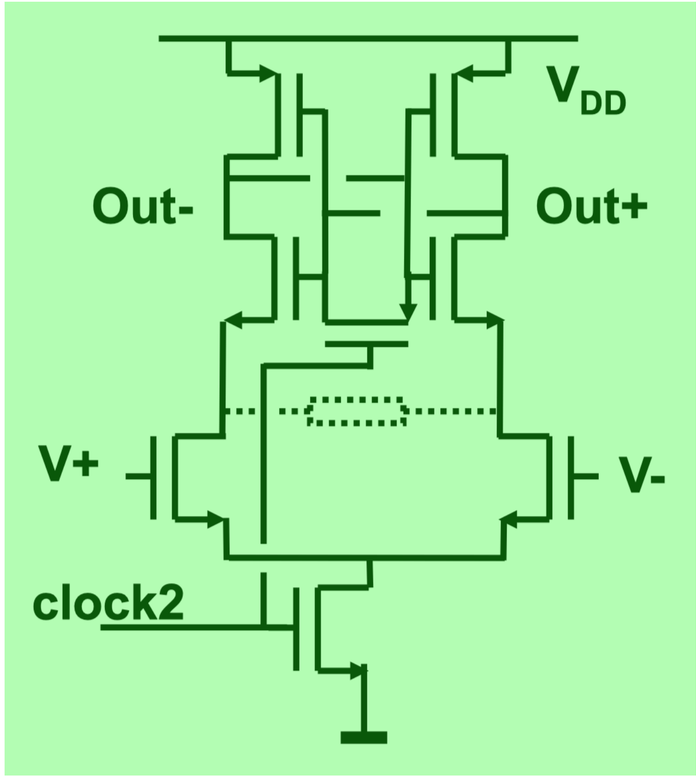
- **High ΔV_{in}:** regeneration time limited by propagation delay
- **Medium ΔV_{in}:** exponential regime
- **Small ΔV_{in}:** noise dominates input resulting in errors

Two-stage comparator

Pre-amplifier



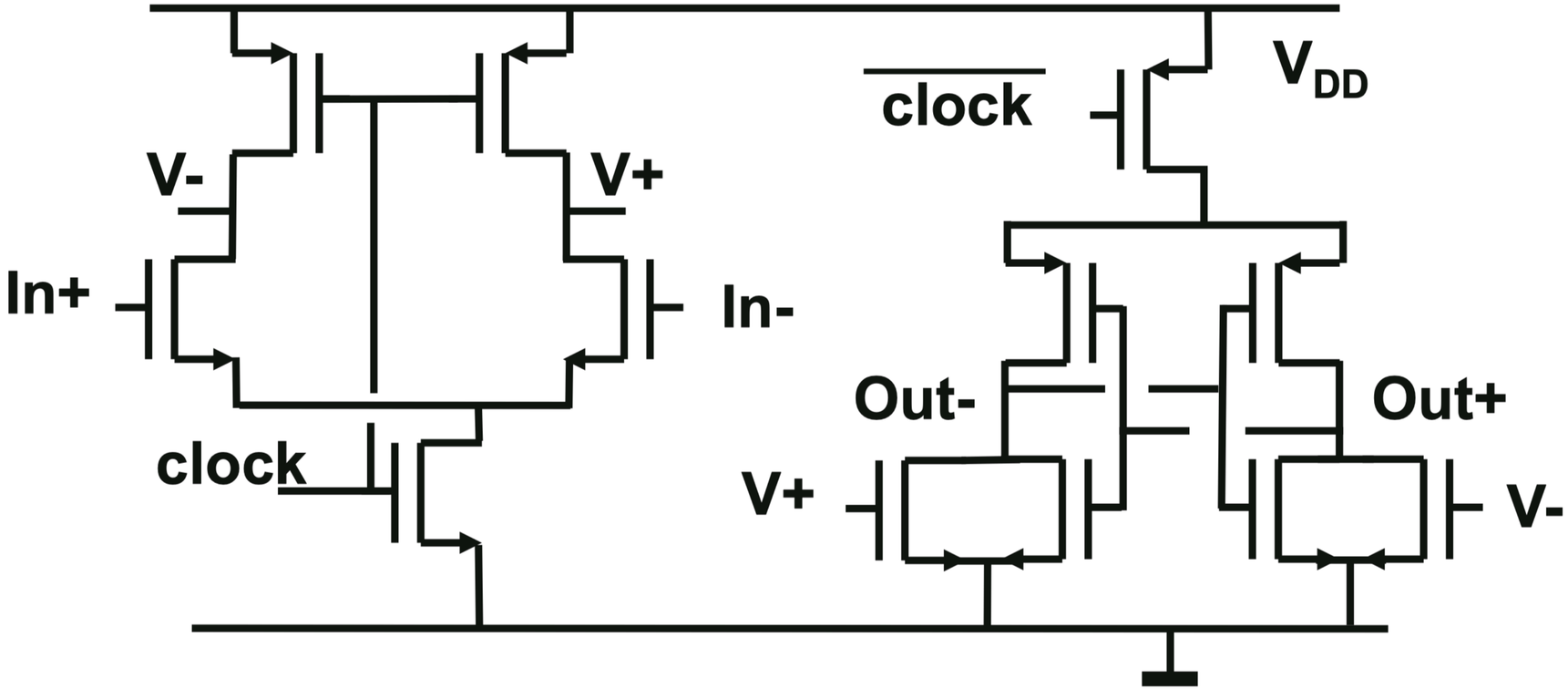
StrongARM latch



Ellersick W, Chih-Kong KY, Horowitz M, Dally W (1999) GAD: a 12-GS/s CMOS 4-bit A/D converter for an equalized multi-level link. In: Symposium on VLSI circuits, digest of technical papers, pp 49–52

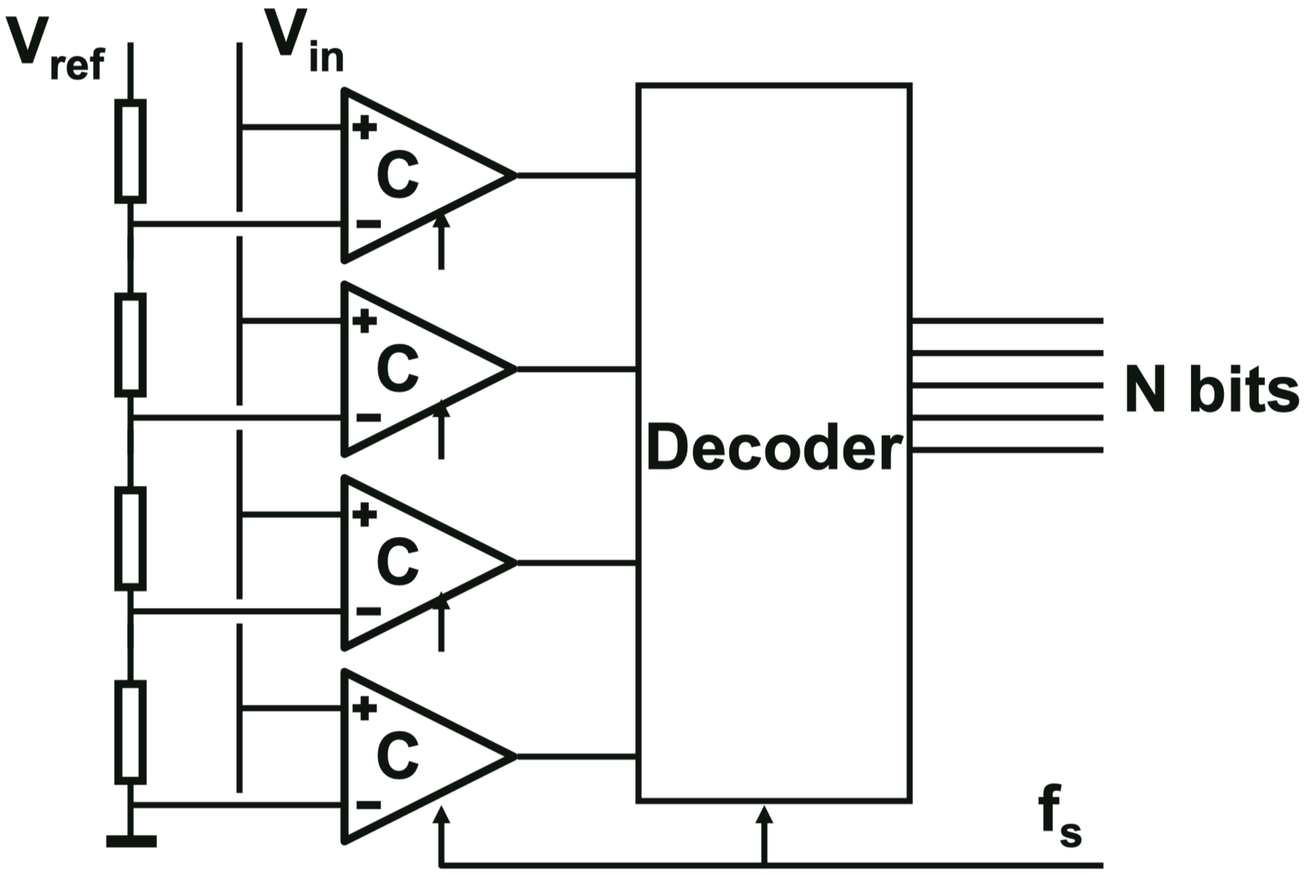
Dynamic two-stage comparator

To reduce the power consumption



Schinkel D, Mensink E, Klumperink E, van Tuijl E, Nauta B (2007) A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold Time. In: IEEE international solid-state circuits conference, digest of technical papers, pp 314–315

Flash converters



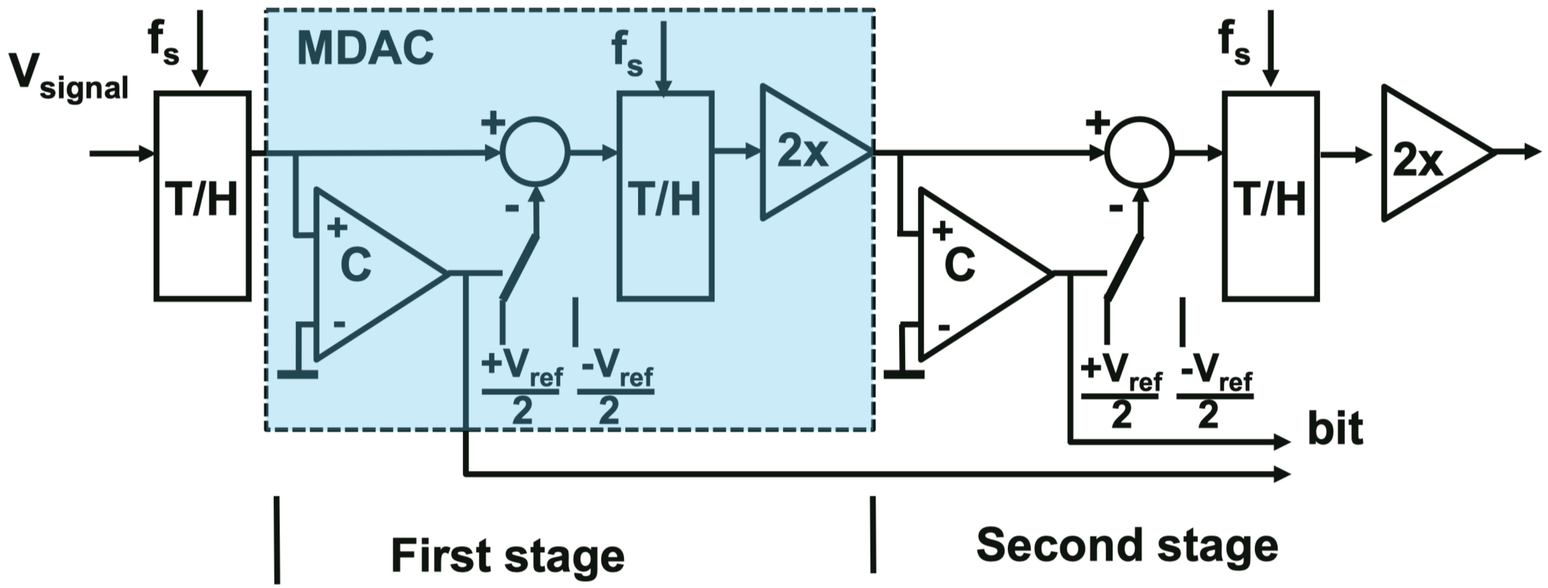
- 2^N - 1 comparators and resistors
- Comparators create thermometer code at every rising clock edge
- Decoder converts thermometer code in N-bit binary word
- Input signal only needed at rising clock edge
- Large area, high power consumption, high input capacitance

Effect of an additional bit

		N bit	N+1 bit	7 bit	8 bit
1	Input range	V_{ref}	V_{ref}	1 V	1 V
2	LSB size	$2^{-N}V_{ref}$	$2^{-(N+1)}V_{ref}$	7.8 mV	3.9 mV
3	Number of comparators	$2^N - 1$	$2^{(N+1)} - 1$	127	255
4	Probability per comparator pair for 95 % ADC yield	$p_N = \sqrt[2^N-1]{0.95}$	$p_{N+1} = \sqrt[2^{(N+1)}-1]{0.95} \approx \sqrt{p_N}$	0.99960	0.99980
5	Excess factor σ's in $N(0,\sigma)$	$z_N \approx 3 \ldots 4$	$z_{N+1} \approx z_N + 0.3$	3.35	3.55
6	Input referred random error	$2^{-N}V_{ref}/z_N\sqrt{2}$	$2^{-(N+1)}V_{ref}/z_{N+1}\sqrt{2}$	2.33 mV	1.10 mV
7	MOS pairs in comparator	3	3	3	3
8	Random error per pair	$\sigma_N = 2^{-N}V_{ref}/z_N\sqrt{6}$	$\sigma_{N+1} = 2^{-(N+1)}V_{ref}/z_{N+1}\sqrt{6}$	1.34 mV	0.63 mV
9	Area per MOS	$WL = A_{VT}^2/\sigma_N^2$	$WL = A_{VT}^2/\sigma_{N+1}^2$	6.8 µm^2	30.7 µm^2
10	Capacitance of all gates	$3 \times 2^N A_{VT}^2 C_{ox}/\sigma_N^2 = 18S_N^2 2^{3N} A_{VT}^2 C_{ox}/V_{ref}^2$	$3 \times 2^{N+1} A_{VT}^2 C_{ox}/\sigma_{N+1}^2 = 18S_{N+1}^2 2^{3(N+1)} A_{VT}^2 C_{ox}/V_{ref}^2$	11 pF	99 pF

$$\frac{C_{in,.N+1}}{C_{in,N}} = \frac{8S_{N+1}^2}{S_N^2} \approx 10 \quad \text{for } N = 5, \ldots, 8$$

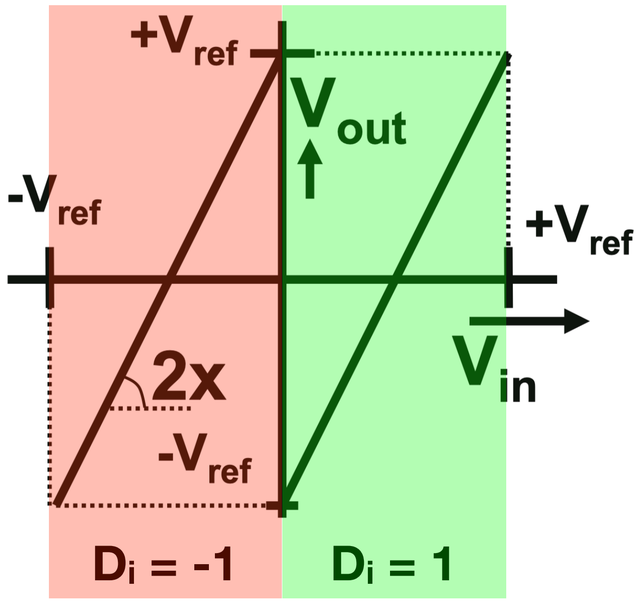
1-bit pipeline converters



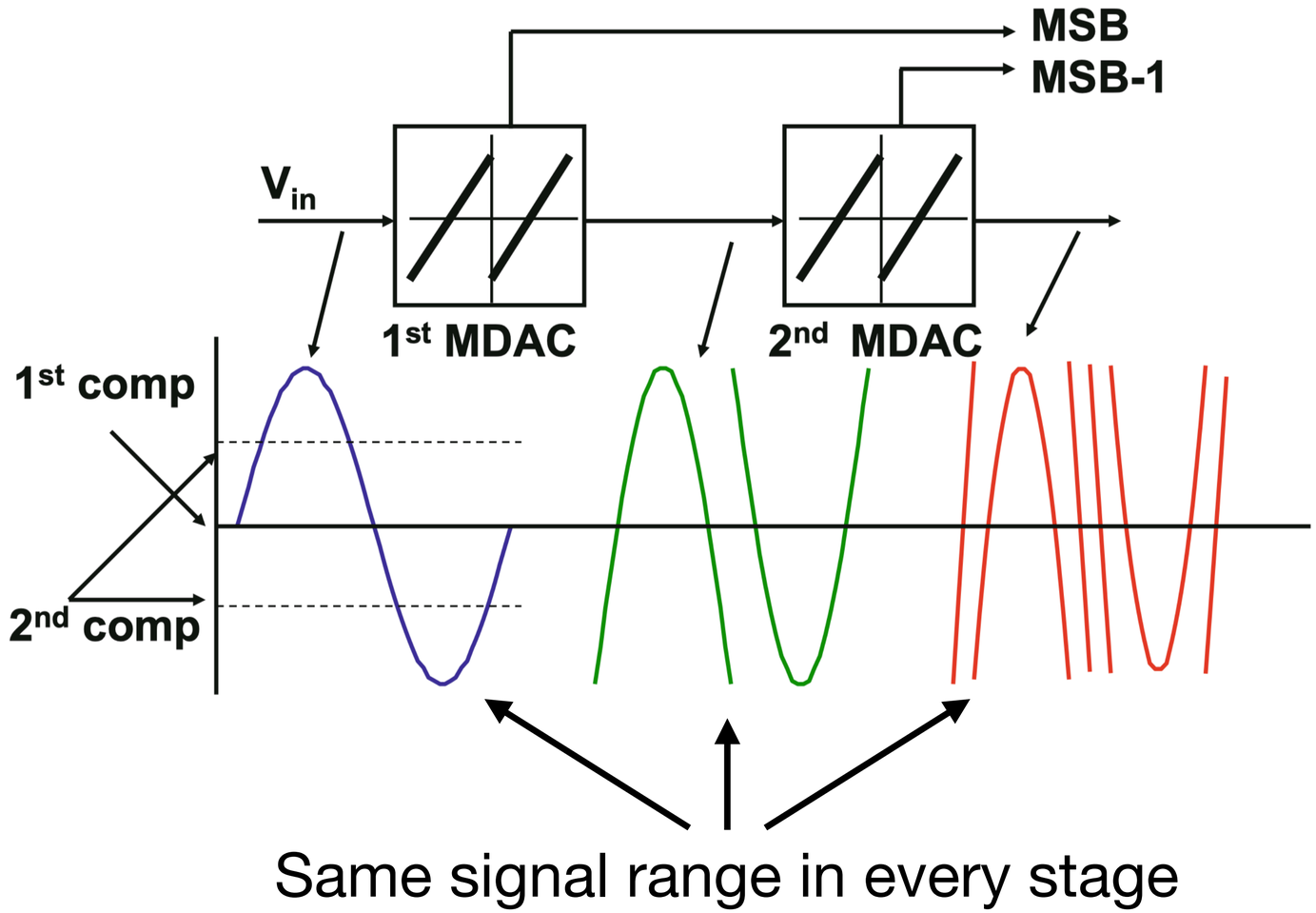
- Subrange limited to one bit → amplifier with 2x gain → **maximum speed**
- **Intrinsically linear** digital-to-analog converter → N-bit precision intrinsically achieved
- Single comparator for analog-to-digital conversion
- Basic building block is multiplying digital-to-analog converter (MDAC)
- Full digital value available after N + 3 clock periods → delay exchanged for speed
- This delay can be a problem in feedback loops

Multiplying digital-to-analog converter

MDAC transfer function

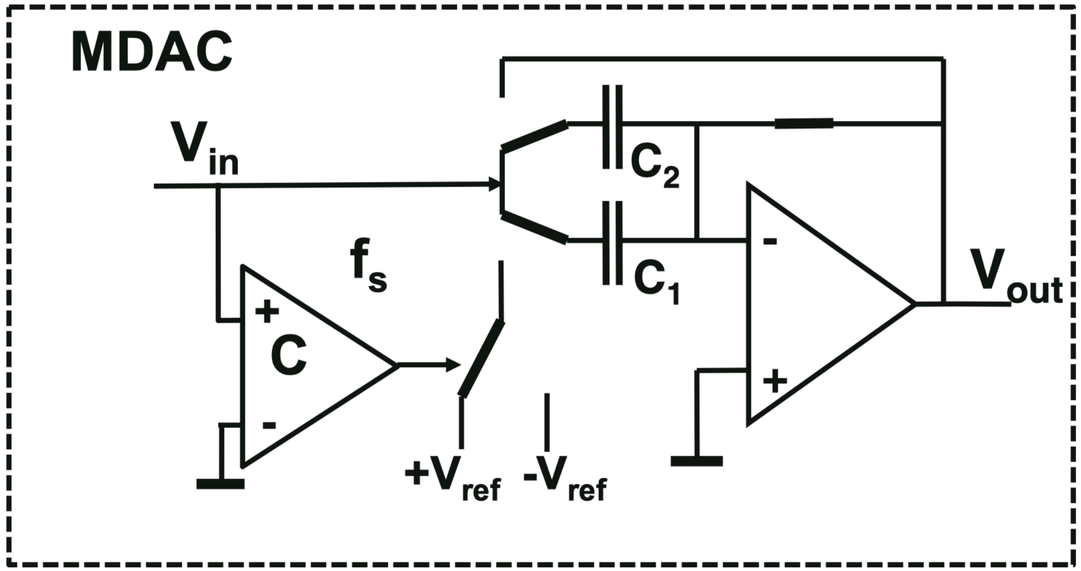


$$V_{out,i} = 2 \times V_{in,i} - D_i V_{ref}$$

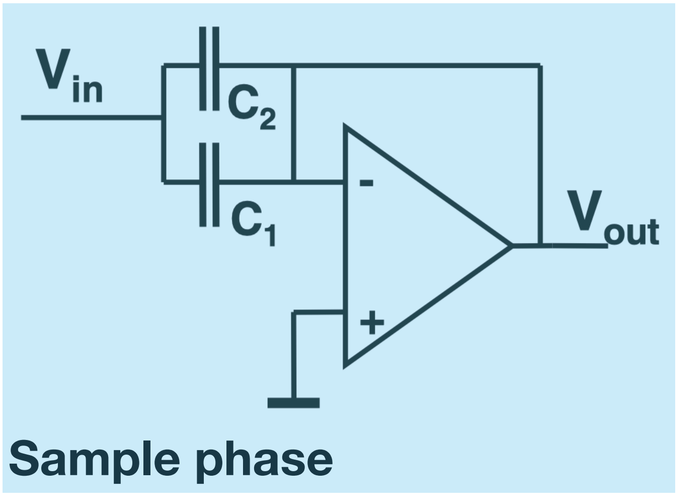


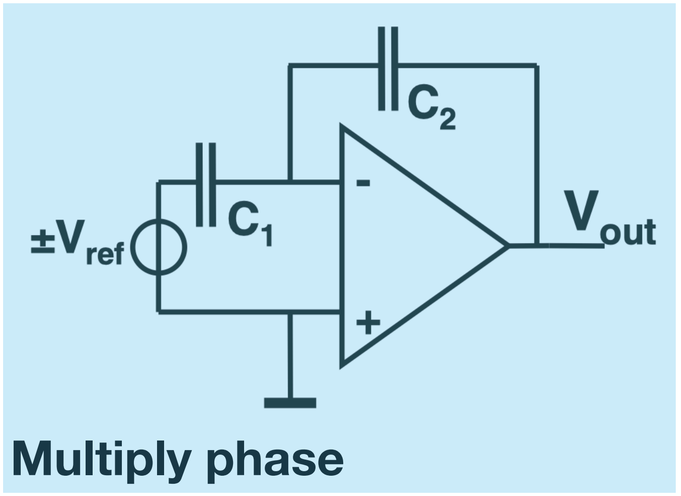
Same signal range in every stage

Multiply-by-two operation



- **Sample phase**
  Signal sampled on C_1 and C_2
- **Multiply phase**
  Charge on C_1 transferred to C_2 and V_{ref} added or subtracted depending on comparator decision



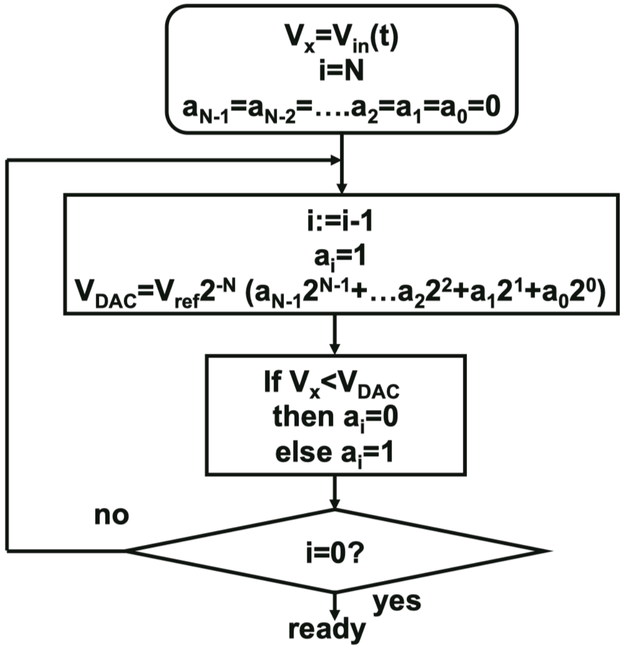


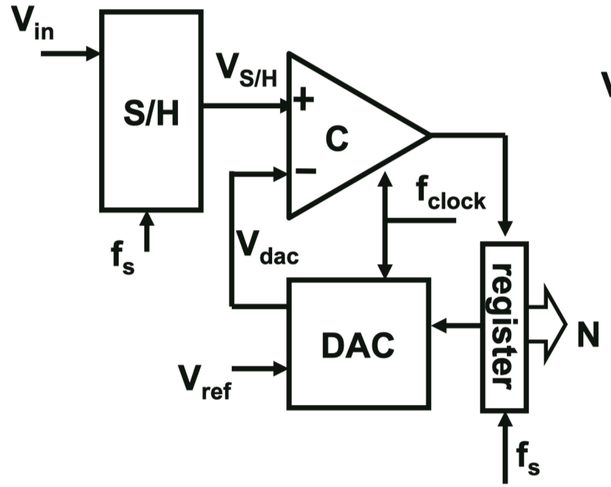
$$V_{out} = \frac{C_1 + C_2}{C_2} V_{in} \pm \frac{C_1}{C_2} V_{ref}$$

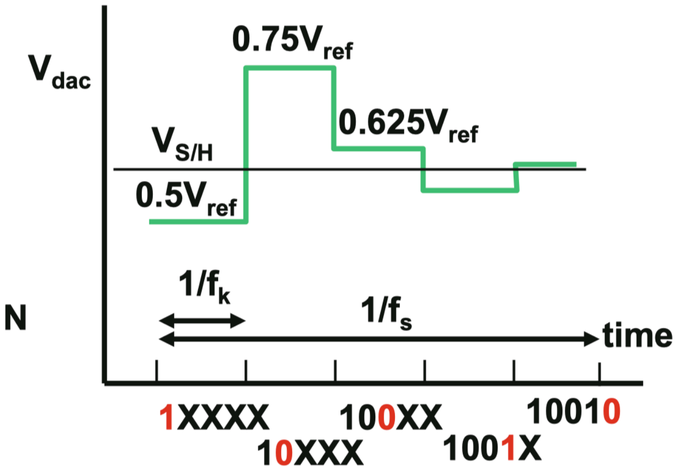
$$= 2V_{in} \pm V_{ref} \quad \text{if } C_1 = C_2$$

Successive approximation converters

≍

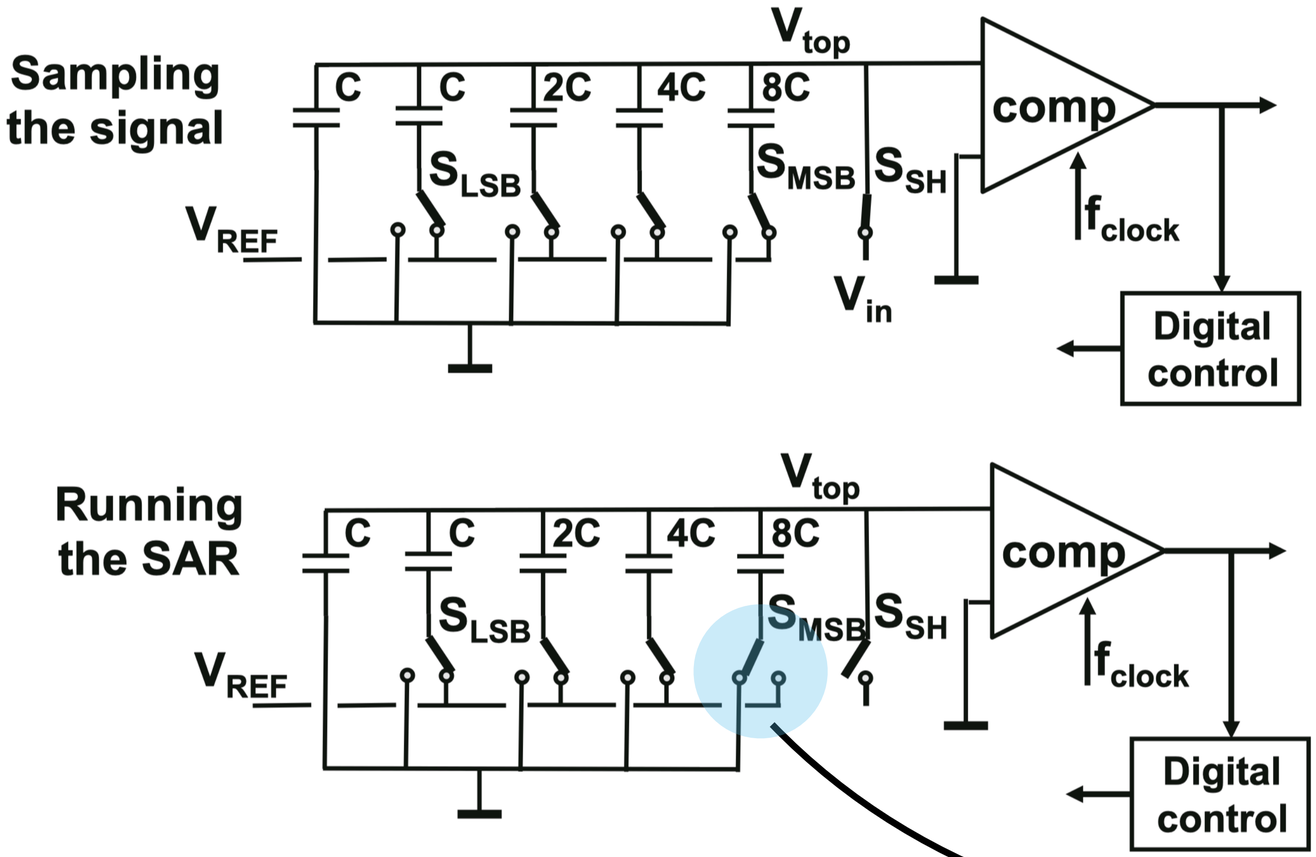






- N approximations (cycles) required for N bit ADC
- Internal clock frequency f_{clock} N times higher than sample rate f_s
- Input signal needs to be kept constant during all cycles
- MSB derived first by setting DAC to 0.5 V_{ref} (a_{N-1} = 1), comparing with input and keeping a_{N-1} to 1 or resetting it to 0

Charge-redistribution conversion

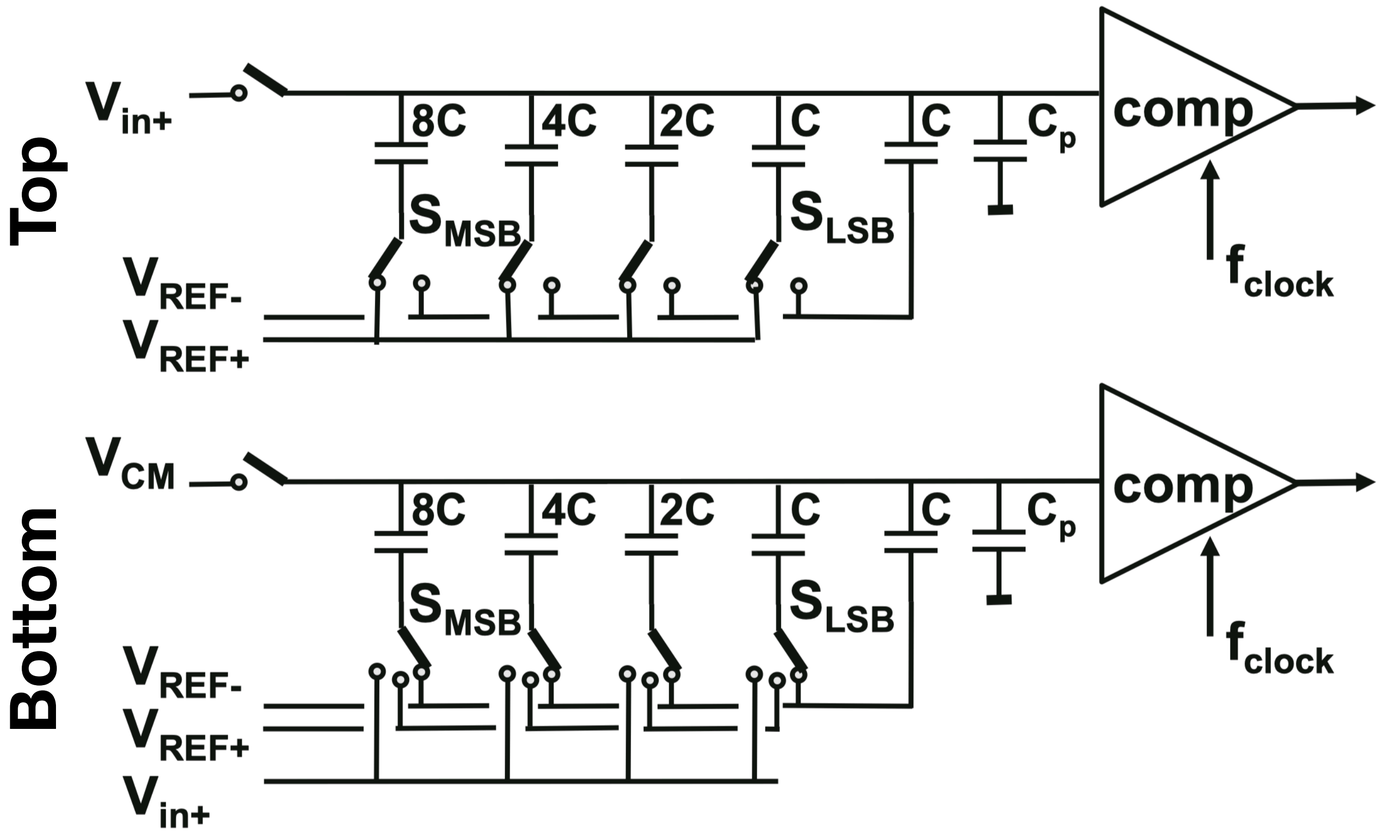


- Capacitive DAC (CDAC) enabling low power and low voltage operation
- Only capacitors, switches, comparator and logic required → profits from technology scaling
- Signal sampled on capacitor bank that is also used as DAC
- SAR operation:
  - Sampling switch remains open
  - Bottom switches toggled to bring V_{top} closer to comparator reference

$$V_{top} = V_{in} - \frac{8C}{C + C + 2C + 4C + 8C} V_{ref}$$

McCreary JL, Gray PR (1975) All-MOS charge redistribution analog-to-digital conversion techniques I. IEEE J Solid-State Circuits 10:371-379

Top-plate and bottom-plate sampling



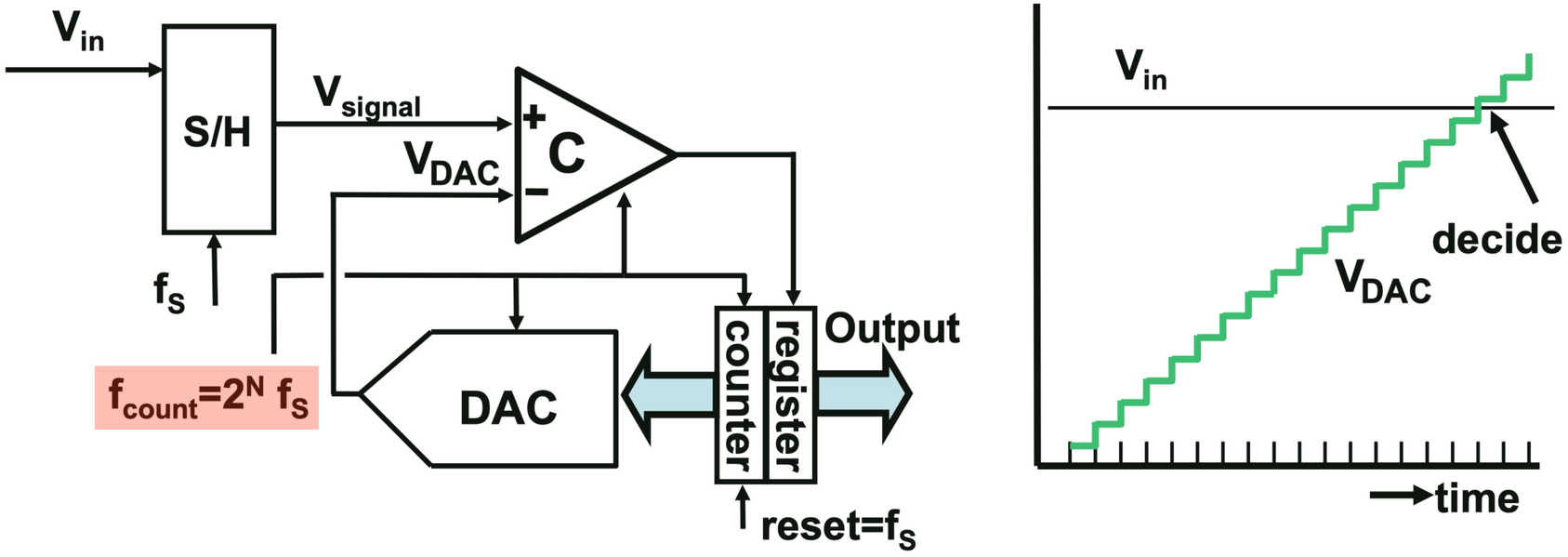
Top-plate sampling (= fast):

- No attenuation of sampled voltage
- Attenuation of reference voltage
- MSB can be determined directly after sampling

Bottom-plate sampling (= accurate):

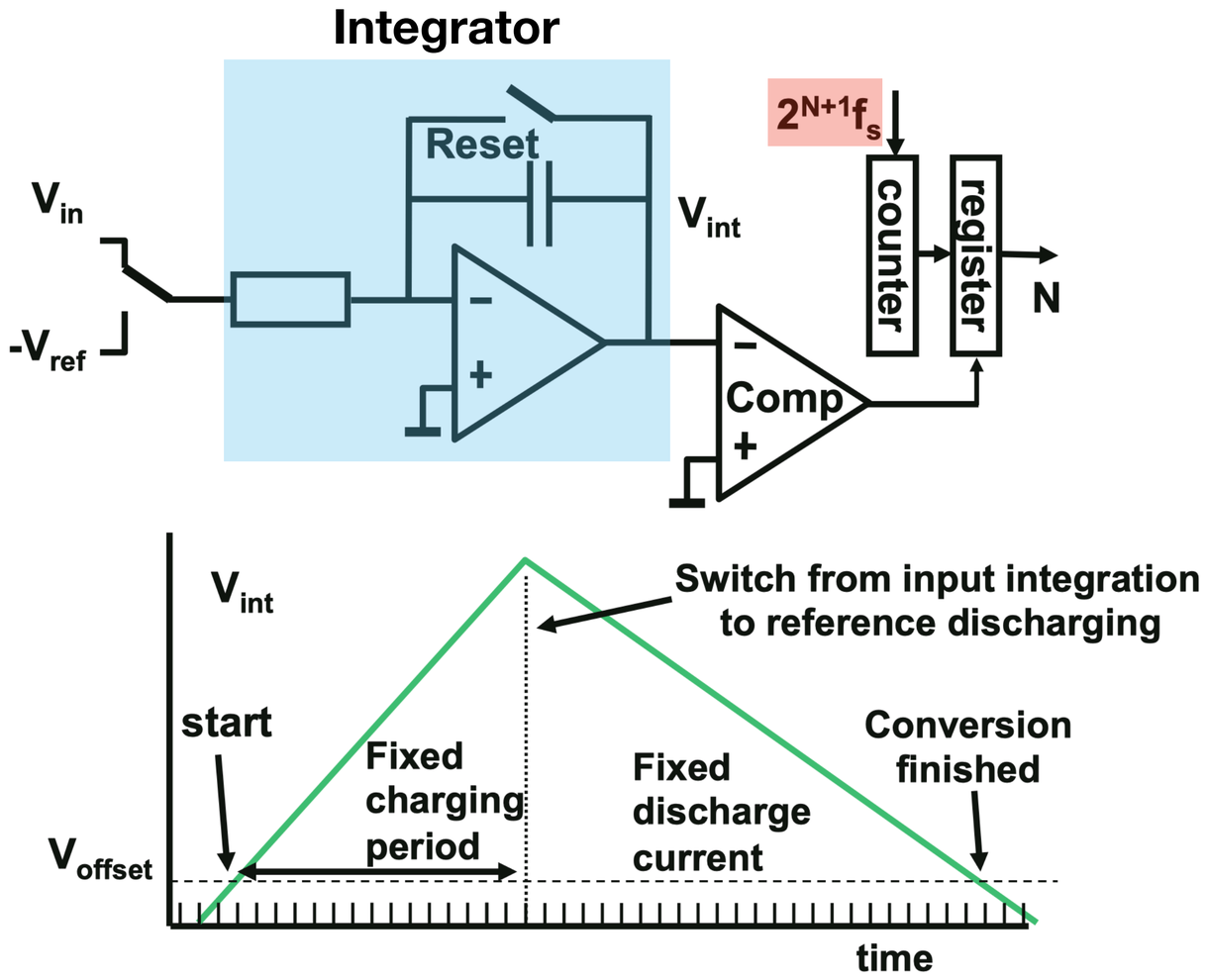
- Same attenuation for input and reference voltage
- Input voltage range can be equal to reference voltage range
- Common-mode voltage V_{CM} to keep comparator input at desired level

Linear approximation converters



- Output ready after 2^N clock cycles compared to 1 clock cycle for flash and pipeline converters and N clock cycles for SAR converters
- Counter lets DAC increase its output linearly
- When DAC output is higher than input, the comparator toggles and the counter value is stored in the register, then the counter is reset
- Also called ‘digital ramp’, ’slope’ or ‘counting’ converter

Dual-slope converters

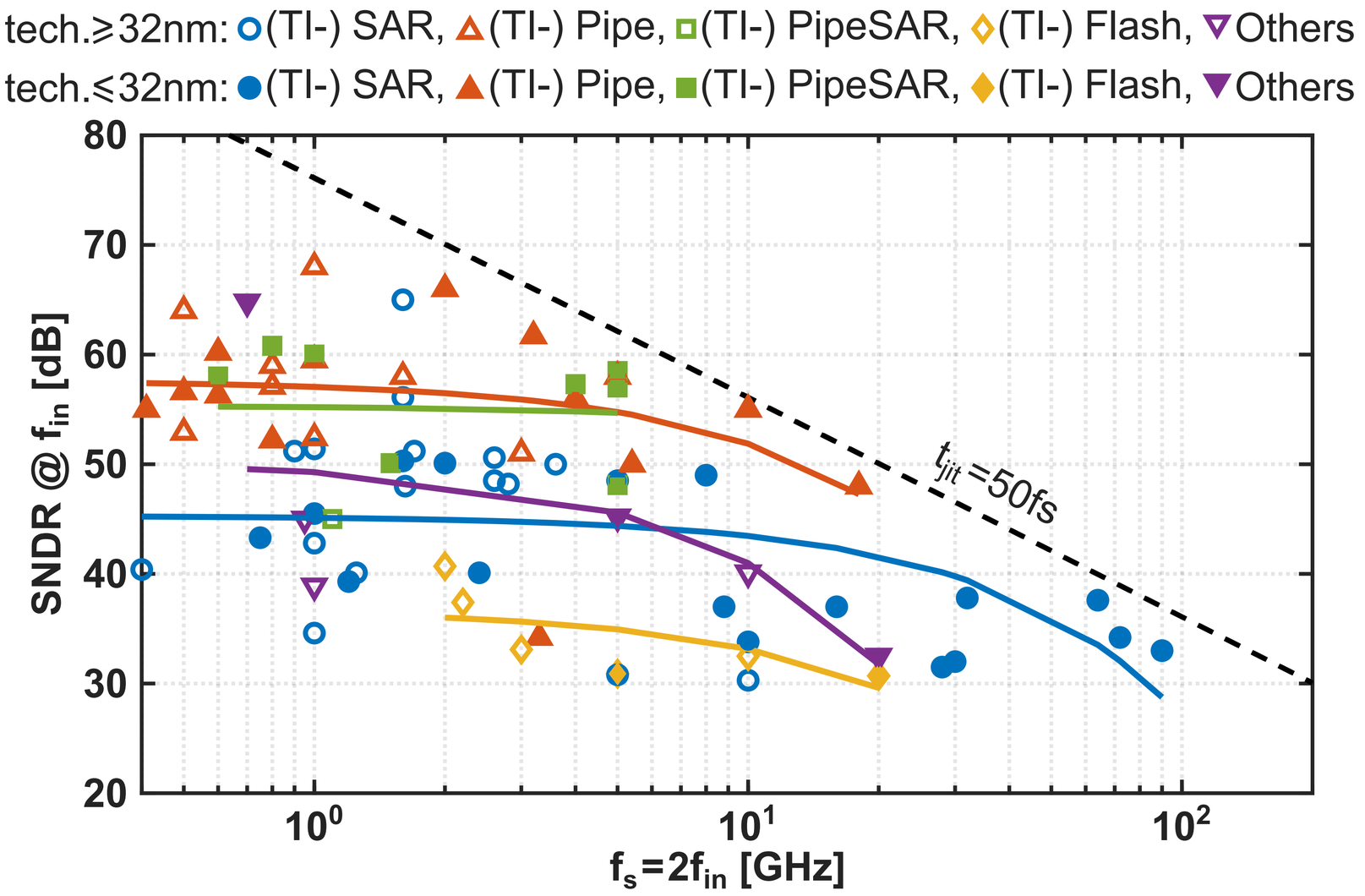


- Only suited for slowly varying input signals
- Two-phase operation:
  1. Integration of input signal during fixed sample period
  2. Discharge of integration capacitor by fixed reference current
- Conversion time $(2 \times 2^N)/f_s$
- Example of zero-crossing method
  - Unknown signal determined by subtracting equivalent signal from DAC
  - Linearity only required around zero level
  - Offsets are cancelled

Outline

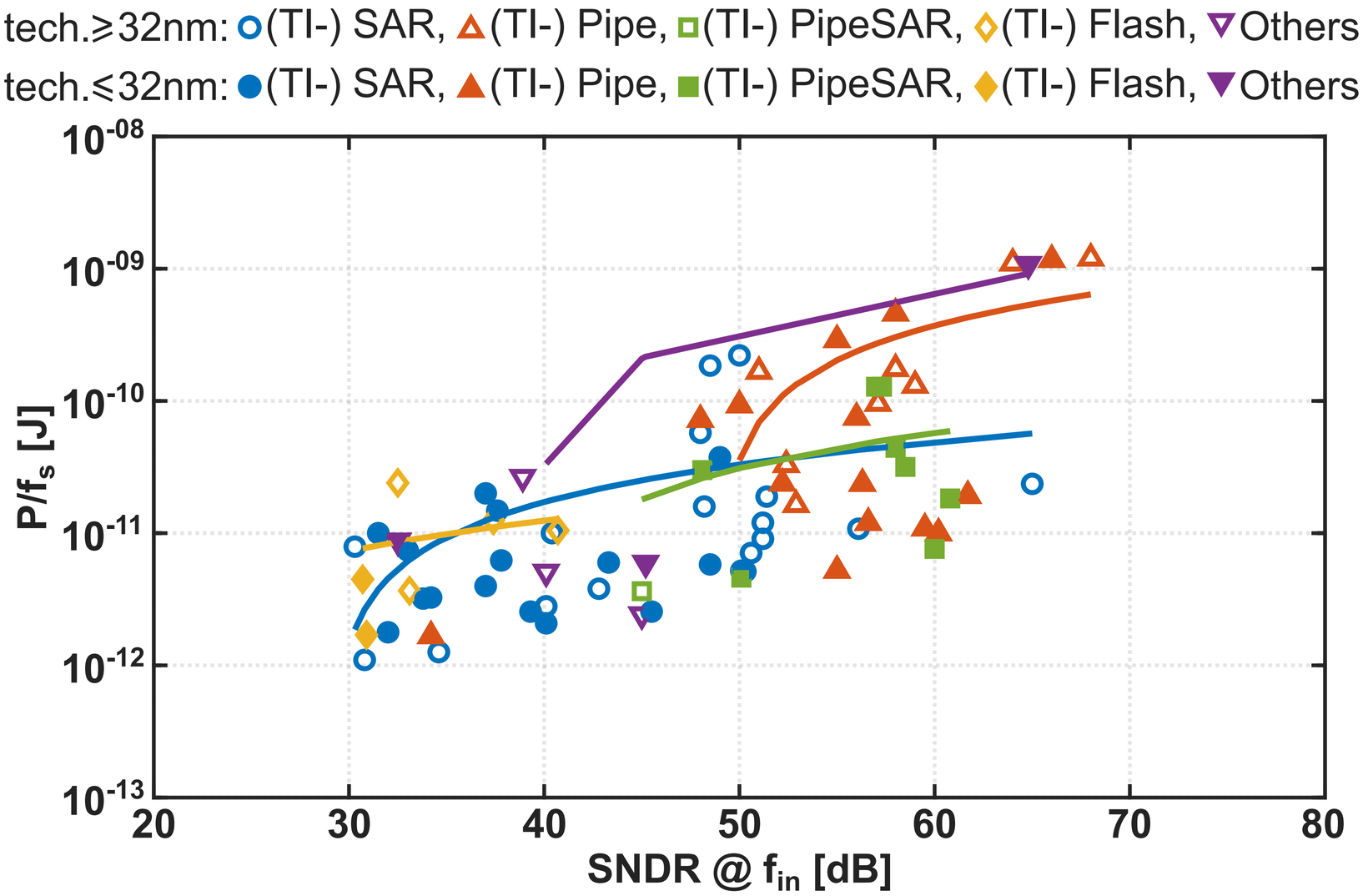
- Introduction
- Principles of Nyquist ADCs
- **Limits of Nyquist ADCs**
- Conclusion

Accuracy versus speed



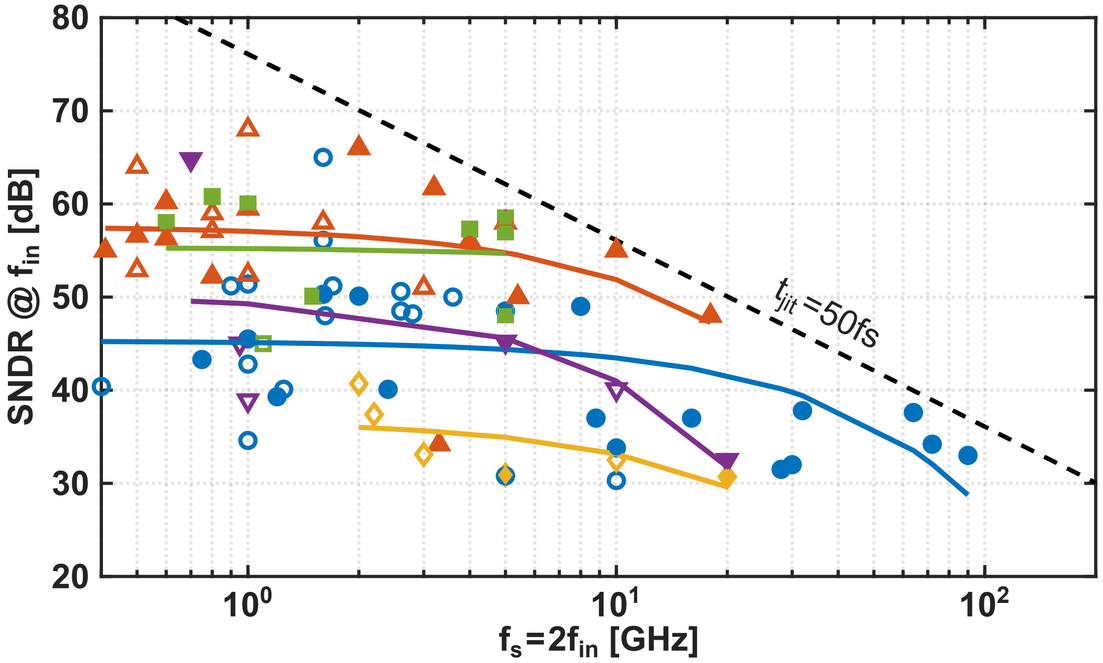
[Murmann, ADC Survey]

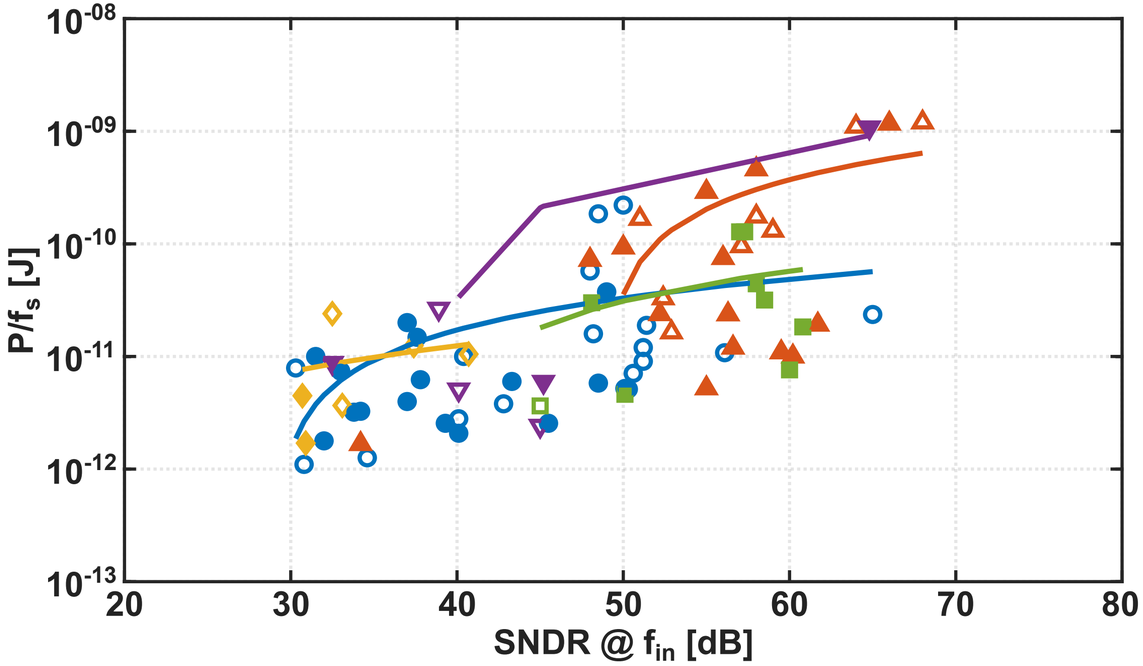
Power/speed versus accuracy



[Murmann, ADC Survey]

Accuracy-speed-power trade-off





Speed ↑ results in accuracy ↓

Accuracy ↑ results in power/speed ↑

$$\frac{\text{accuracy} \cdot \text{speed}}{\text{power}} = \text{constant} = \text{f(technology, architecture, circuit)}$$

1 2 3

[Murmann, ADC Survey]

V_{DD} and C_{min}

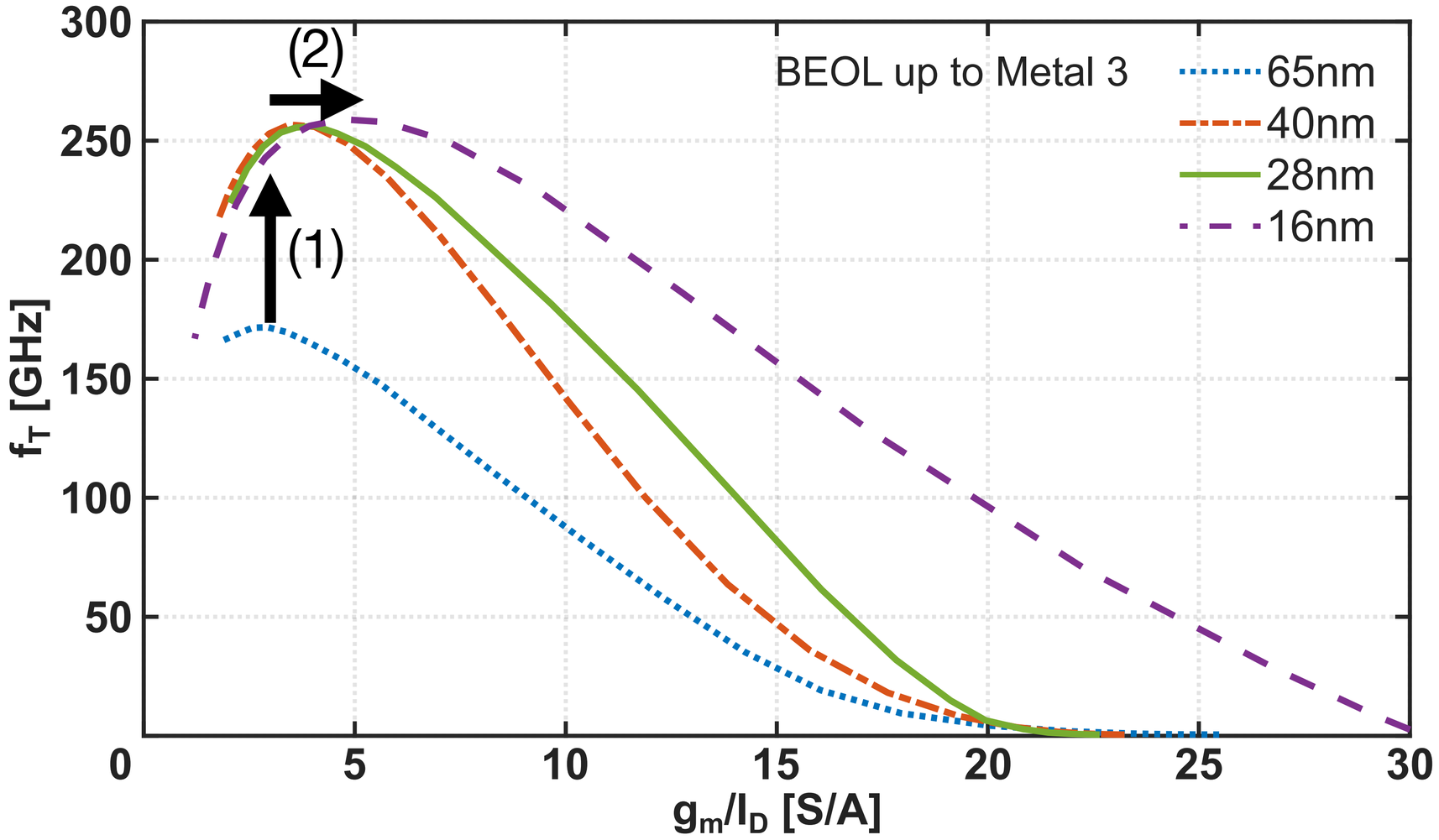
	Bulk			FinFET
	65 nm	**40 nm**	**28 nm**	**16 nm**
V_{DD}	1.2 V →	0.9 V →	0.9 V →	0.8 V
C_{min}*	960 aF →	630 aF →	570 aF →	880 aF

* extracted input capacitance of inverter with two times minimal size

g_m/I_D and f_T

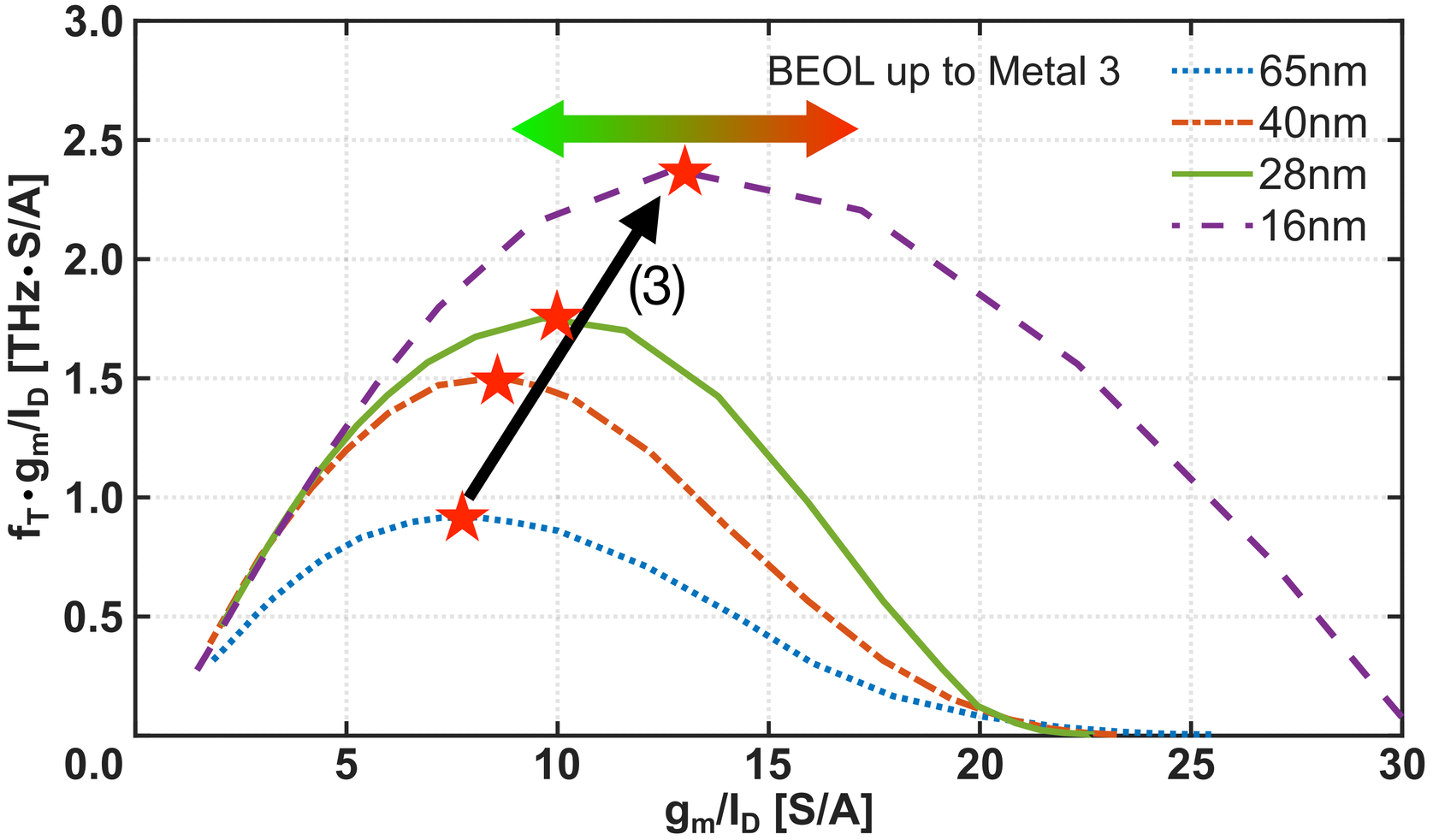
	Weak inversion	Strong inversion	Velocity saturation
$\frac{g_m}{I_D}$	$\frac{1}{n \cdot \frac{kT}{q}}$	$\frac{2}{V_{GS} - V_{TH}}$	$\frac{1}{V_{GS} - V_{TH}}$
f_T	$\frac{3 \cdot \mu}{2\pi \cdot L^2} \cdot \exp\left(\frac{V_{GS}}{n \cdot kT/q}\right)$	$\frac{3 \cdot \mu}{2\pi \cdot L^2}(V_{GS} - V_{TH})$	$\frac{v_{sat}}{2\pi \cdot L}$

f_T versus g_m/I_D



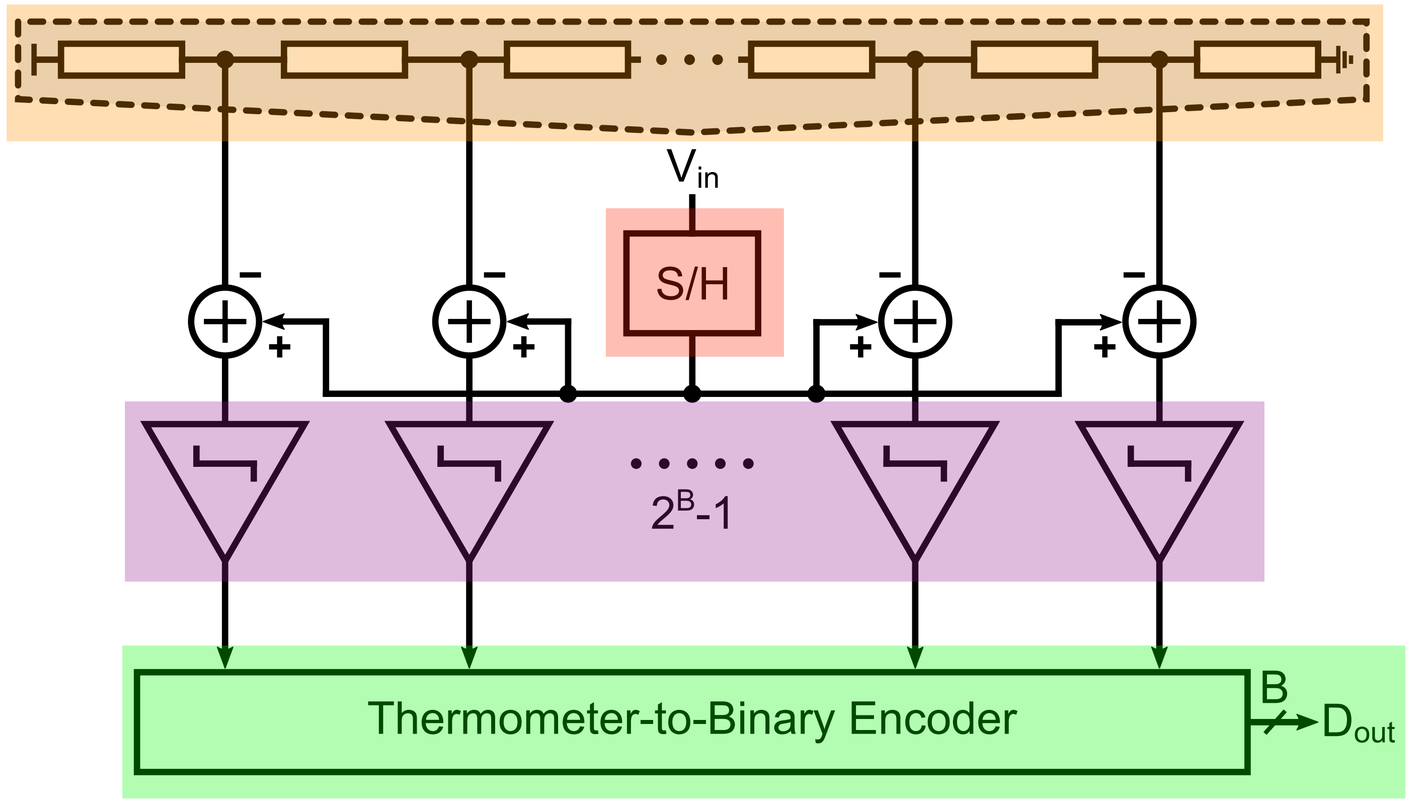
- Significant f_T benefit for technologies < 65 nm (1)
- Same f_T at lower power when scaling from 40 nm to 16 nm (2)
- Peak-f_T does not increase anymore due to increased effect of interconnect

$f_T \cdot g_m/I_D$ versus g_m/I_D



- Speed-efficiency trade-off still increases when scaling to 16 nm
- Maximum $f_T \cdot g_m/I_D$ shifts towards weak inversion when scaling to 16 nm (3)
- Wider optimum in 16 nm → easier to trade speed for power

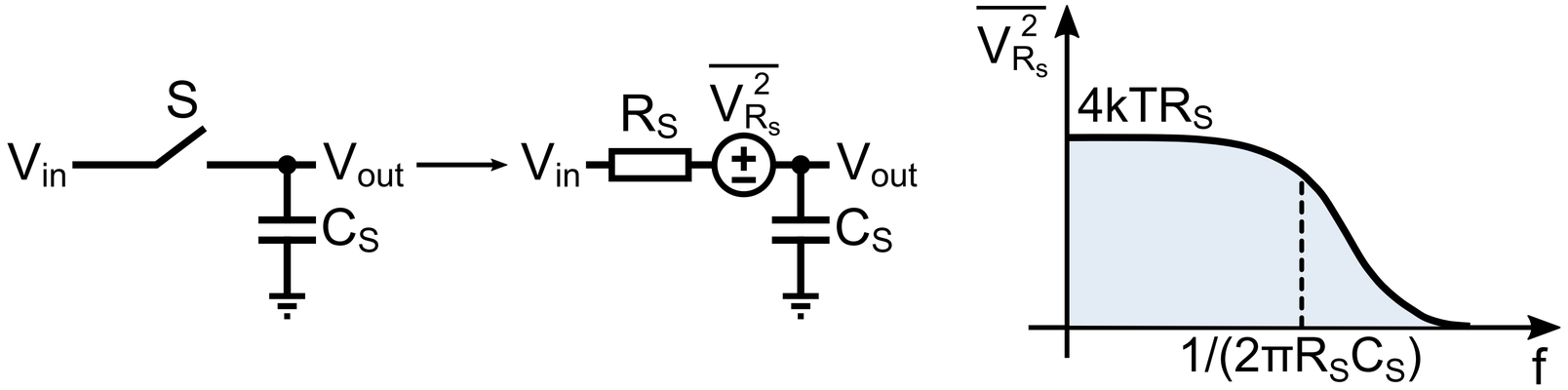
B-bit flash ADC



$$P_{\mathrm{F,tot}} = P_{\mathrm{F,samp}} + \left(2^B - 1\right) \cdot P_{\mathrm{F,comp}} + P_{\mathrm{F,lad}} + P_{\mathrm{F,dig}}$$

- Fastest architecture, shortest delay
- Exponential increase in number of components:
  - 2^B - 1 comparators
  - 2^B resistors
- Exponential increase in area per component to guarantee noise and matching limits
- Many comparators: power, noise, offset, kickback

Sampler power consumption

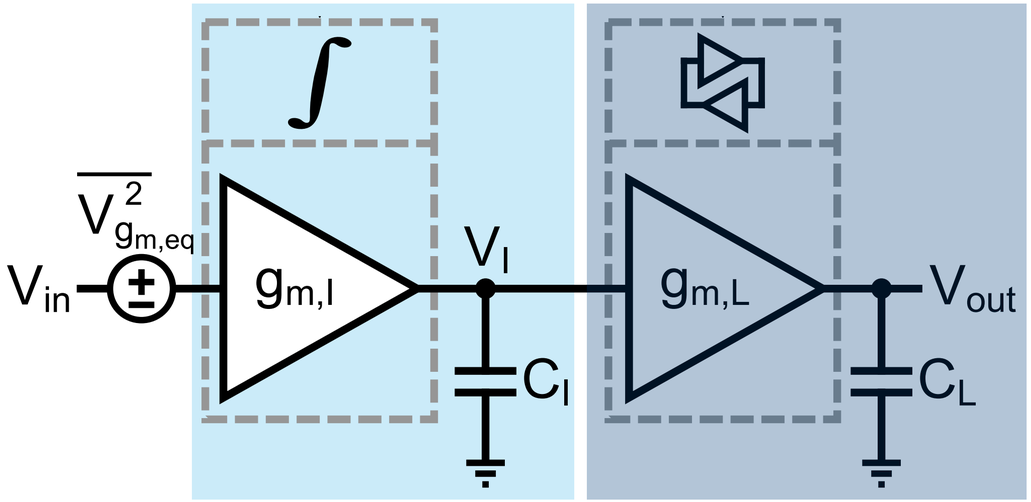


- Sampling capacitance determined by converter LSB: $C_S = \dfrac{2^{2B} \cdot 12 \cdot kT}{\left(\phi_{\text{sup}} \cdot V_{\text{DD}}\right)^2}$

- $P_{\text{F,samp}} = V_{\text{DD}} \cdot I_{\text{F,samp}} = V_{\text{DD}} \cdot \text{NTC} \cdot \theta_{\text{F,samp}}^{-1} \cdot f_s \cdot \phi_{\text{sup}} \cdot V_{\text{DD}} \cdot \left(C_S + \left(2^B - 1\right) \cdot C_{\text{in,comp}}\right)$

- B: # bits, ϕ_{sup}: fraction of supply voltage used for signal, $\theta_{\text{F,samp}}$: fraction of sample period for sampling, NTC: # time constants for settling

Comparator power consumption



- Integrator determines noise, latch determines metastability (BER)
- $$P_{\mathrm{F,comp}} = V_{\mathrm{DD}} \cdot \theta_{\mathrm{F,comp}}^{-1} \cdot f_{\mathrm{s}} \cdot \left(C_{\mathrm{I}} \cdot \Delta V_{\mathrm{I}} + \left(\left(B - \log_2 A_{\mathrm{I}} \right) \cdot \ln 2 + \ln \mathrm{BER}^{-1} \right) \cdot C_{\mathrm{L}} \cdot \frac{I_{\mathrm{D,L}}}{g_{\mathrm{m,L}}} \right)$$

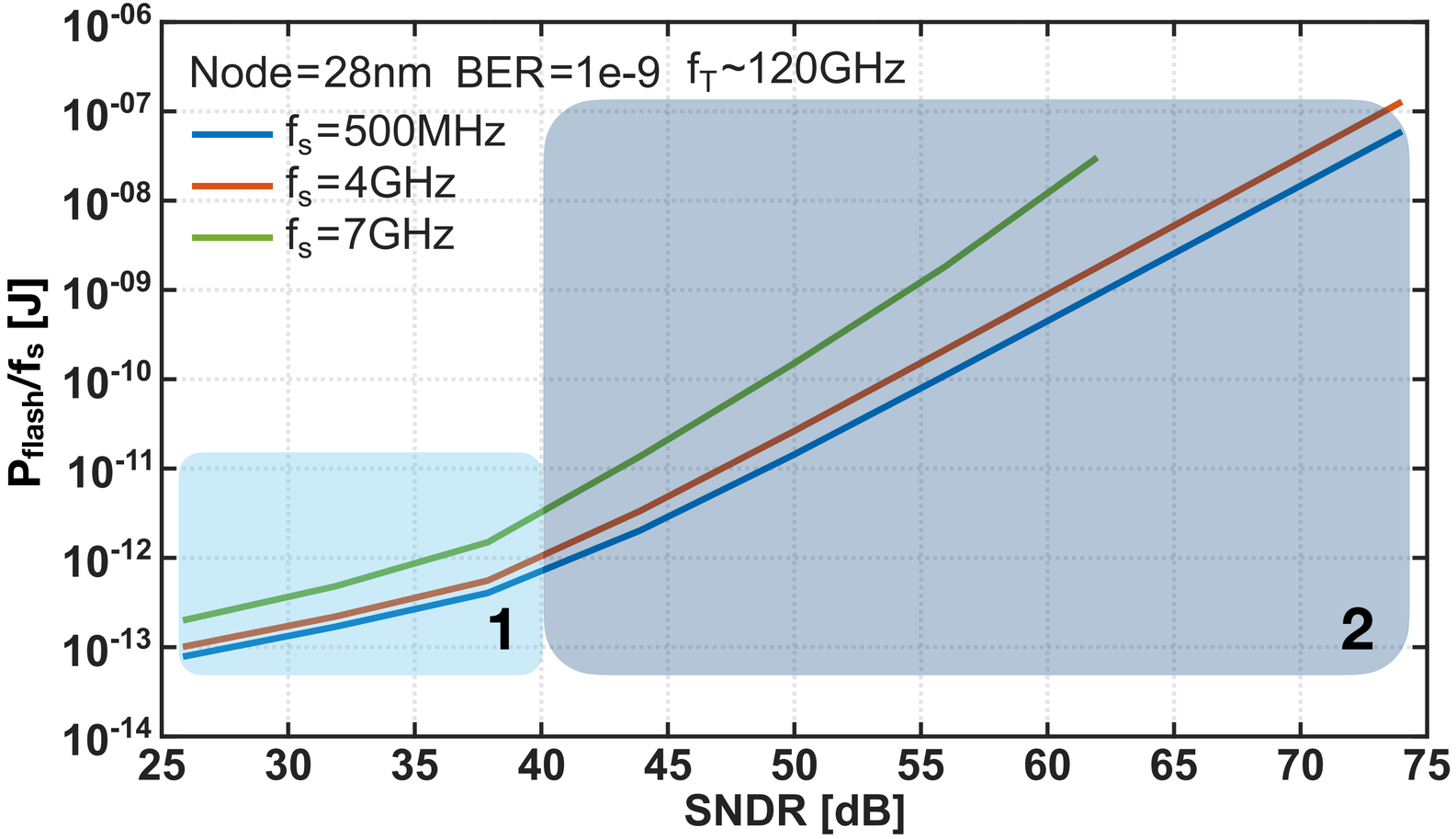
$\theta_{\mathrm{F,comp}}$: fraction of sample period for comparison, ΔV_{I}: voltage drop at integrator output, A_{I}: integrator gain, $I_{\mathrm{D,L}}$: current in latch, $g_{\mathrm{m,L}}$: transconductance in latch

Flash ADC power consumption

$$P_{\mathrm{F,tot}} = P_{\mathrm{F,samp}} + \left(2^B - 1\right) \cdot P_{\mathrm{F,comp}} + P_{\mathrm{F,lad}} + P_{\mathrm{F,dig}}$$

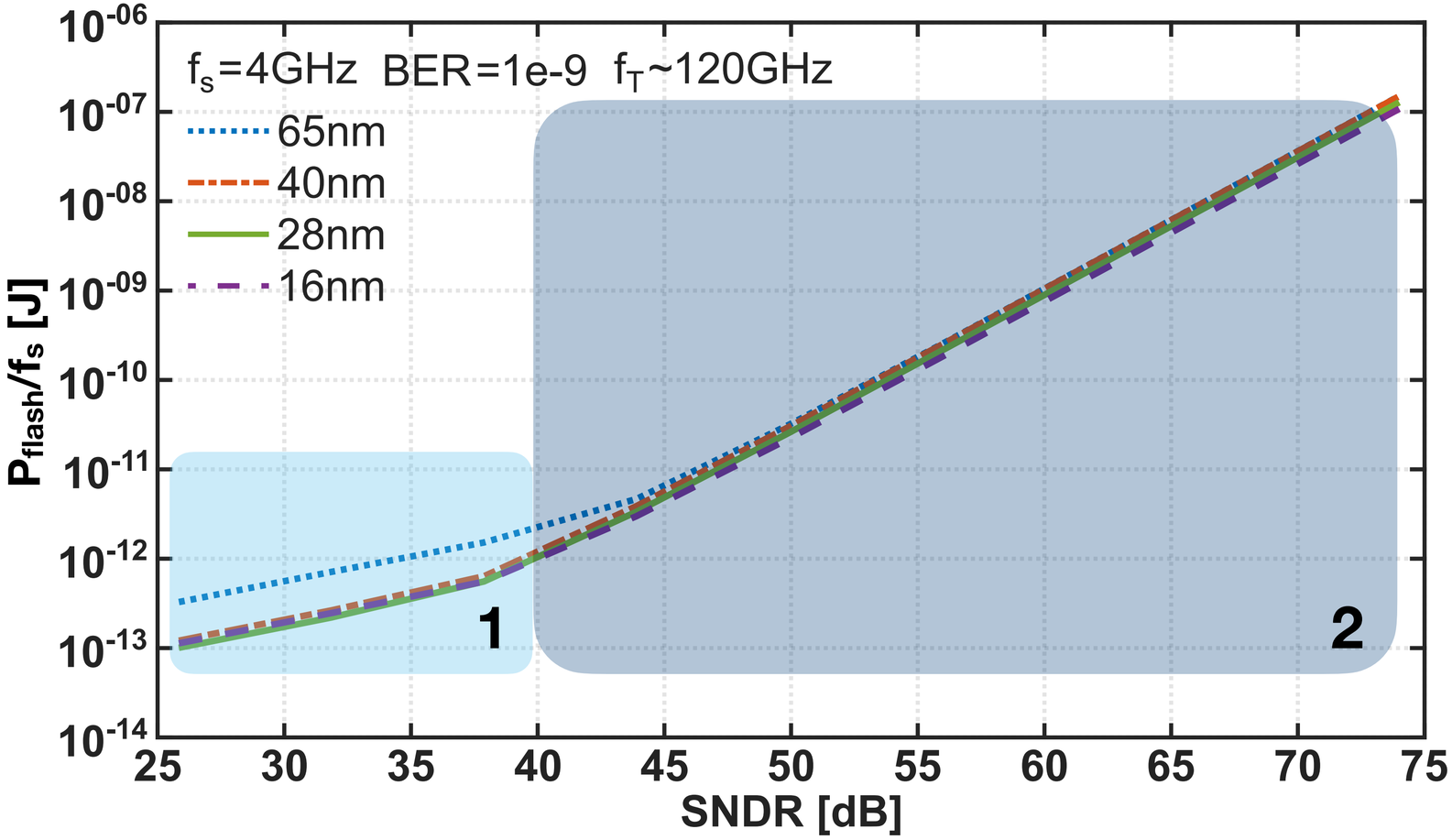
- $P_{\mathrm{F,samp}}$ and $P_{\mathrm{F,comp}}$
  - Sample period divided between sampler and comparators, ex. $\theta_{\mathrm{F,samp}} = \theta_{\mathrm{F,comp}} = 0.5$
  - Thermal noise partitioning between sampler and comparators
- $P_{\mathrm{F,lad}} = \dfrac{\left(\phi_{\mathrm{sup}} \cdot V_{\mathrm{DD}}\right)^2}{R_{\mathrm{lad}}}$ for DC power through resistor ladder
  - R_{lad} needs to be small enough to limit its noise and settling time constant
- $P_{\mathrm{F,dig}} = V_{\mathrm{DD}}^2 \cdot f_{\mathrm{s}} \cdot C_{\mathrm{min}} \cdot \#\mathrm{gates}$ for thermometer-to-binary encoder

Flash ADCs at different f_s



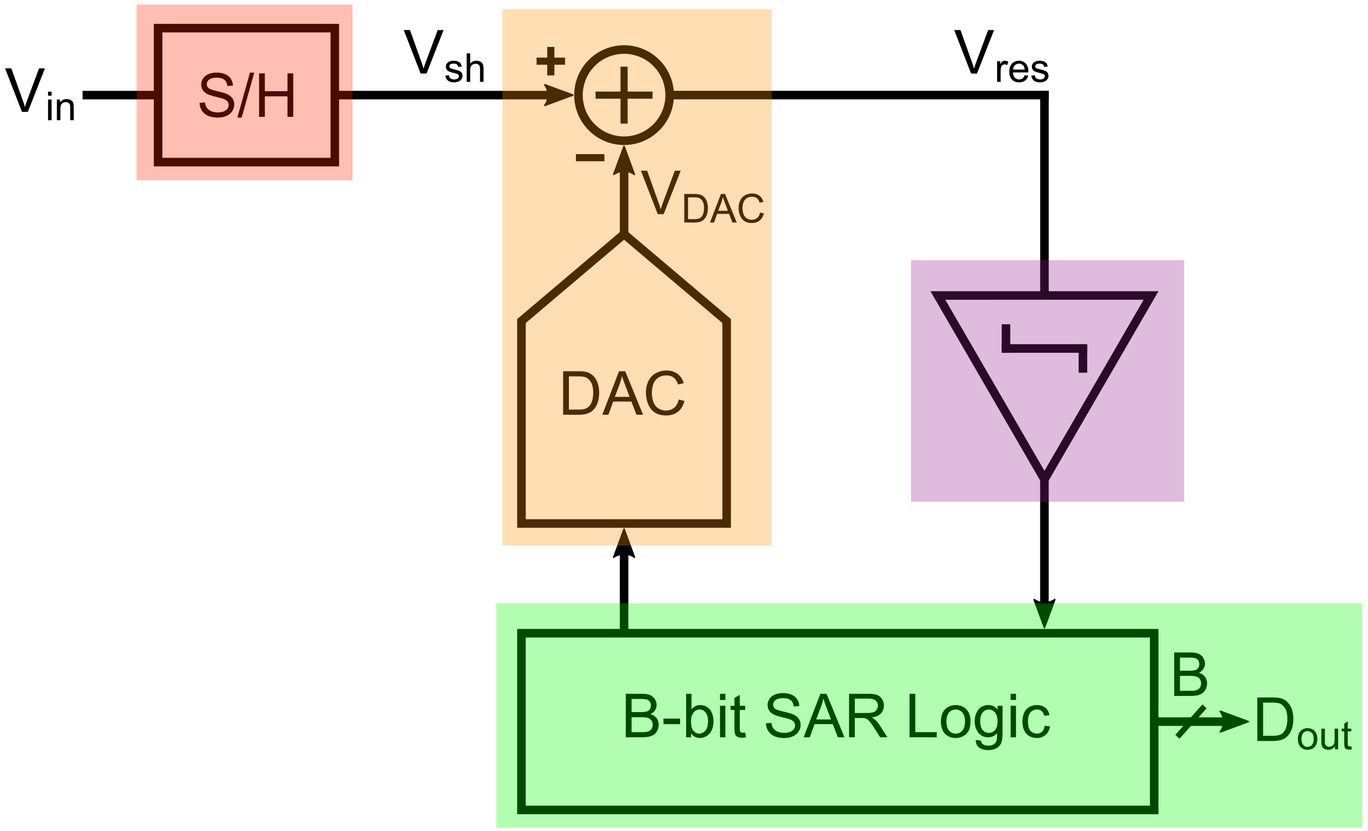
- Two regions:
  1. **SNDR ≤ 40 dB**
     Power/speed determined by C_{min}
  2. **SNDR > 40 dB**
     Power/speed determined by noise
- Technology parasitics push power/speed up increasingly as f_s/f_T increases

Scaling of flash ADCs



- Same two regions
- Smaller C_{min} in region 1 results in lower power/speed
- Similar power/speed in noise-limited region 2
- Lower V_{DD} leveraged by higher g_m/I_D for same f_T

B-bit SAR ADC



$$P_{SA,tot} = P_{SA,samp} + B \cdot P_{SA,comp} + P_{SA,DAC} + P_{SA,dig}$$

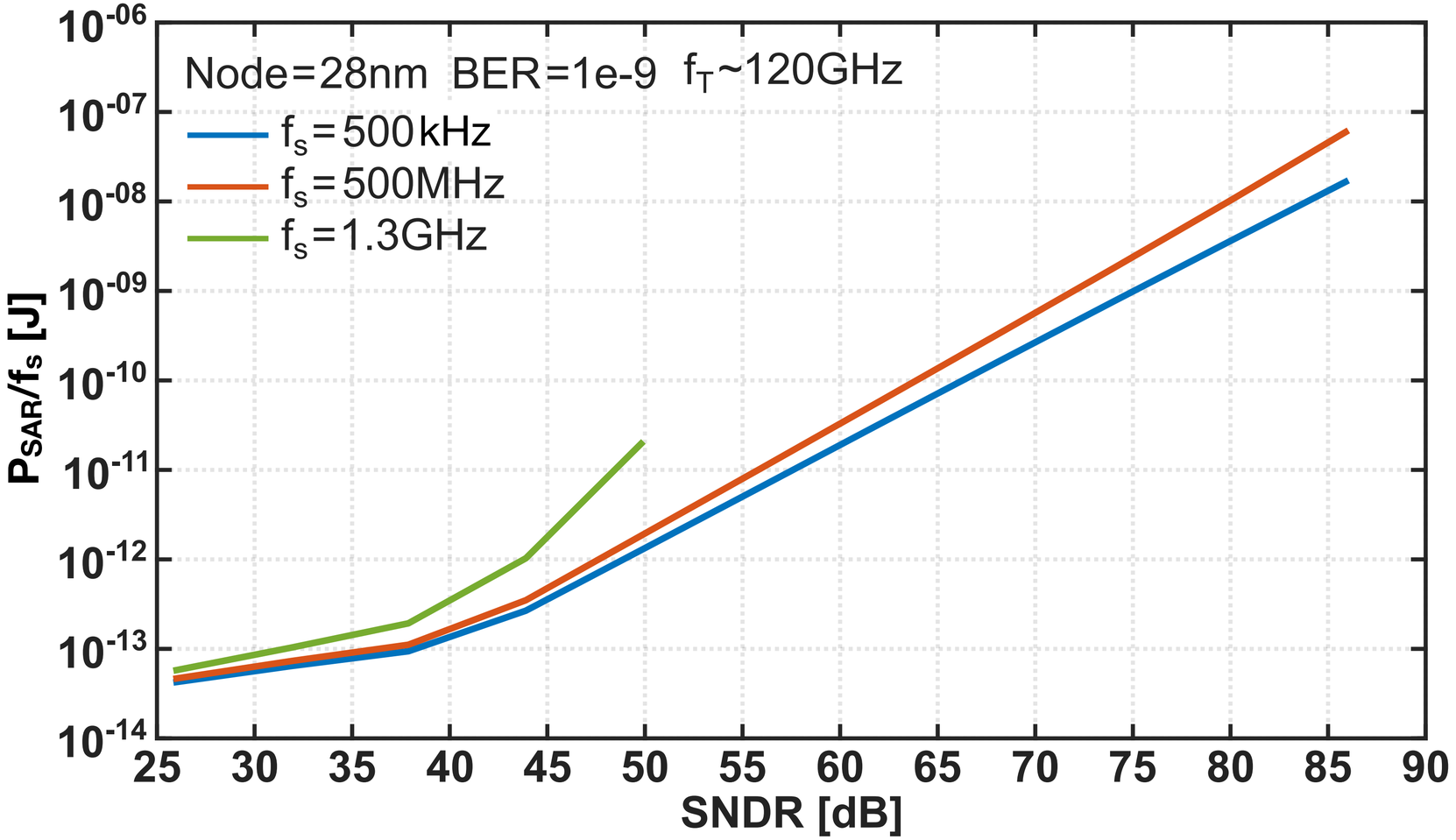
- B clock cycles per sample
- Minimal hardware thanks to hardware reuse
- Highly digital architecture, scaling well in smaller technologies
- DAC is typically capacitive DAC (CDAC) with several possible switching schemes

SAR ADC power consumption

$$P_{\mathrm{SA,tot}} = P_{\mathrm{SA,samp}} + B \cdot P_{\mathrm{SA,comp}} + P_{\mathrm{SA,DAC}} + P_{\mathrm{SA,dig}}$$

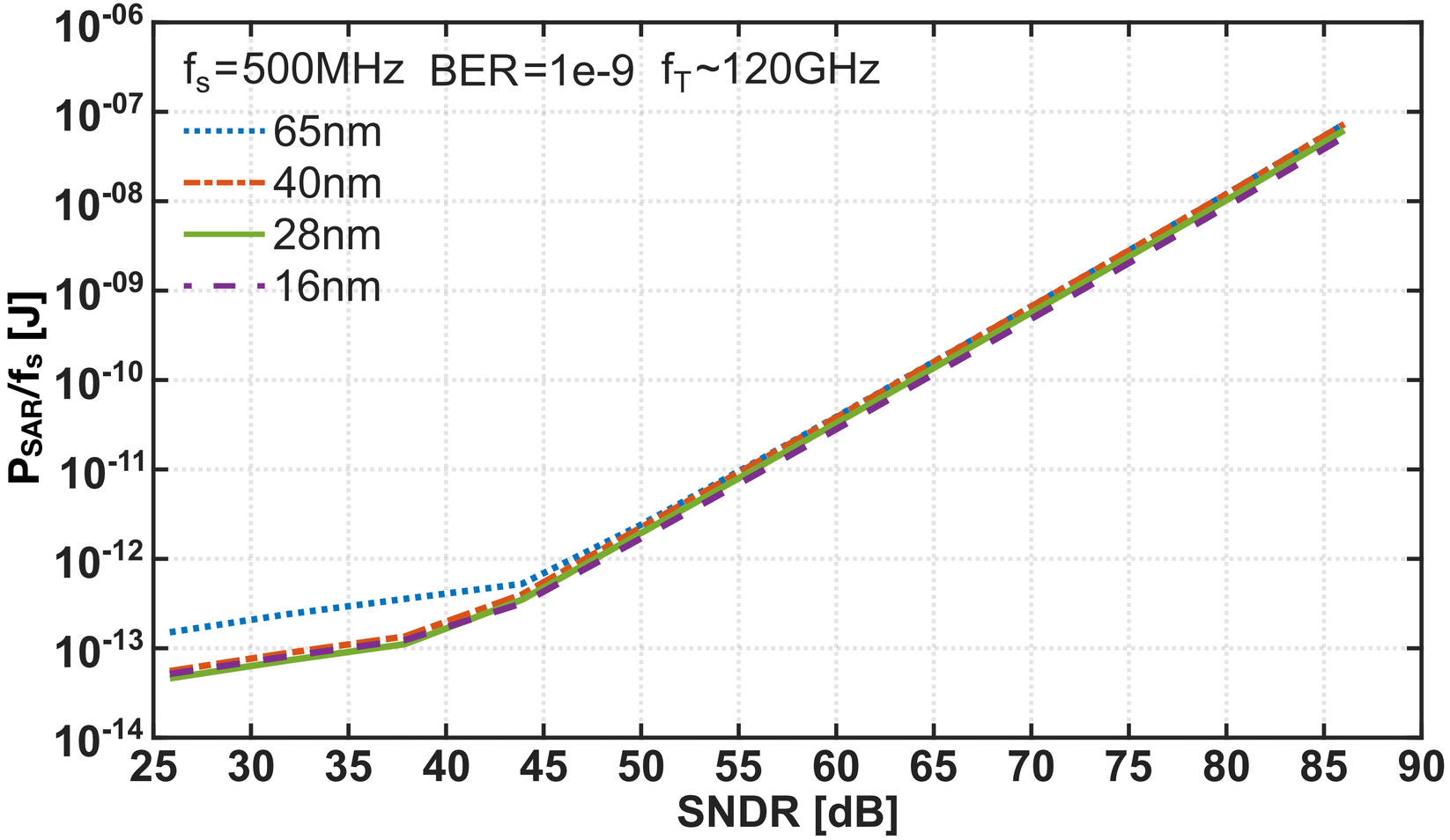
- $P_{\mathrm{SA,samp}}$ and $P_{\mathrm{SA,comp}}$ same as with flash ADC
  - Sample period divided in time for sampler and B times time for comparator
    ex.: $\theta_{\mathrm{SA,samp}} = \theta_{\mathrm{SA,comp}} = B + 1$ for equal duration of sampler time and comparator cycles
  - Thermal noise partitioning between sampler and comparator
- $P_{\mathrm{SA,DAC}} = \dfrac{E_{\mathrm{MCS}} \cdot f_{\mathrm{s}}}{\eta_{\mathrm{reg}}}$ and assuming 50% efficiency
- $P_{\mathrm{SA,dig}} = V_{\mathrm{DD}}^2 \cdot f_{\mathrm{s}} \cdot C_{\mathrm{min}} \cdot \#\mathrm{gates}$ for DAC control, clocking and storing comparator outputs
- Binary SAR with synchronous timing scheme

SAR ADCs at different f_s



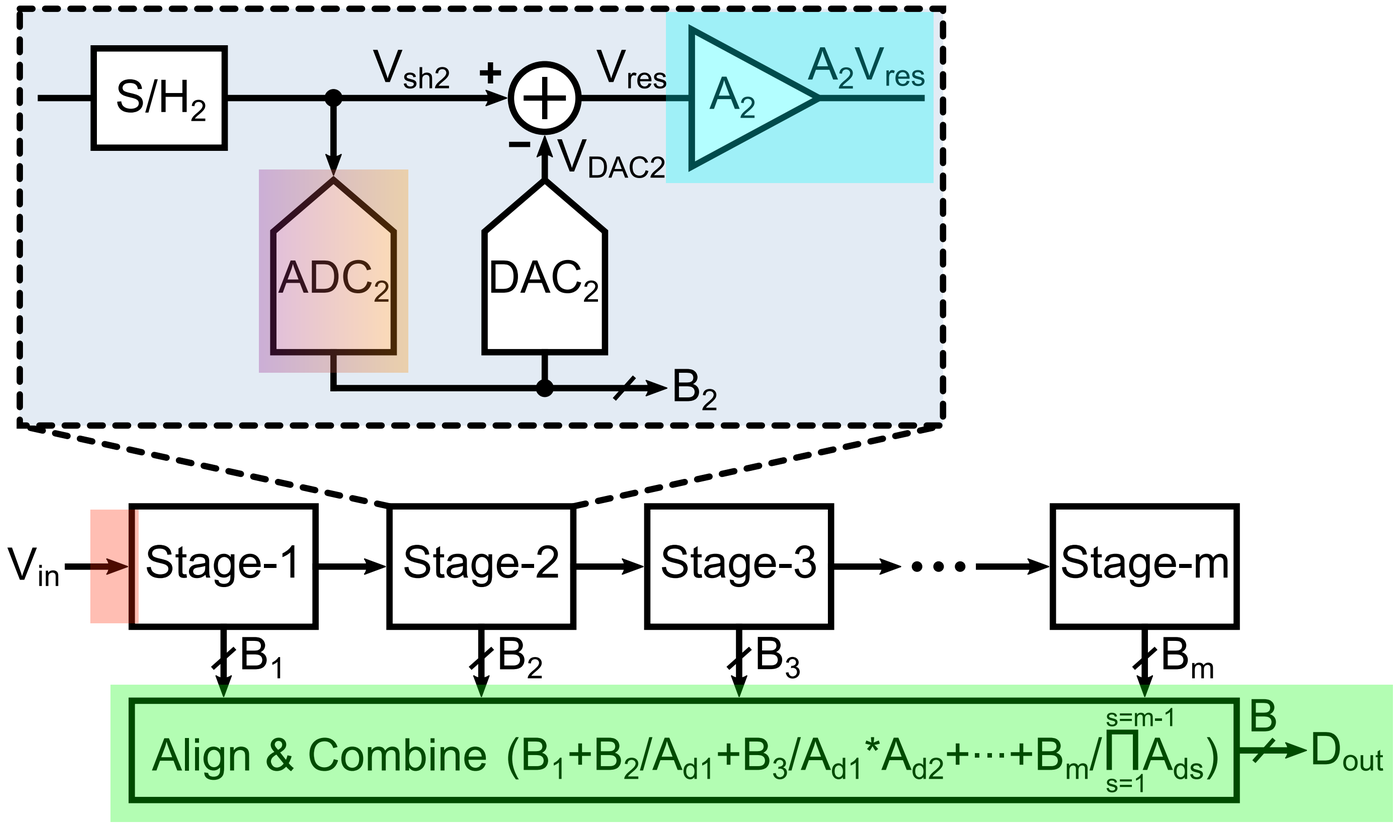
- Similar trends as flash but:
  - Lower power/speed for same accuracy
  - Smaller slope thanks to linear increase of power with B
- For high f_s/f_T, slope becomes steeper due to short internal cycle time

Scaling of SAR ADCs



- Scaling helps in process-limited region dictated by C_{min}
- Scaling does only marginally help in noise-limited region

B-bit m-stage pipeline ADC



- Speed limited by speed of sub-flash ADC + residue amplifier → popular high-speed architecture
- Similar binary search as SAR but without hardware reuse
- Performance (power, speed, linearity, noise) mainly limited by residue amplifiers

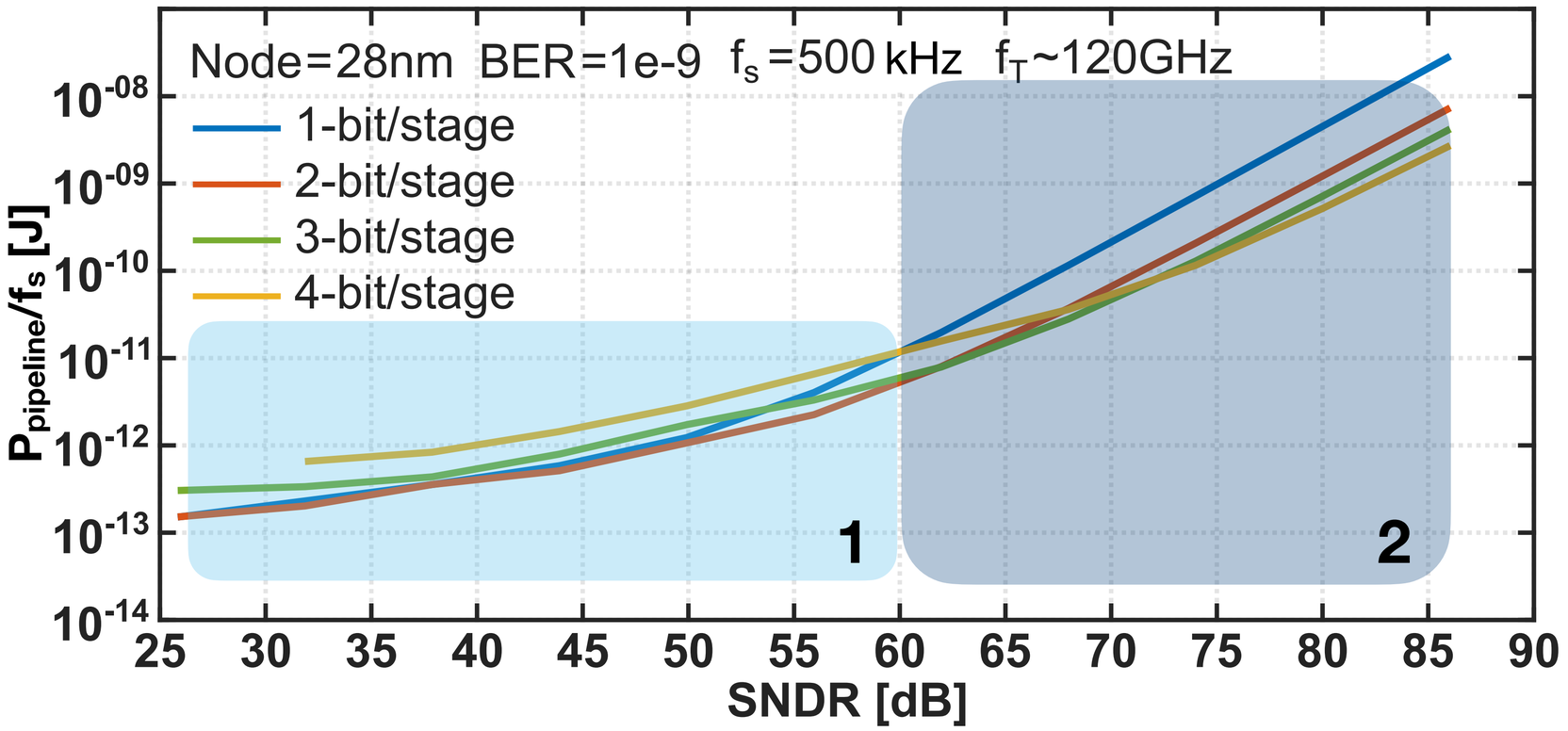
$$P_{\mathrm{P,tot}} = P_{\mathrm{P,samp}} + \sum_{i=1}^{m} \left(\left(2^{B_s} - 1\right) \cdot P_{\mathrm{P,comp},i} + P_{\mathrm{P,lad},i} + P_{\mathrm{P,RA},i} \right) + P_{\mathrm{P,dig}}$$

Pipeline ADC power consumption

$$P_{\mathrm{P,tot}} = P_{\mathrm{P,samp}} + \sum_{i=1}^{m} \left(\left(2^{B_{\mathrm{s}}} - 1\right) \cdot P_{\mathrm{P,comp},i} + P_{\mathrm{P,lad},i} + P_{\mathrm{P,RA},i} \right) + P_{\mathrm{P,dig}}$$

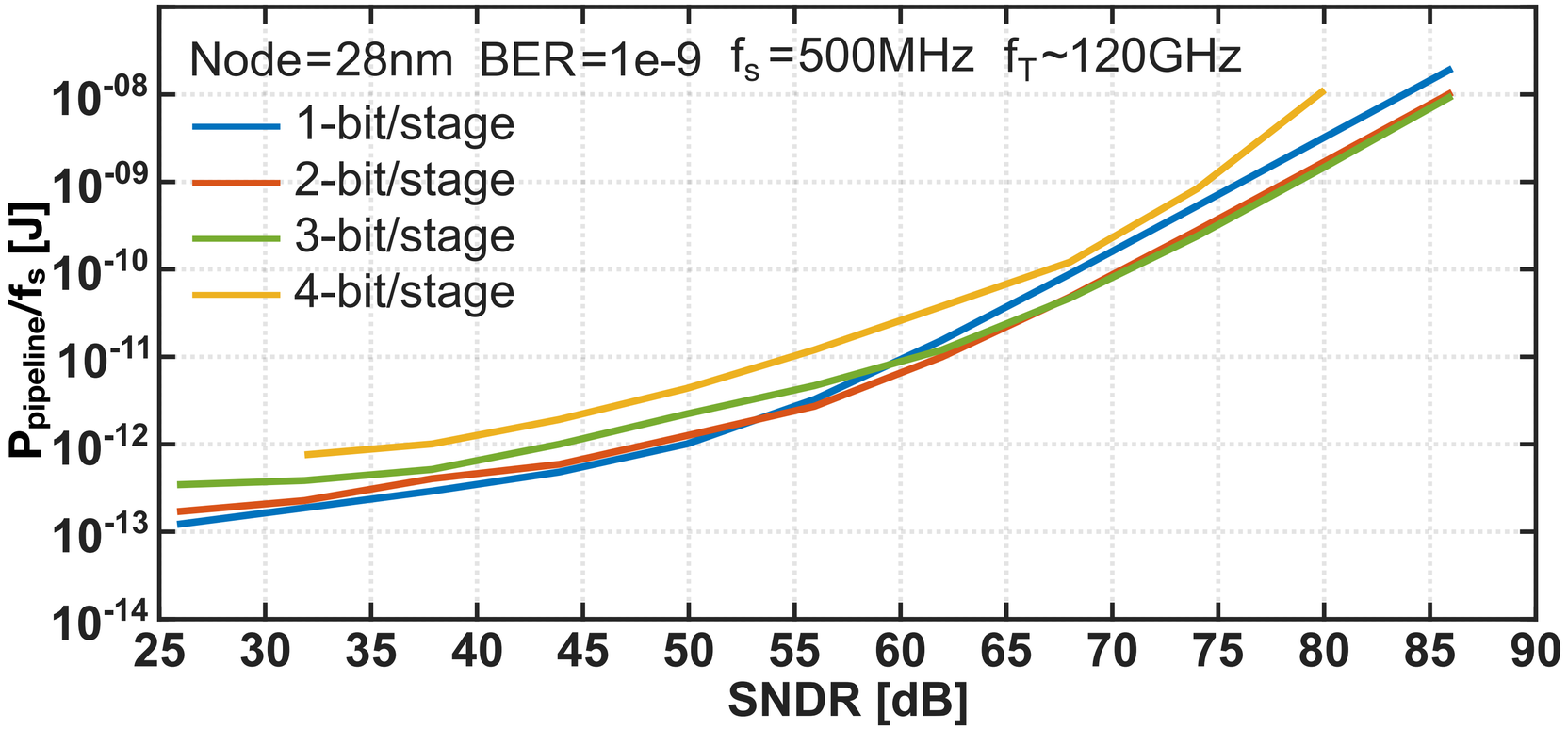
- $P_{\mathrm{P,samp}}$ same as for flash and SAR
- Gain in pipeline allows to scale down $P_{\mathrm{P,comp},i}$, $P_{\mathrm{P,lad},i}$ and $P_{\mathrm{P,RA},i}$ with i
  - More bit/stage result in more aggressive scaling
  - Scaling ultimately stops when C_{min} is reached
  - Comparator can have higher noise, amplifier can have higher noise, less linearity and reduced accuracy
- $P_{\mathrm{P,dig}} = V_{\mathrm{DD}}^2 \cdot f_{\mathrm{s}} \cdot C_{\mathrm{min}} \cdot \#\mathrm{gates}$

Pipeline ADCs at low f_s



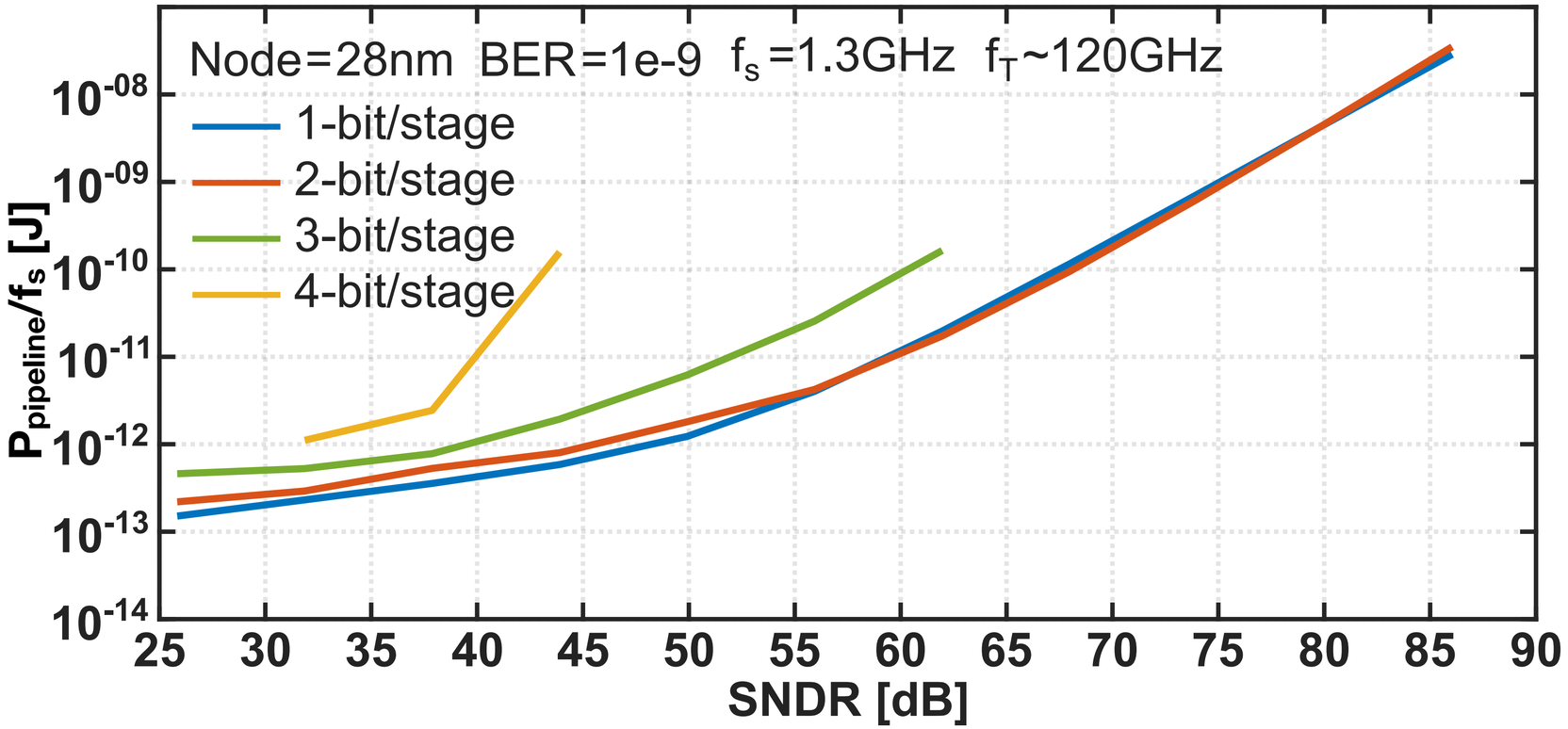
- Two regions:
  1. **SNDR ≤ 60 dB**
     Fewer bit/stage results in lower power/speed
  2. **SNDR > 60 dB**
     More bit/stage results in lower power/speed
- Steeper slope in second region due to exponential increase of sub-flash

Pipeline ADCs at medium f_s



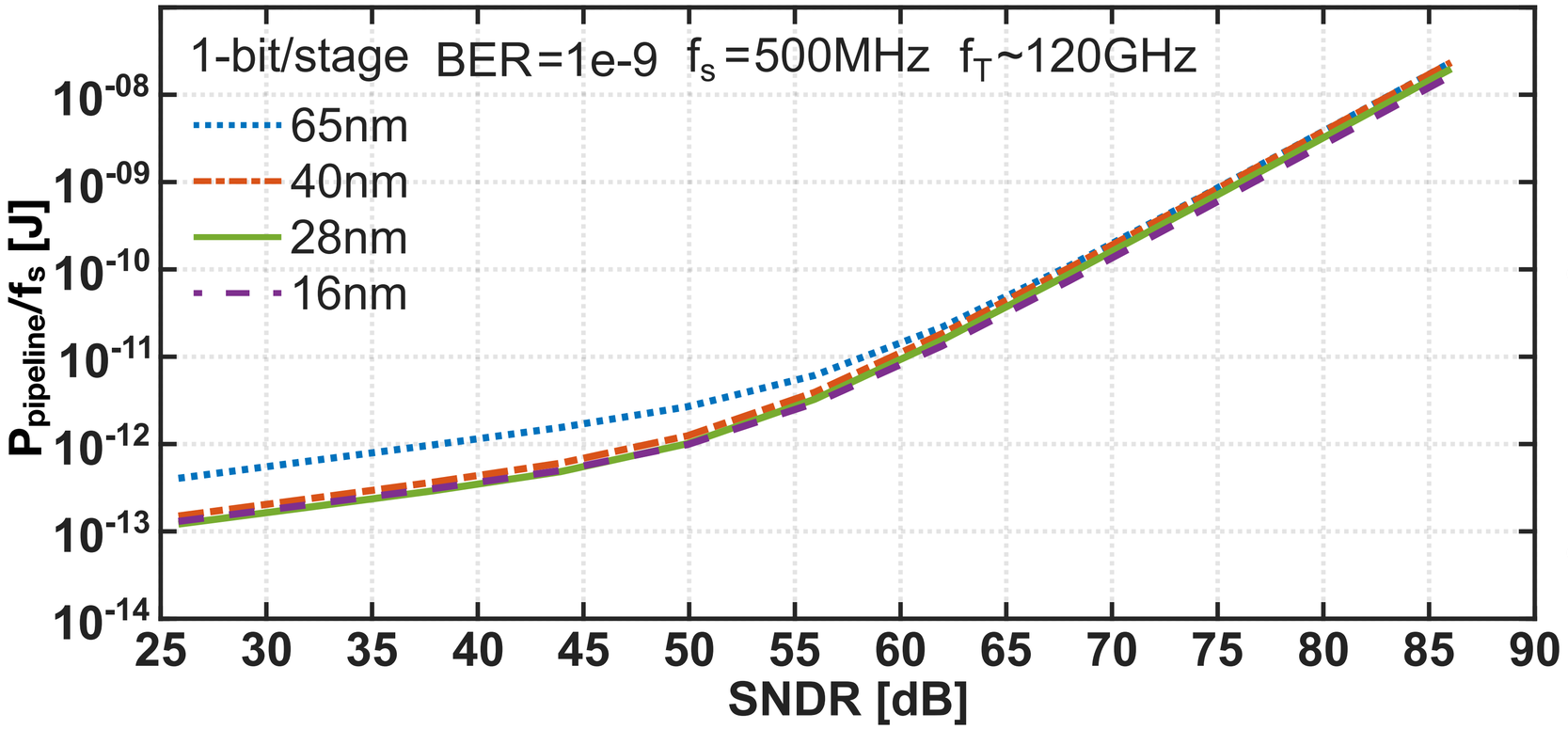
- 4-bit/stage never optimal
- 3-bit/stage still best at high SNDR
- 1 or 2-bit/stage best at low SNDR

Pipeline ADCs at high f_s



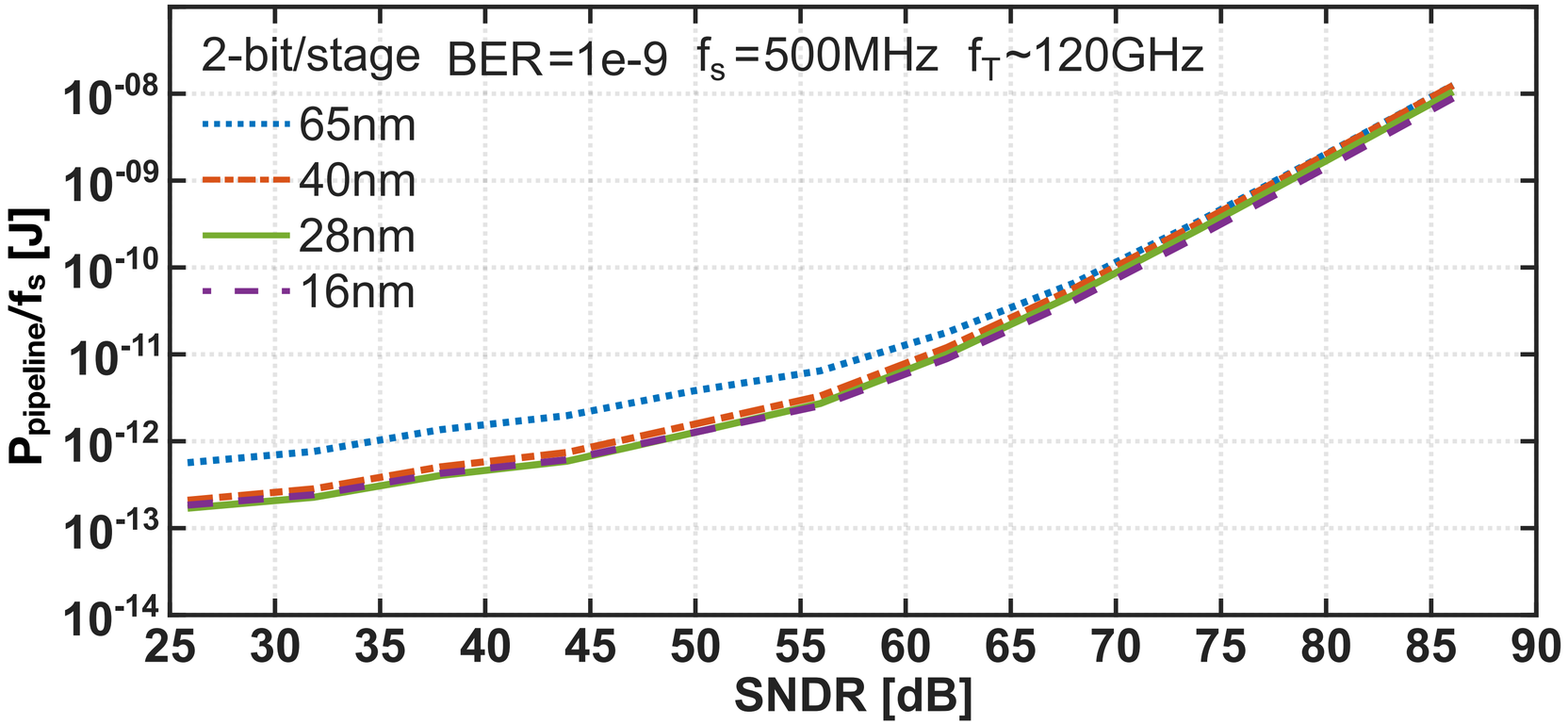
- Ongoing trend of fewer bit/stage for minimal power/speed
- High gain and settling requirements for residue amplifier are imposing the limit
- 1-bit/stage is best for high-speed and high SNDR

Scaling of 1-bit/stage pipeline ADCs



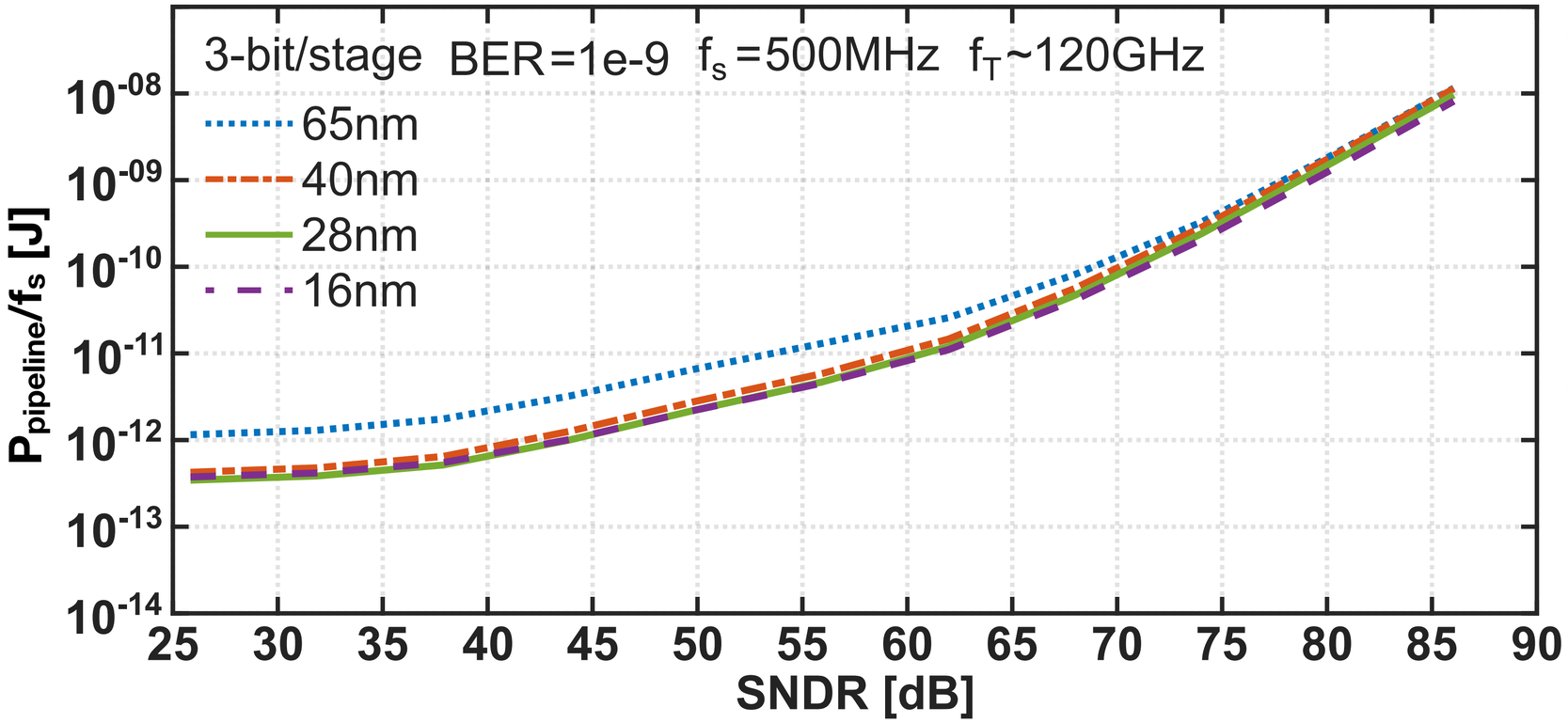
- Same trend as flash and SAR in process-limited region
- Noise-limited region similar to flash due to sub-flash stages
- No scaling benefit in noise-limited region

Scaling of 2-bit/stage pipeline ADCs



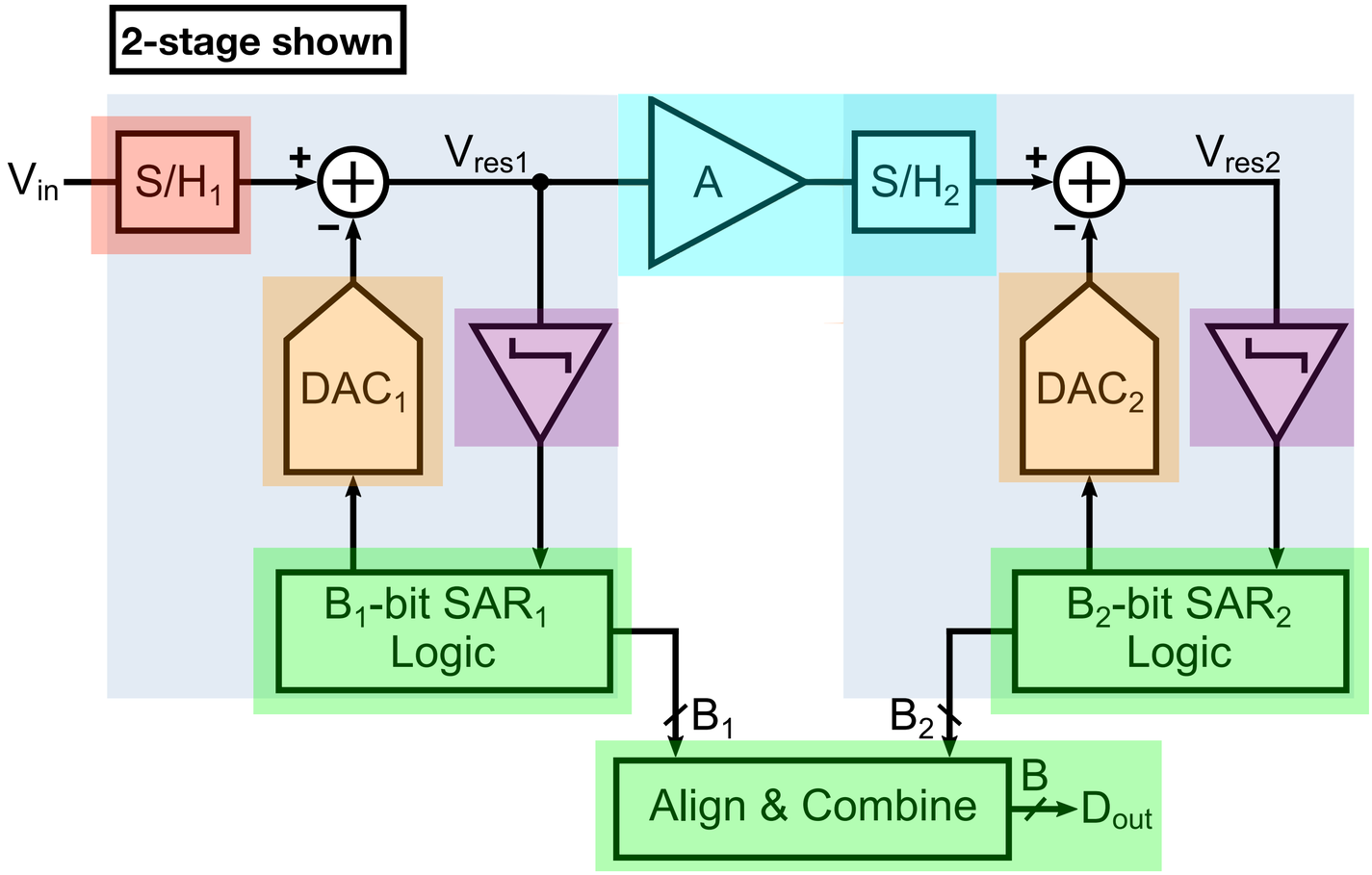
- Process-limited region shifted towards higher SNDR
- More aggressive stage-scaling results in hitting C_{min}-limit earlier in the pipeline

Scaling of 3-bit/stage pipeline ADCs



- Process-limited region shifted towards even higher SNDR
- Higher power due to exponentially increasing sub-flash C_{min}

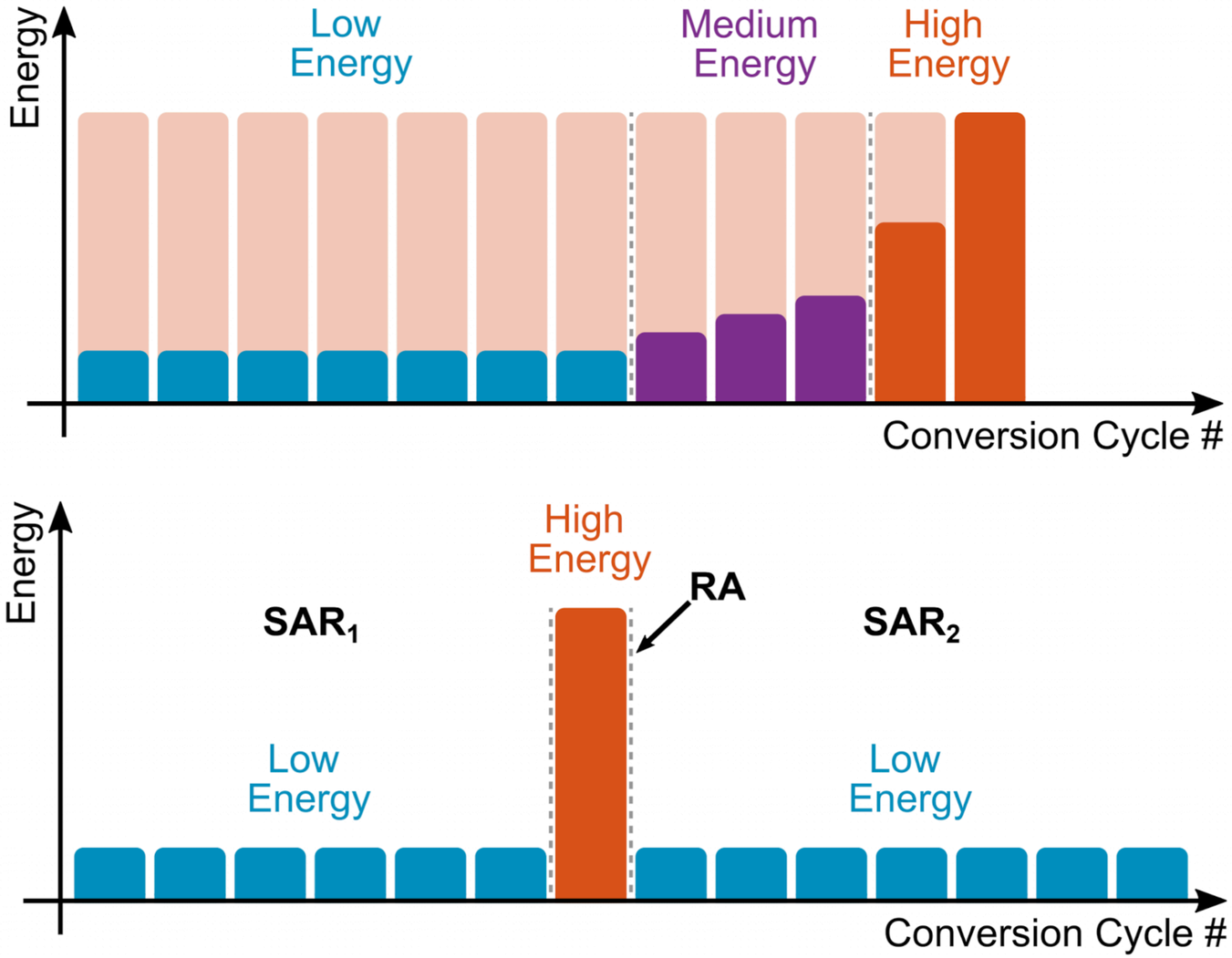
B-bit m-stage pipelined-SAR ADC



- Hybrid ADC architecture
- Same as pipeline with sub-SAR instead of sub-flash stages
- SAR is more efficient than flash
- (Open-loop) amplifier typically merged with subsequent S/H

$$P_{\mathrm{PS,tot}} = P_{\mathrm{PS,samp}} + \sum_{i=1}^{m} \left(P_{\mathrm{PS,comp},i} + P_{\mathrm{PS,DAC},i} + P_{\mathrm{PS,RA},i} + P_{\mathrm{PS,dig},i} \right) + P_{\mathrm{PS,dig}}$$

Pipelined-SAR ADC advantage



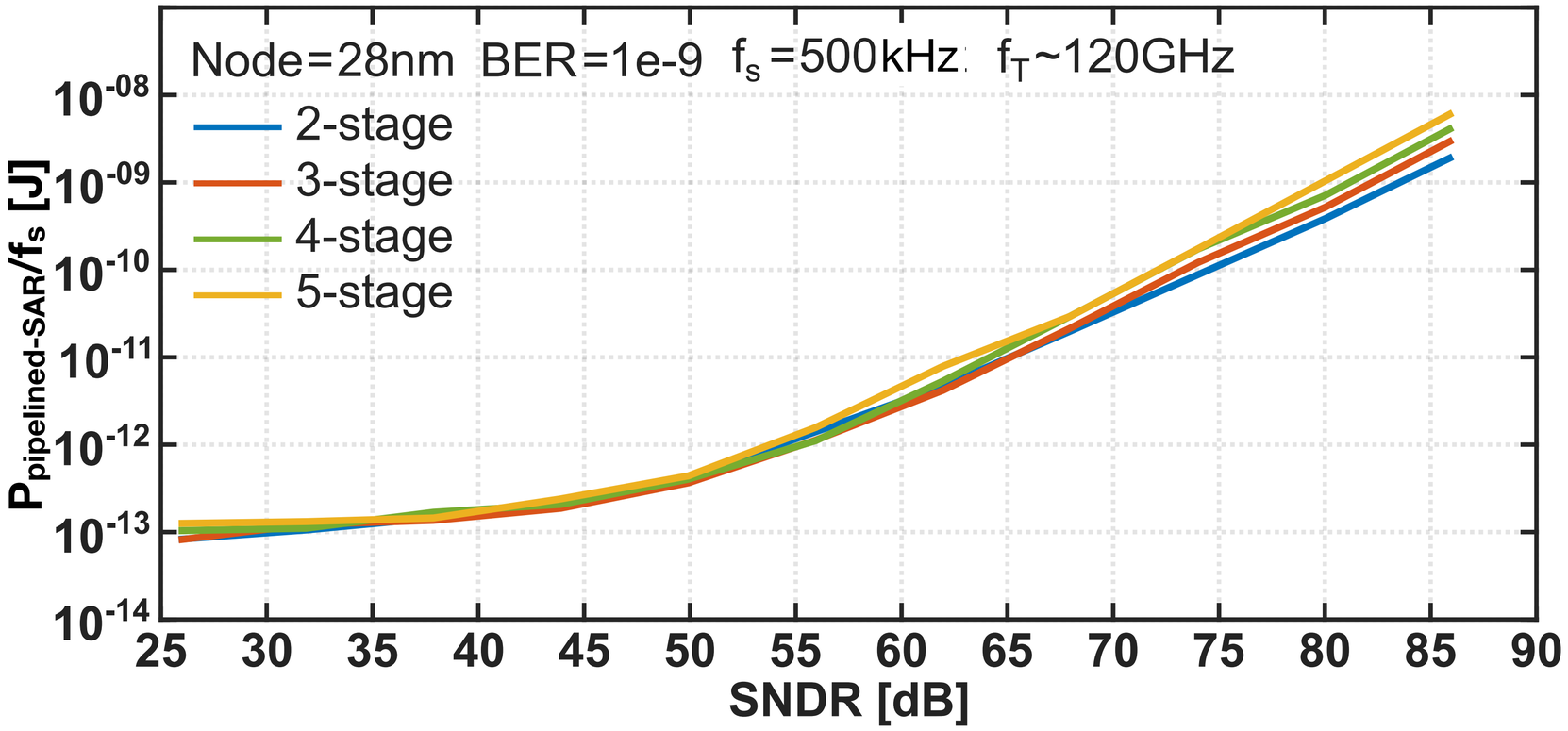
- Typically two extra cycles required compared to SAR:
  - One cycle for the amplifier
  - One cycle for redundancy between the stages
- Energy waste of SAR avoided in pipelined-SAR
  - Comparator can have higher noise
  - Only amplifier determines power

Pipelined-SAR ADC power consumption

$$P_{\mathrm{PS,tot}} = P_{\mathrm{PS,samp}} + \sum_{i=1}^{m} \left(P_{\mathrm{PS,comp},i} + P_{\mathrm{PS,DAC},i} + P_{\mathrm{PS,RA},i} + P_{\mathrm{PS,dig},i} \right) + P_{\mathrm{PS,dig}}$$

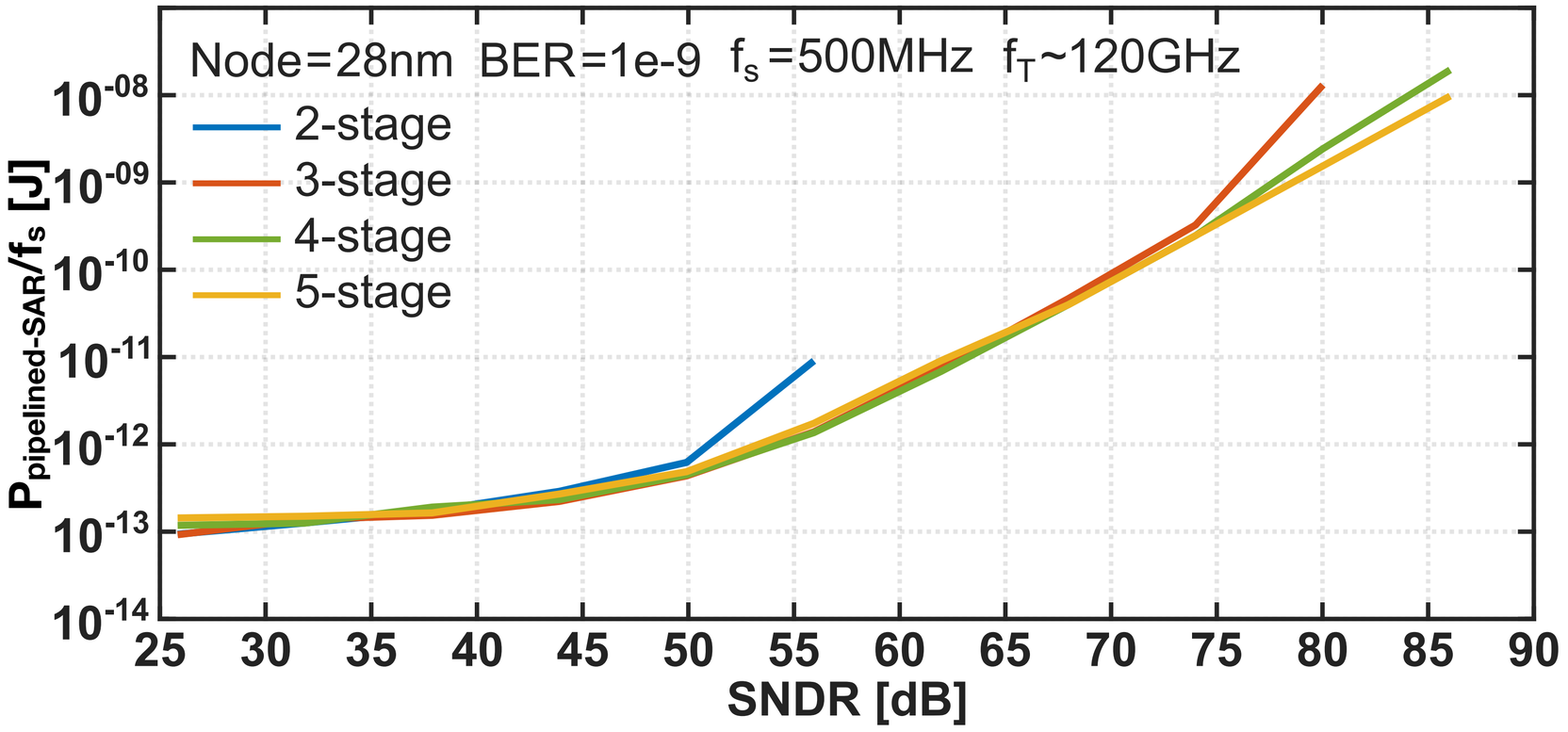
- $P_{\mathrm{PS,samp}}$ same as for flash, SAR and pipeline
- Gain in pipeline allows to scale down $P_{\mathrm{PS,comp},i}$, $P_{\mathrm{PS,DAC},i}$ and $P_{\mathrm{PS,RA},i}$ with i
  - Typically more aggressive scaling thanks to more bit/stage than pipeline
  - Amplifier needs to share its timing with the sub-SAR and needs to provide a lot of gain
  - Scaling ultimately stops when C_{min} is reached
- $P_{\mathrm{PS,dig},i}$ same as in regular SAR, $P_{\mathrm{PS,dig}}$ same is in regular pipeline

Pipelined-SAR ADCs at low f_s



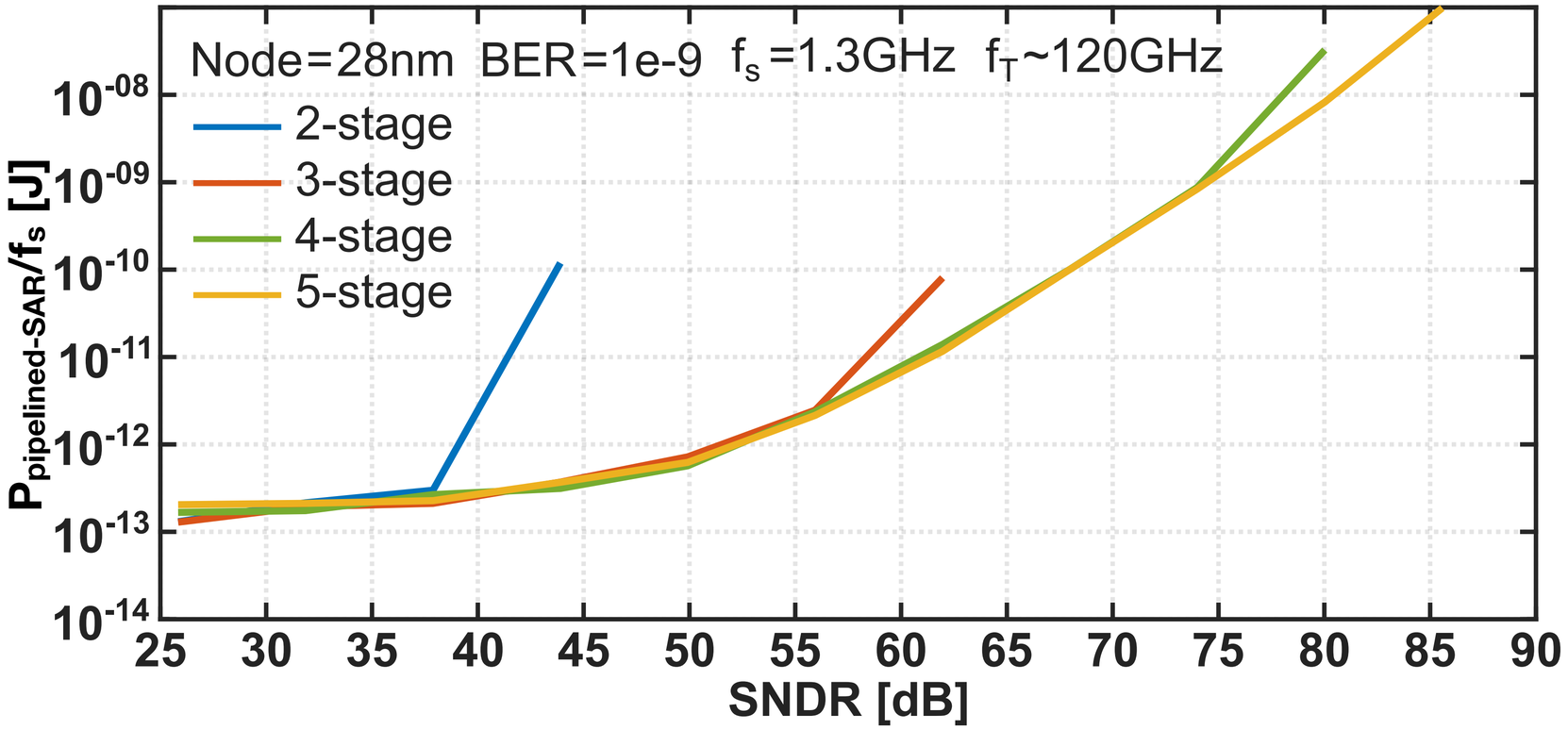
- More stages is marginally better at low SNDR
- Less stages is better at high SNDR in noise-limited region
- Fewer stages:
  - Increased amplifier gain
  - Relaxed settling

Pipelined-SAR ADCs at medium f_s



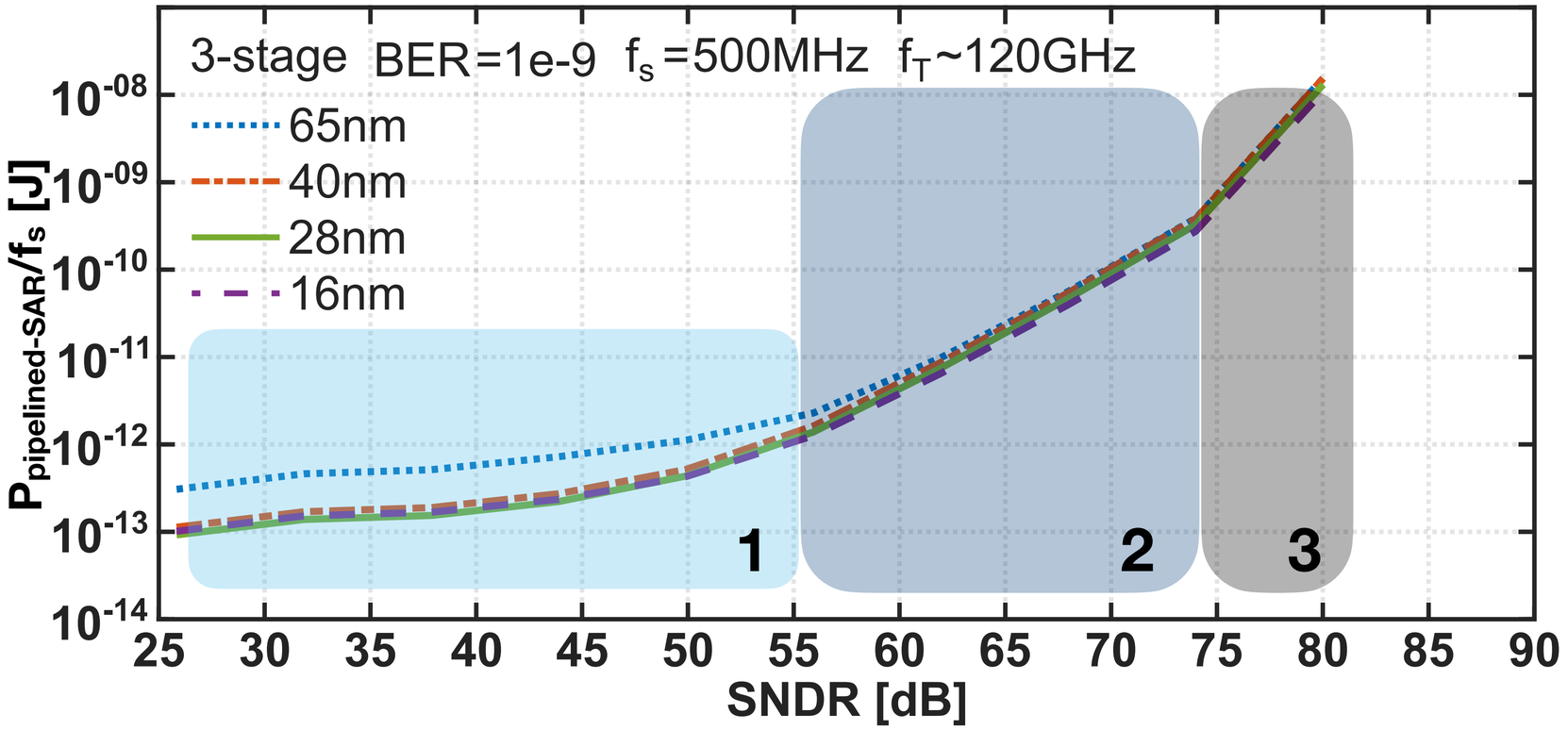
- Same trend as in pipeline
- More stages is better due to:
  - Longer sub-ADC times
  - Less stringent amplifier specifications
- 2-stage stops at 55 dB due to too high f_s/f_T

Pipelined-SAR ADCs at high f_s



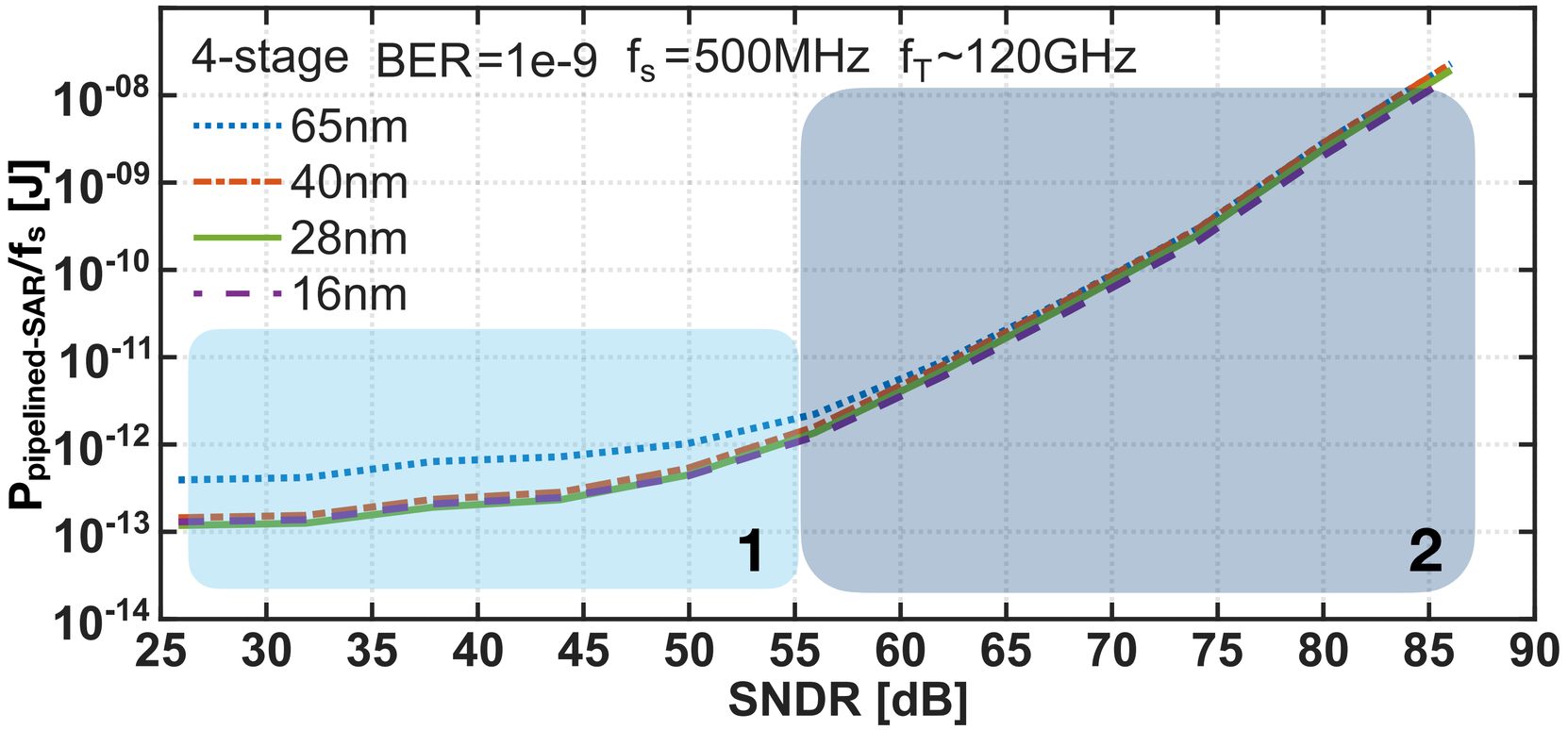
- Trend towards more stages continuous
- > 5 stages can be considered at high SNDR

Scaling of 3-stage pipelined-SAR ADCs



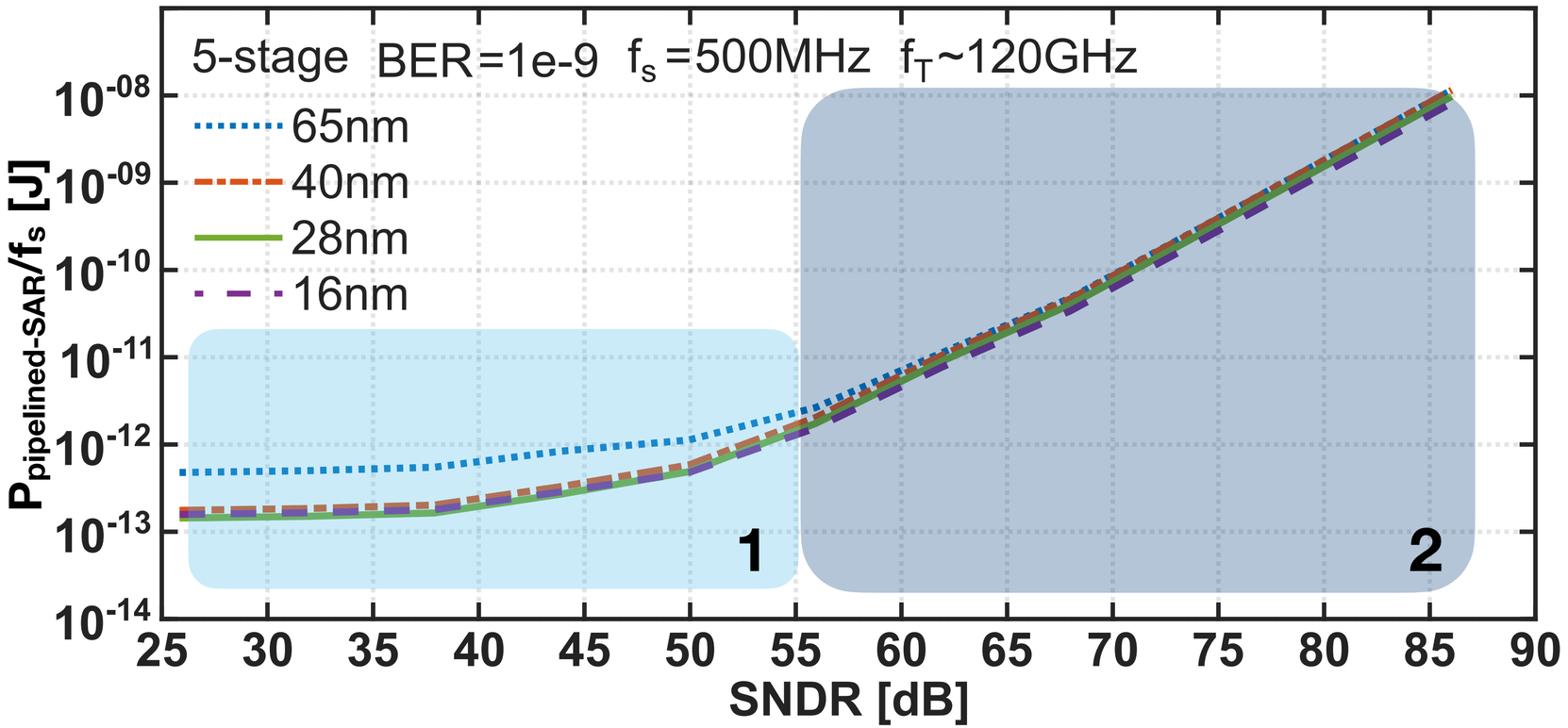
- Process-limited region (1) extended towards higher SNDR
  → scaling helps more
- Same slope as SAR in noise-limited region (2) due to sub-SAR stages
- Steeper slope at highest SNDR (3) due to high f_s/f_T

Scaling of 4-stage pipelined-SAR ADCs



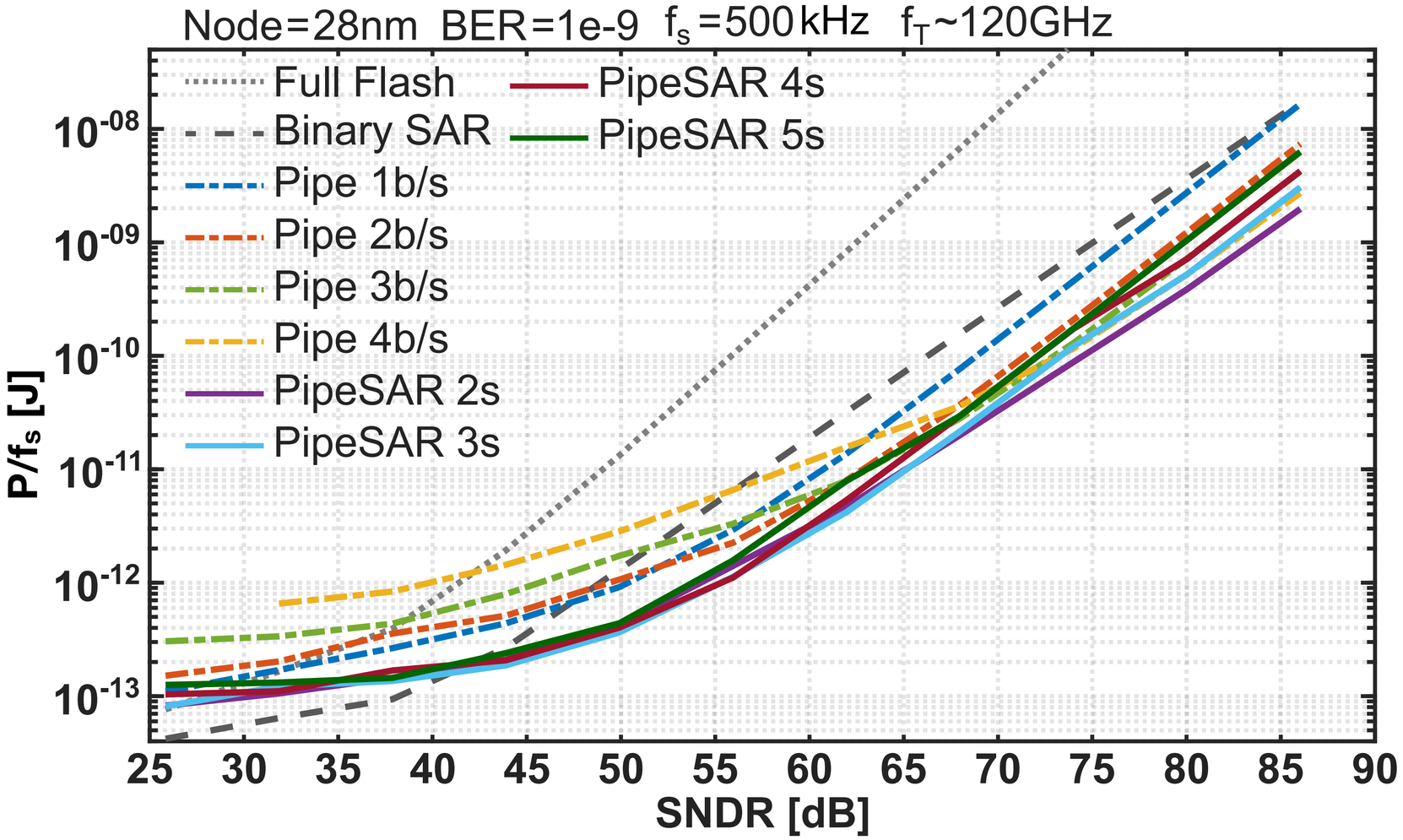
- Relatively stable cross-over between process- and noise-limited regions
- No steep third region visible thanks to more time available per stage

Scaling of 5-stage pipelined-SAR ADCs



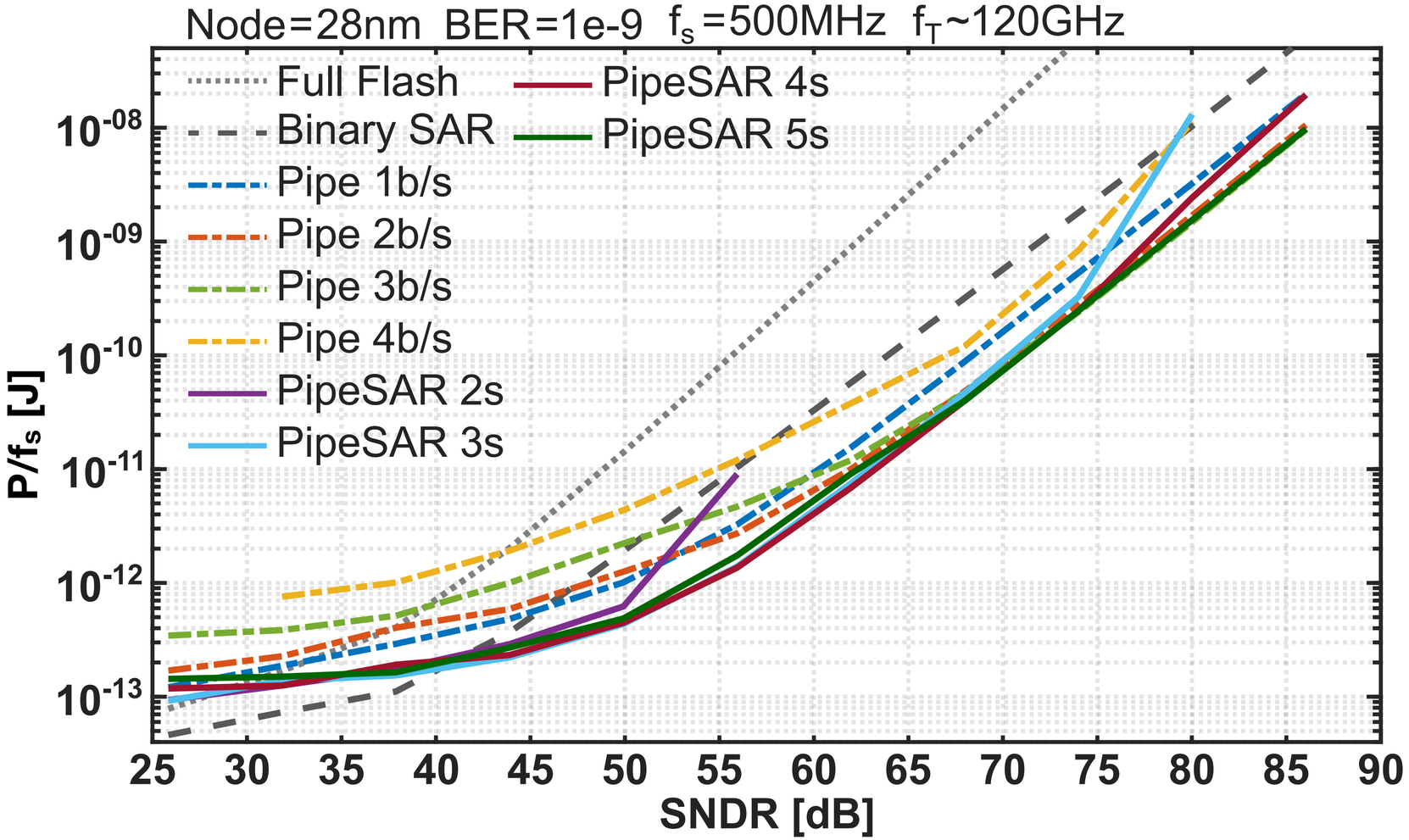
- Relatively stable cross-over between process- and noise-limited regions
- No steep third region visible thanks to more time available per stage
- Main advantage at high SNDR

Performance comparison at low f_s



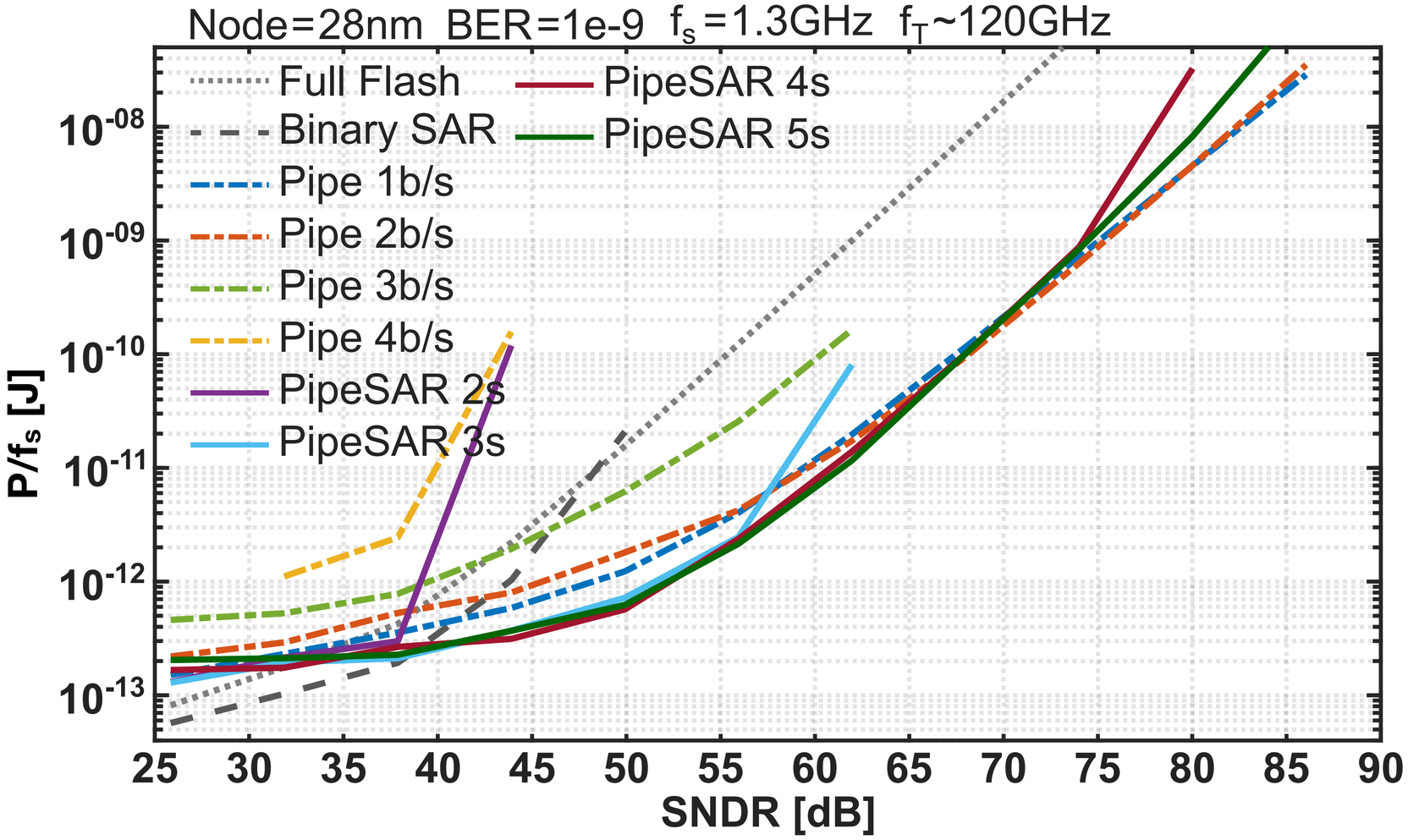
- **SNDR ≤ 40 dB**
  SAR ADC is best
- **40 dB < SNDR ≤ 65 dB**
  Pipelined-SAR ADC is best irrespective of number of stages
- **65 dB < SNDR**
  2-stage pipelined-SAR ADC or 4-bit/stage pipeline ADC are superior

Performance comparison at medium f_s



- **SNDR ≤ 40 dB**
  SAR ADC remains best
- **40 dB < SNDR ≤ 65 dB**
  Pipelined-SAR ADC is best irrespective of number of stages
- **65 dB < SNDR**
  5-stage pipelined-SAR ADC or 2-bit/stage pipeline ADC are superior

Performance comparison at high f_s



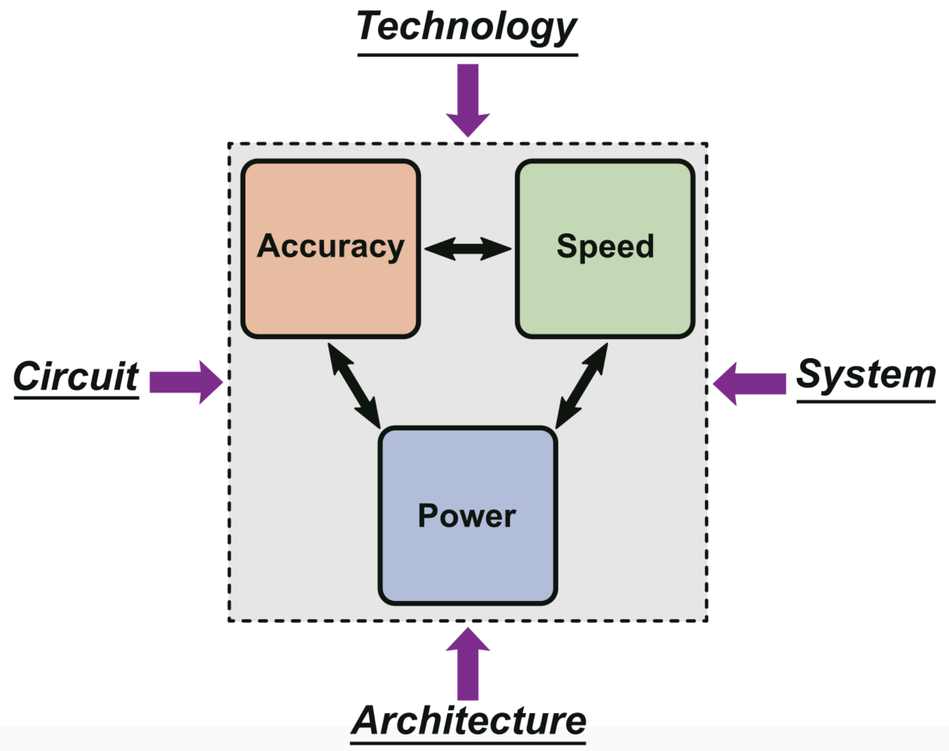
- Steeper slopes for all architectures due to higher f_s/f_T
- 5-stage pipelined-SAR ADC and 1/2-bit/stage pipeline ADC superior at high SNDR
- 1-bit/stage pipeline ADC best at highest SNDR, but many amplifiers and complex!
  → time-interleaving!

Outline

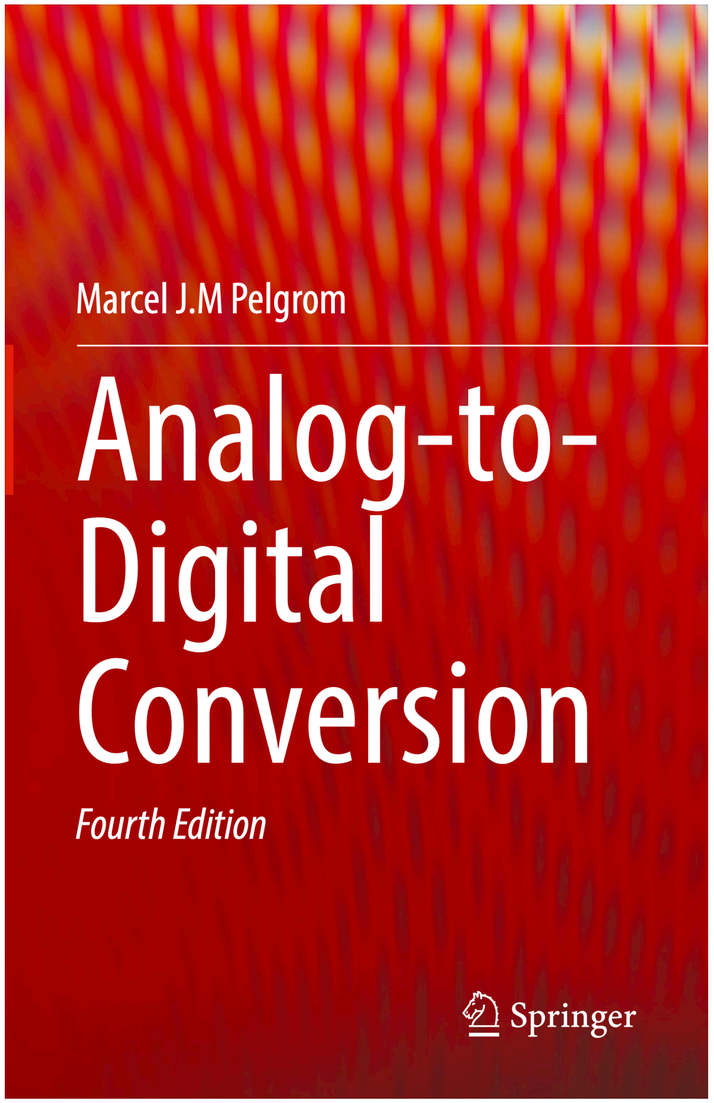
- Introduction
- Principles of Nyquist ADCs
- Limits of Nyquist ADCs
- **Conclusion**

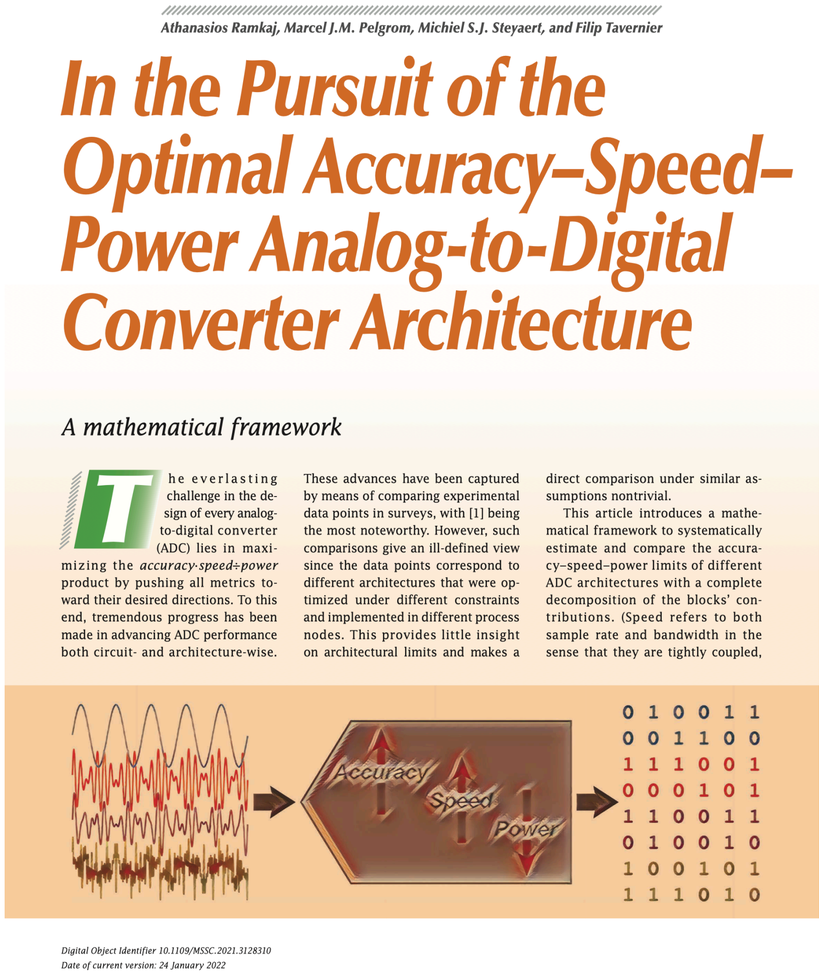
Conclusion

- ADC design is a blend of system, architecture, circuit, and technology
- Understanding the limits at the lower levels, helps making decisions at higher levels
- Higher-level decisions typically impact the ADC performance more significantly
- ADCs will remain the performance limitation in many systems



Reference material





Athanasios Ramkaj, Marcel J.M. Pelgrom, Michiel S.J. Steyaert, and Filip Tavernier

In the Pursuit of the Optimal Accuracy–Speed–Power Analog-to-Digital Converter Architecture

A mathematical framework

The everlasting challenge in the design of every analog-to-digital converter (ADC) lies in maximizing the *accuracy·speed÷power* product by pushing all metrics toward their desired directions. To this end, tremendous progress has been made in advancing ADC performance both circuit- and architecture-wise. These advances have been captured by means of comparing experimental data points in surveys, with [1] being the most noteworthy. However, such comparisons give an ill-defined view since the data points correspond to different architectures that were optimized under different constraints and implemented in different process nodes. This provides little insight on architectural limits and makes a direct comparison under similar assumptions nontrivial.

This article introduces a mathematical framework to systematically estimate and compare the accuracy–speed–power limits of different ADC architectures with a complete decomposition of the blocks' contributions. (Speed refers to both sample rate and bandwidth in the sense that they are tightly coupled,

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