Depleted detectors
Timing detectors

Days of Detection

1st international school on microelectronics for solid-state detectors design, manufacturing and application
October 23 – 25, 2023

Padova

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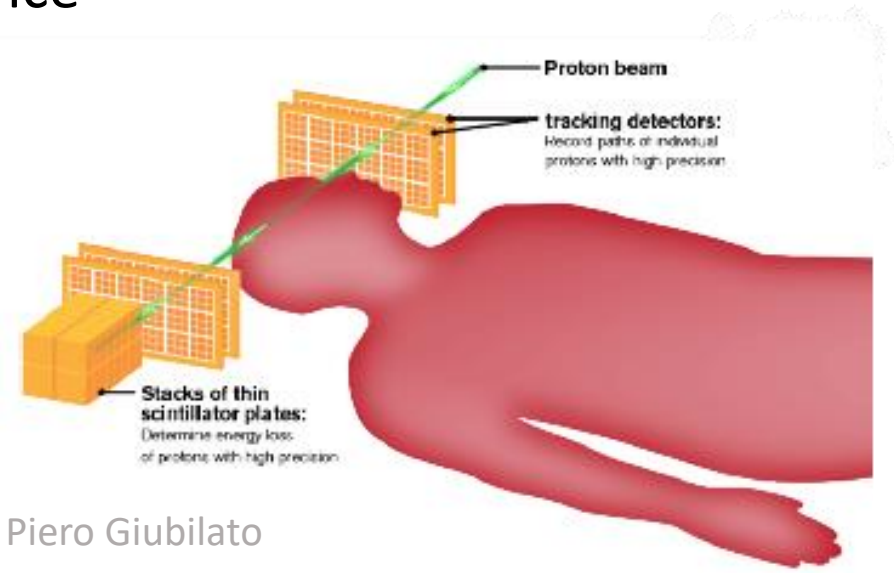
Outline

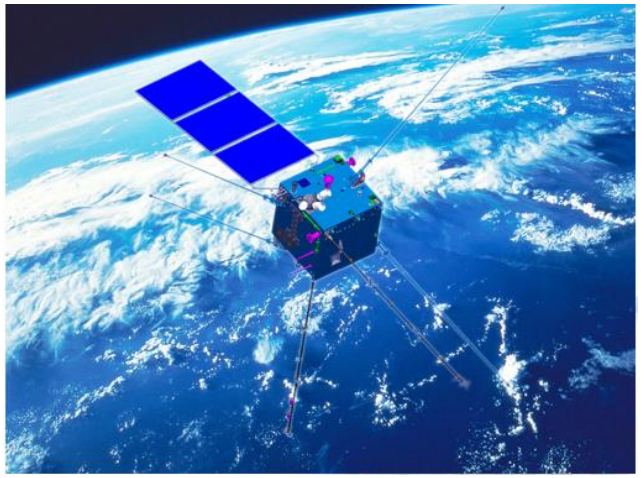
- Introduction
- Overview of CMOS depleted sensors technologies
- Latest developments on silicon sensors for ps timing
- Trends and future perspectives

Silicon depleted sensors for radiation detection

- **Depleted silicon pixel sensors**: large active volume for ionizing particles and X-rays.
- Target **applications**:
  - Tracking and timing in High Energy Physics experiments
  - Medical imaging
  - Astro-particle detection on satellites
  - Material science
  - …



Piero Giubilato



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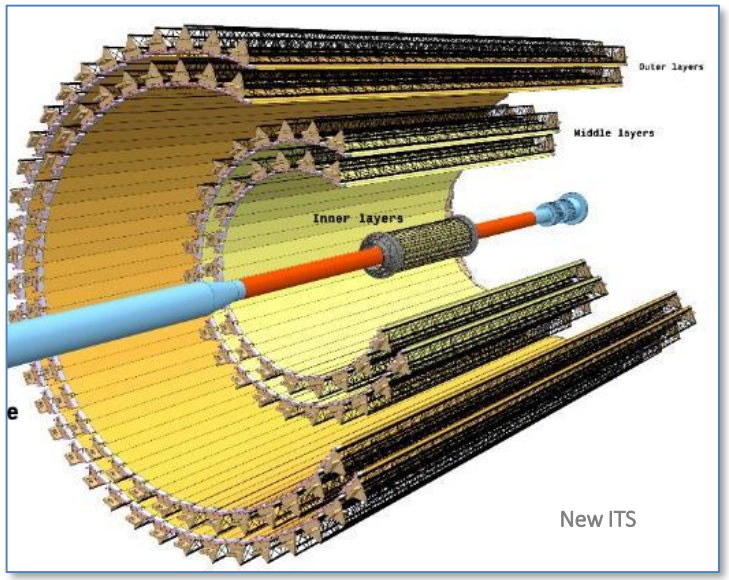
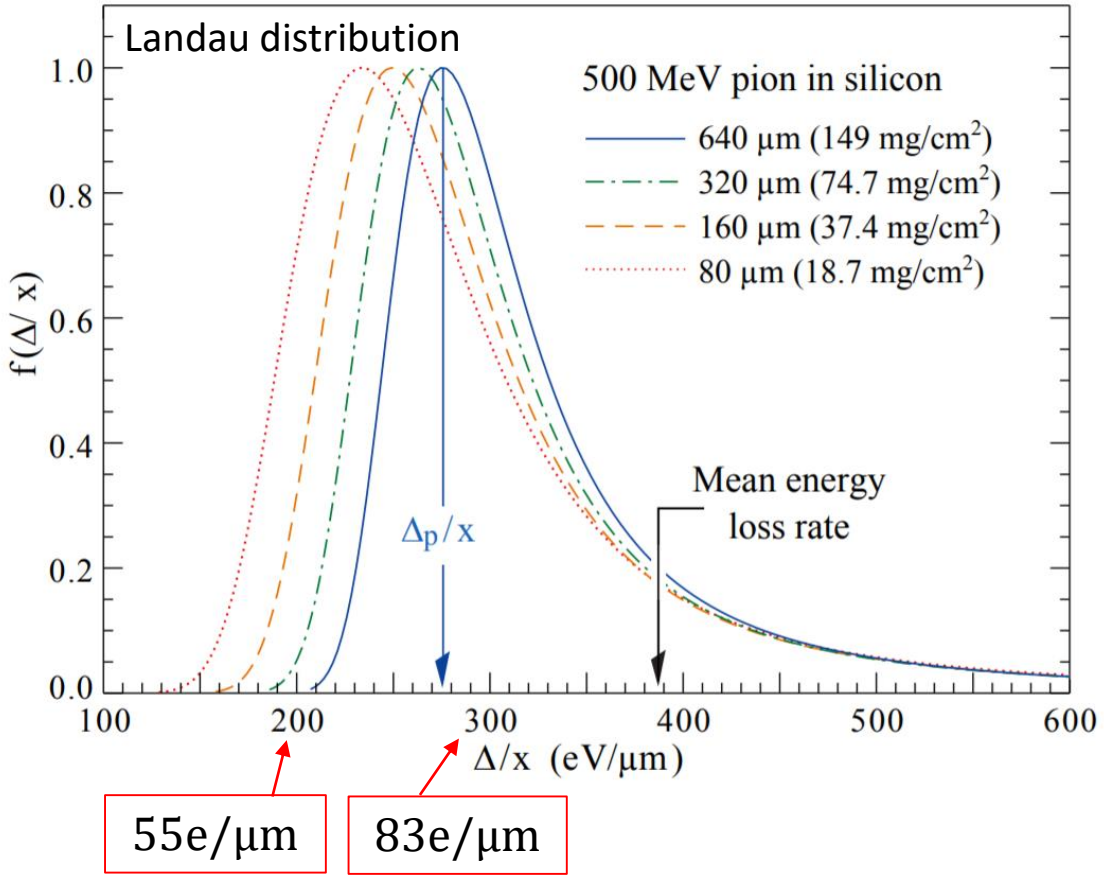
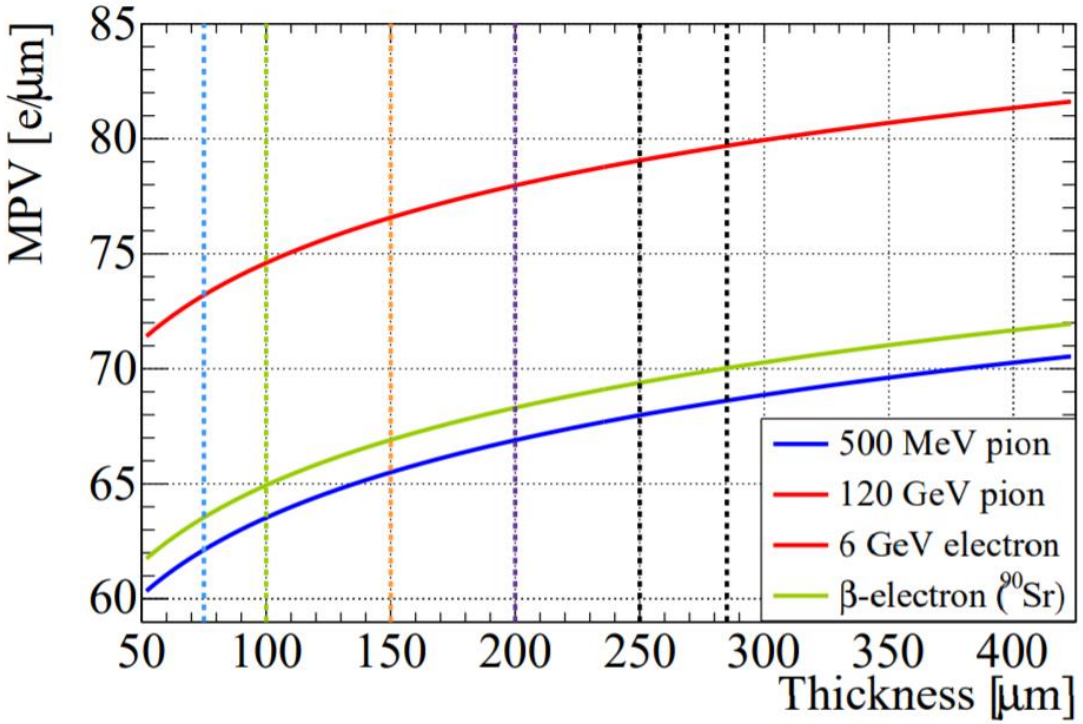


ALICE ITS

Minimum Ionizing particles: energy loss distribution in silicon

- Signal released by M.I.P.s: typically from 60 to 80 $e^-/\mu m$ in Silicon: required detector active thickness increases with electronic noise
- Signal to Noise Ratio determines performance for both tracking and timing applications





S.Terzo, PhD thesis, MPI, 2015

X-rays

EUV, X-rays: “Point-like” interaction with the production of many e-h pairs in a small region, a few μm wide.

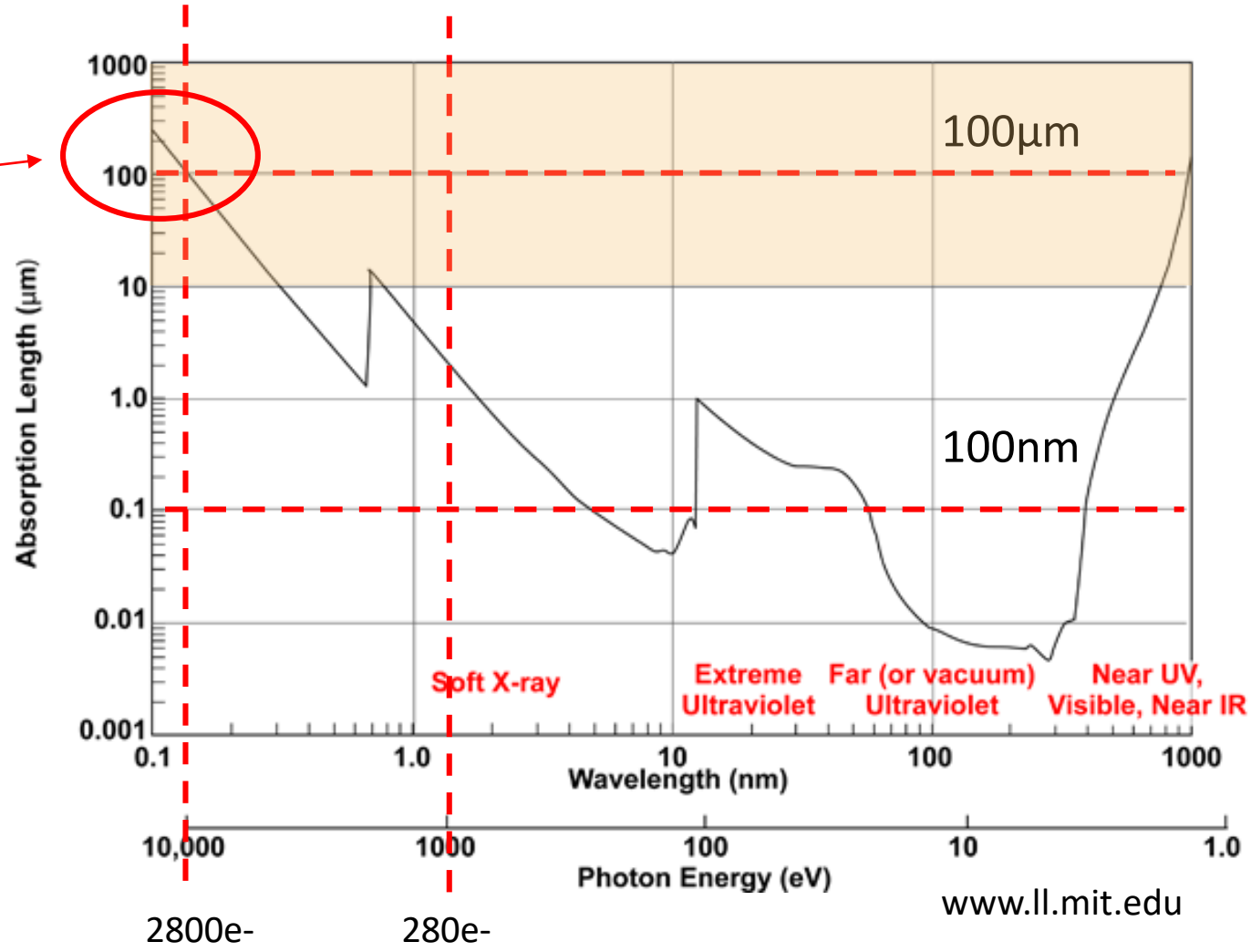
- 100s μm thickness required for efficiency
- Low electronic noise required for charge resolution

Average number of e-h pairs:

$$n_{e-h} = \frac{E_{ph}}{E_{ion}}$$

Si ionization energy

E_{ion}=3.6eV

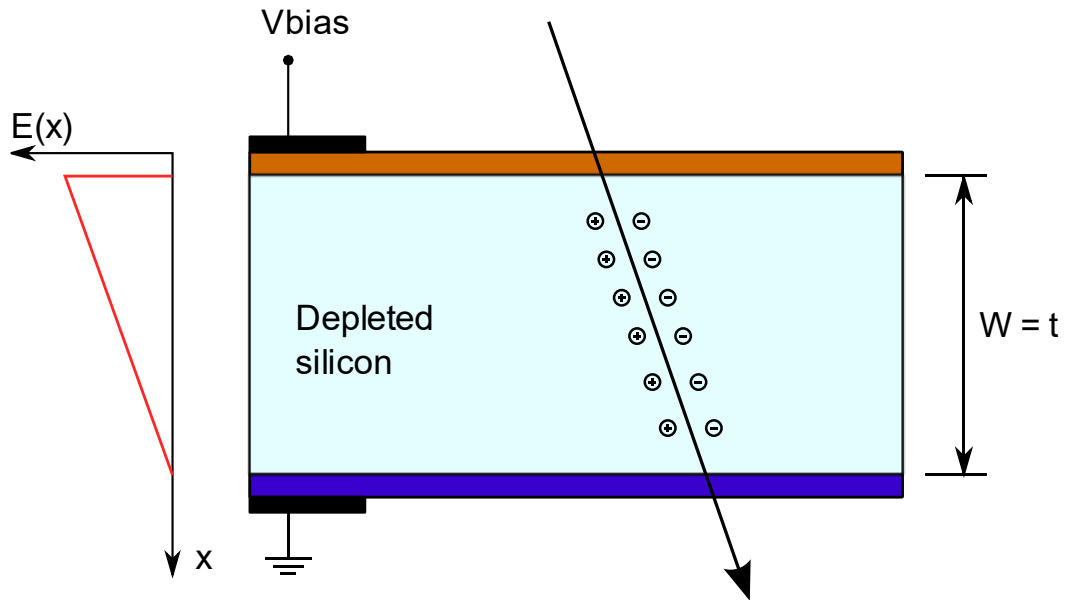


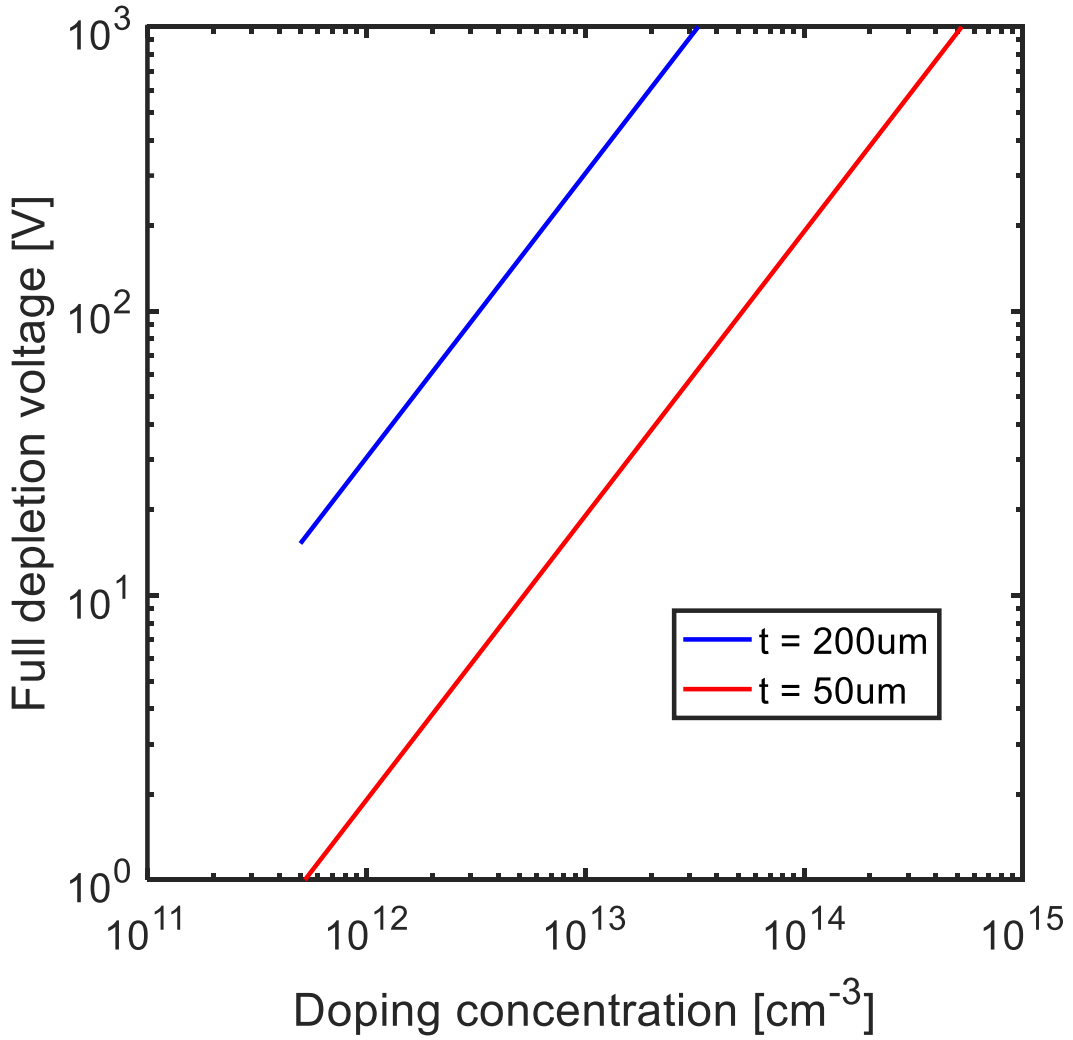
Detector bias

Minimum bias voltage for full depletion:

$$V_{bFD} \cong \frac{qNt^2}{2\epsilon_s}$$

N: detector doping
t: detector thickness

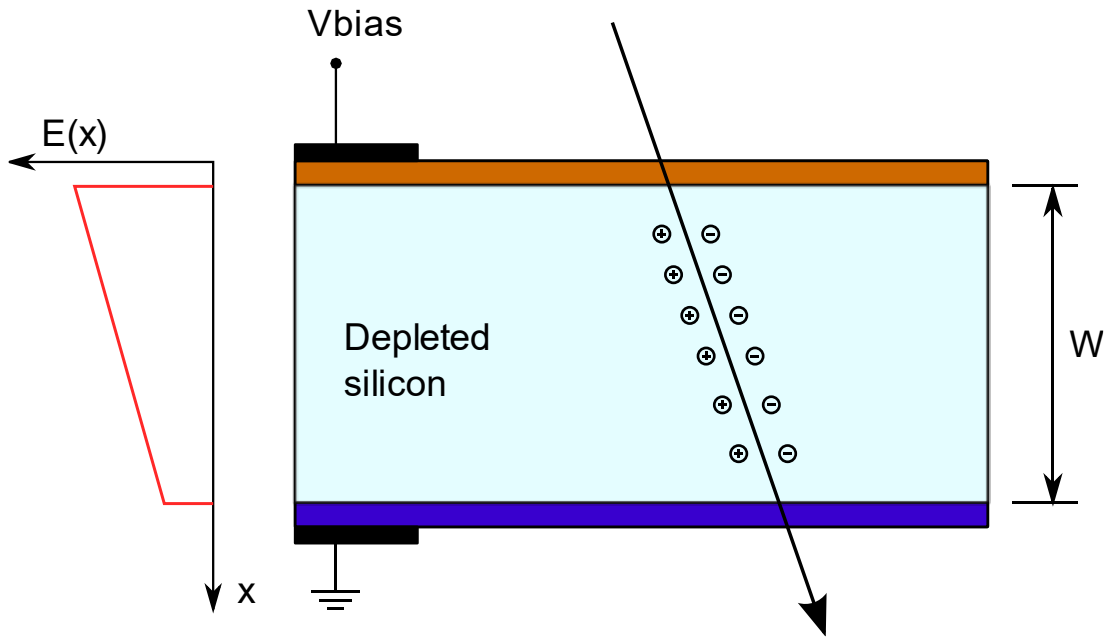


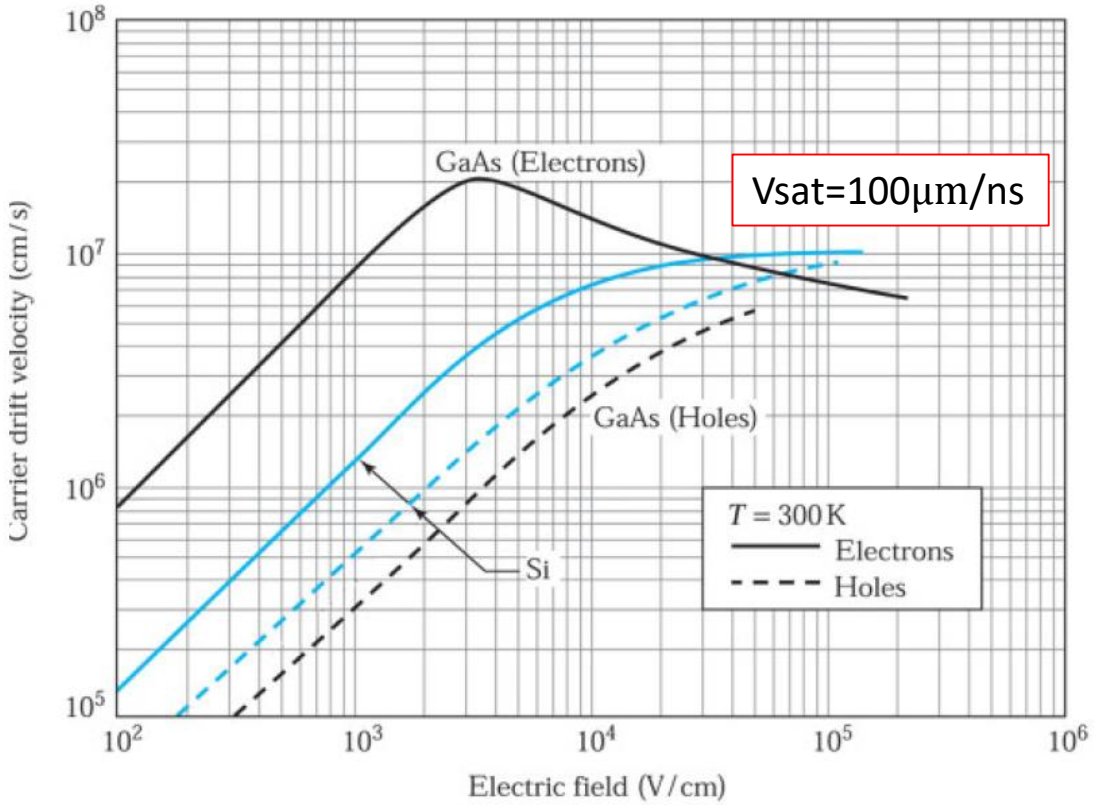


Charge collection: drift

Charge collection by drift required for:

- Timing resolution
- Radiation hardness



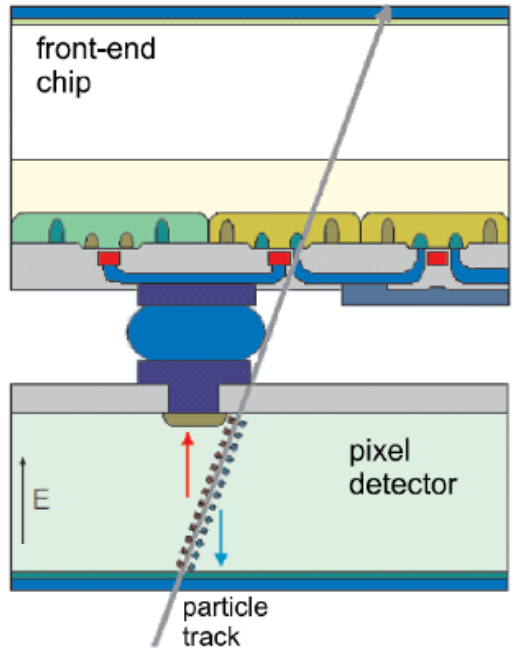


Sze, Semiconductor devices, Wiley & Sons, 2012

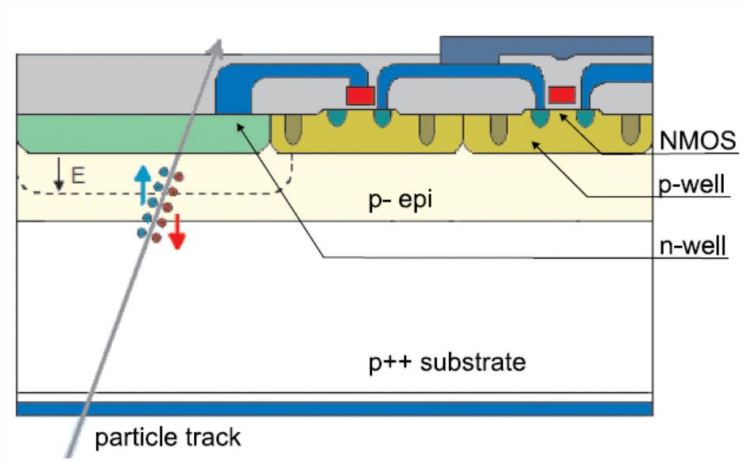
To minimize the charge collection time, the electric field in the detector should be large enough to saturate the charge carrier drift velocity

Hybrid and monolithic pixel sensors

- **Hybrid Pixel Sensors**
  - Detectors and electronics optimized separately
  - Excellent radiation damage tolerance
  - Problems: interconnection stray capacitance (affects SNR) interconnection cost, yield, material budget



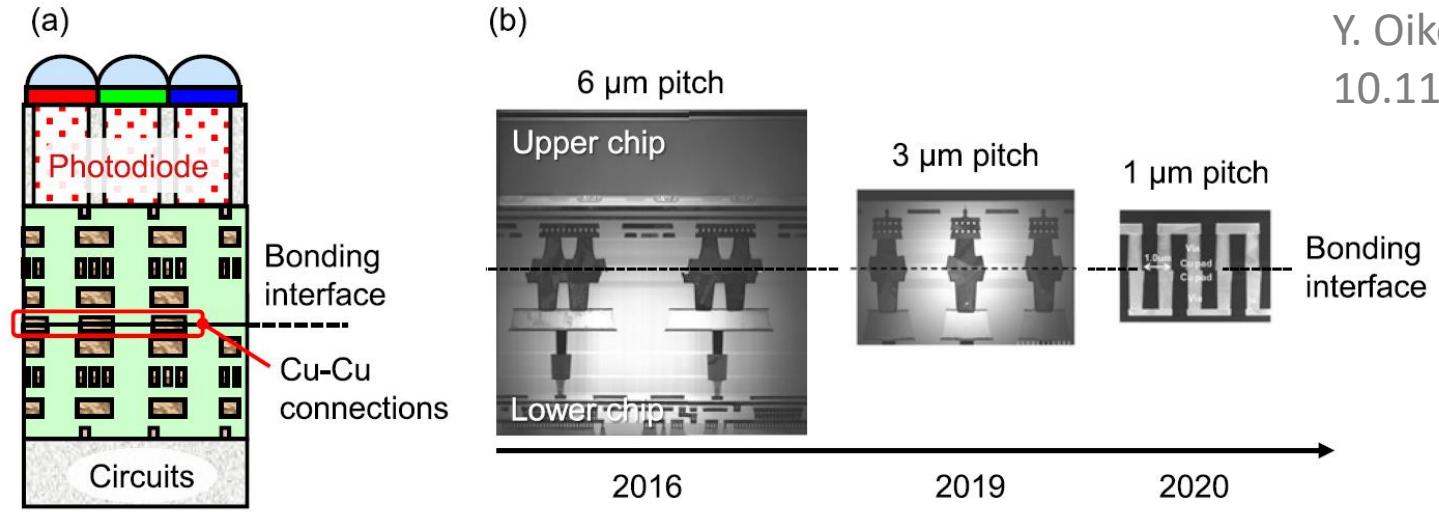
- **Monolithic Active Pixel Sensors (MAPS)**
  - Constraints on the detector optimization: CMOS processes need customization (special substrates, dedicated implants)
  - More freedom with older process nodes (110 to 350nm)
  - Lower capacitance, lower costs, better yield and low material budget



L. Gonella, Particle Physics Seminar, 2017

Hybrid pixel sensors: perspectives

- The situation is changing. Wafer-level **3D stacking** has become an industry standard in the last years: widely adopted in image sensors for the consumer market
- **Accessibility** of 3D integration processes is still a problem for niche applications.



Y. Oike, IEEE TED 2021, doi: 10.1109/TED.2021.3097983

Fig. 8. Trend of Cu–Cu connection pitch. (a) Simplified device structure and (b) cross sections.

The origins of depleted monolithic imaging detectors: deep depleted CCDs

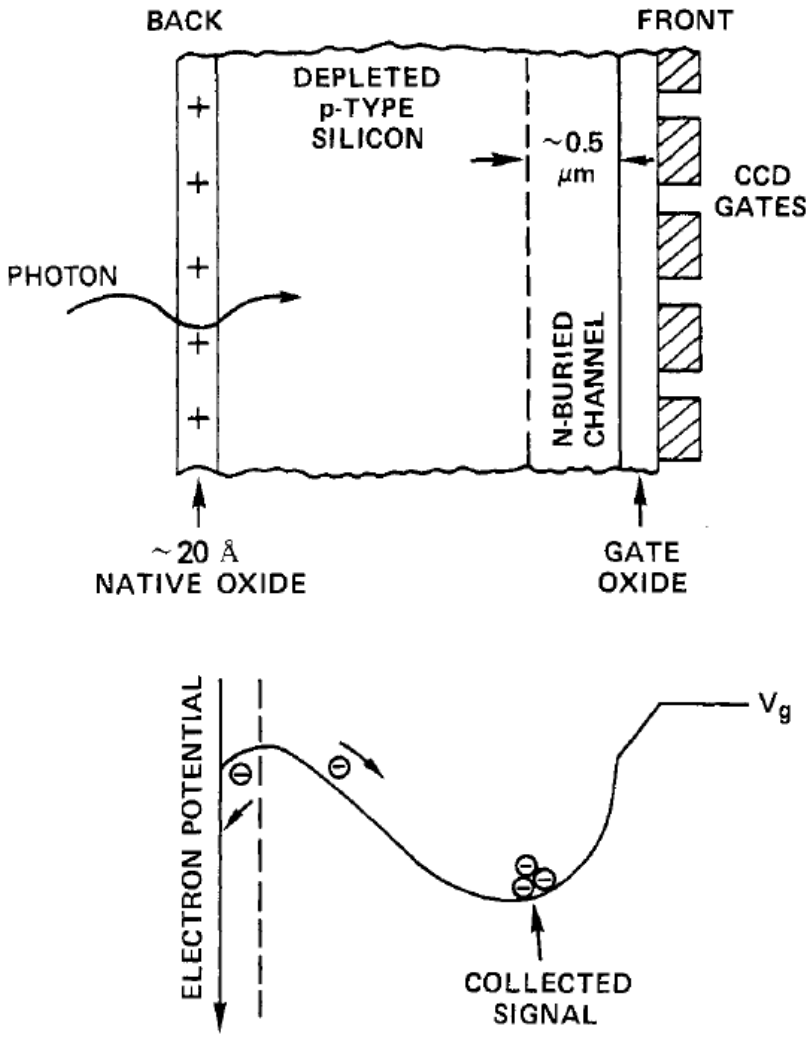


Fig. 2. Backside-Illuminated Deep-Depletion CCD

IEEE IEDM Tech. Dig. 1979

DEEP DEPLETION CHARGE-COUPLED DEVICES
FOR X-RAY AND IR SENSING APPLICATIONS

M. C. Peckerar, D. McCann, F. Blaha, W. Mend & R. Fulton

Westinghouse Electric Corporation
Advanced Technology Laboratory
Baltimore, Maryland 21203

IEEE IEDM Tech. Dig. 1985

DEEP-DEPLETION CCDS WITH IMPROVED UV SENSITIVITY

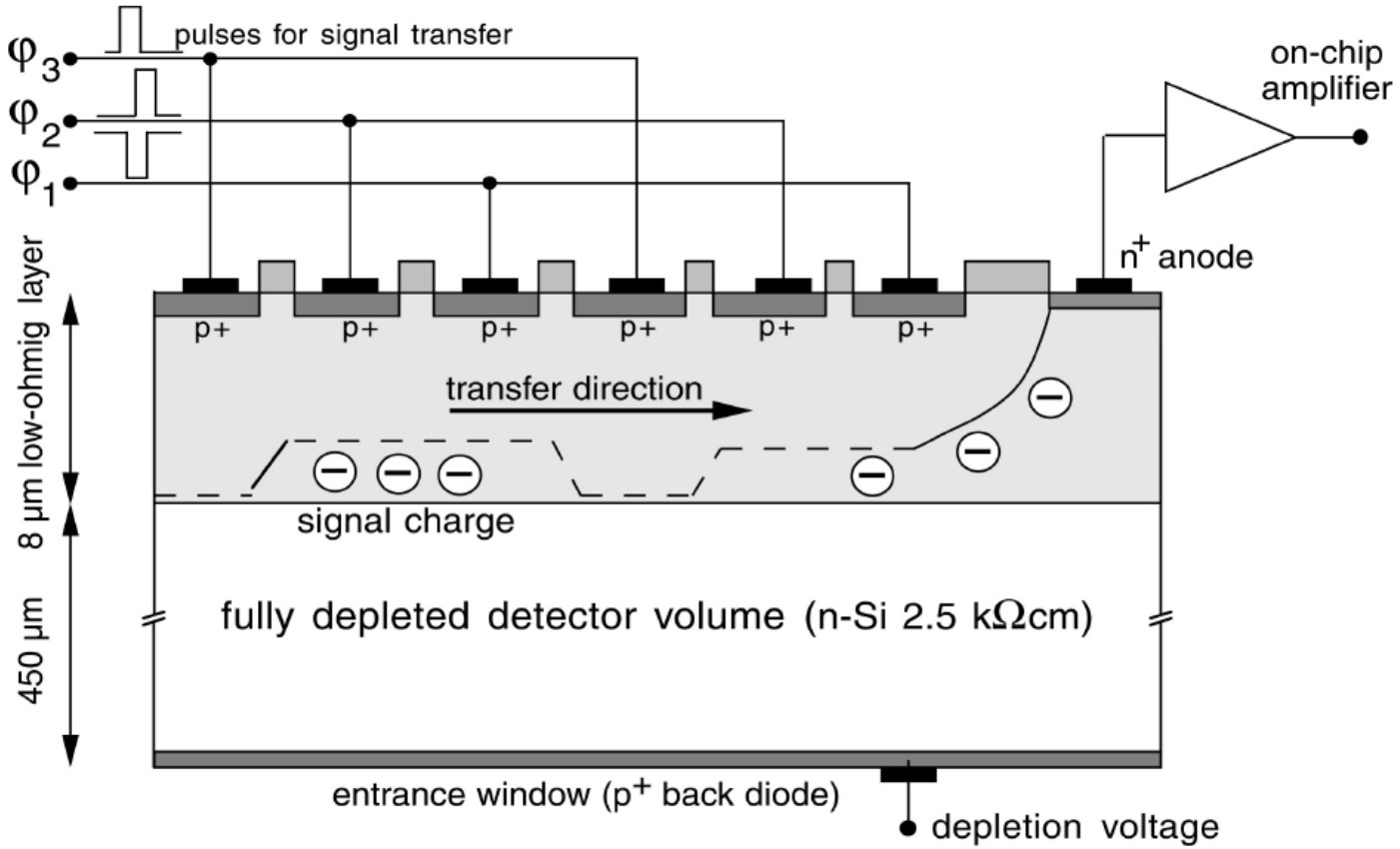
J.T. Bosiers*, N.S. Saks, D.J. Michels, D. McCarthy, M.C. Peckerar

Naval Research Laboratory, Washington, D.C. 20375

*Sachs-Freeman Associates, Inc., Landover, MD 20785

The origins of depleted monolithic imaging detectors: pn CCDs

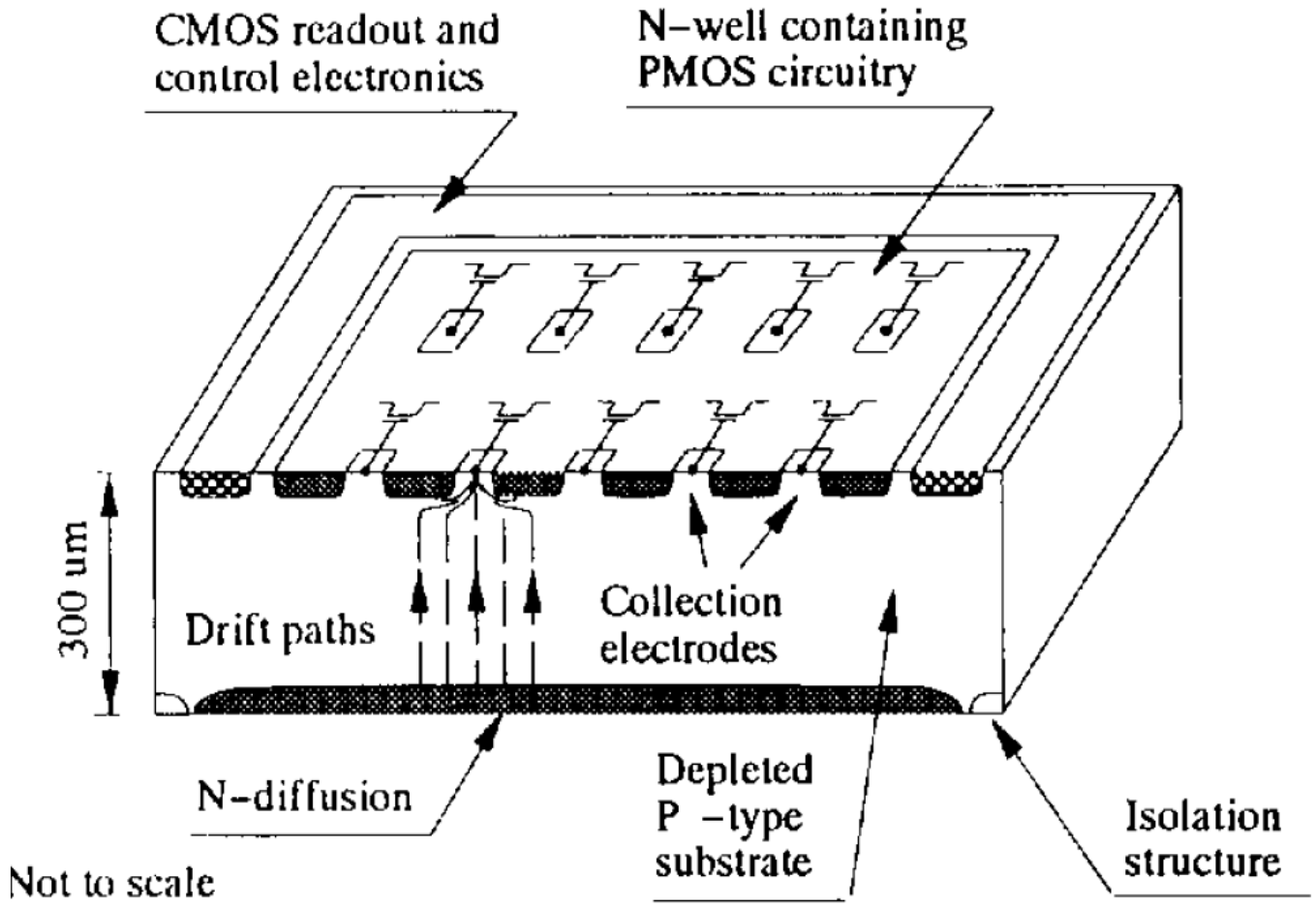
- Idea dates back to the 1980s (E.Gatti, P. Rehak)
- Operation concept: same as CCD, but gates are replaced with pn junctions
- Successfully employed in color X-ray imaging, X-ray fluorescence, electron detection in SEM/TEM microscopy



S. Ihle et al., IEEE NSS 2008

CMOS fully depleted pixel array with backside junction

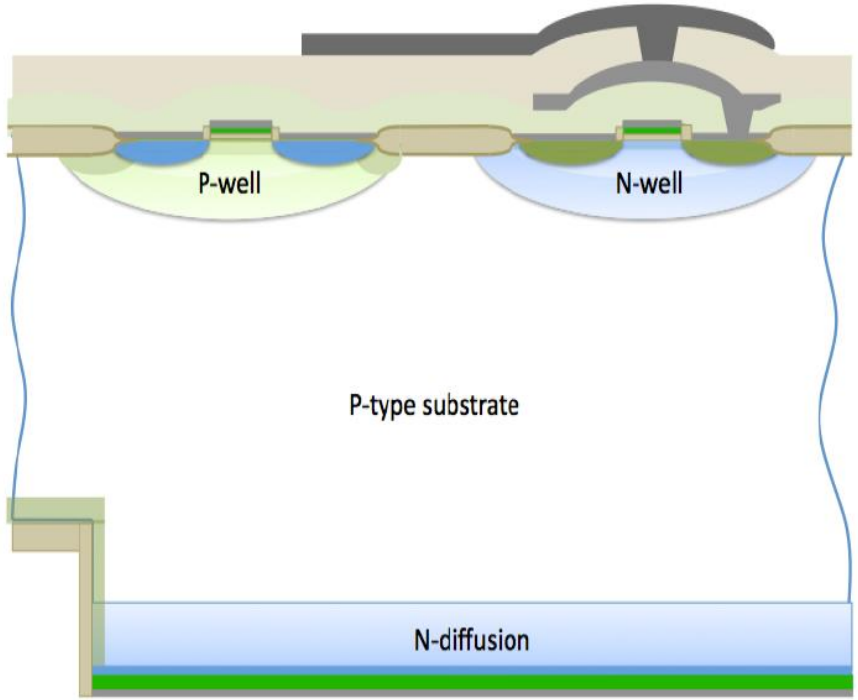
- Full CMOS at the periphery
- PMOS-only in the pixels
- Backside N-diffusion: backside processing needed
- P-type collection nodes: collection of holes



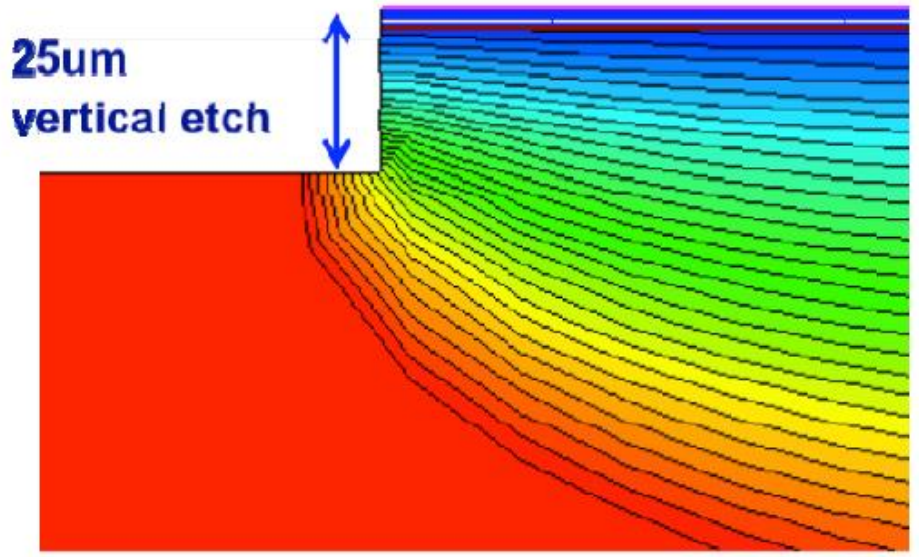
W. Snoeys, IEEE Tran. Electron Dev., 1994

CMOS fully depleted pixel array pixel array with backside junction

- BS junction terminates on a trench for breakdown prevention
- Requires BS lithography and trench etching in the middle of the process flow: difficult to integrate in a commercial CMOS



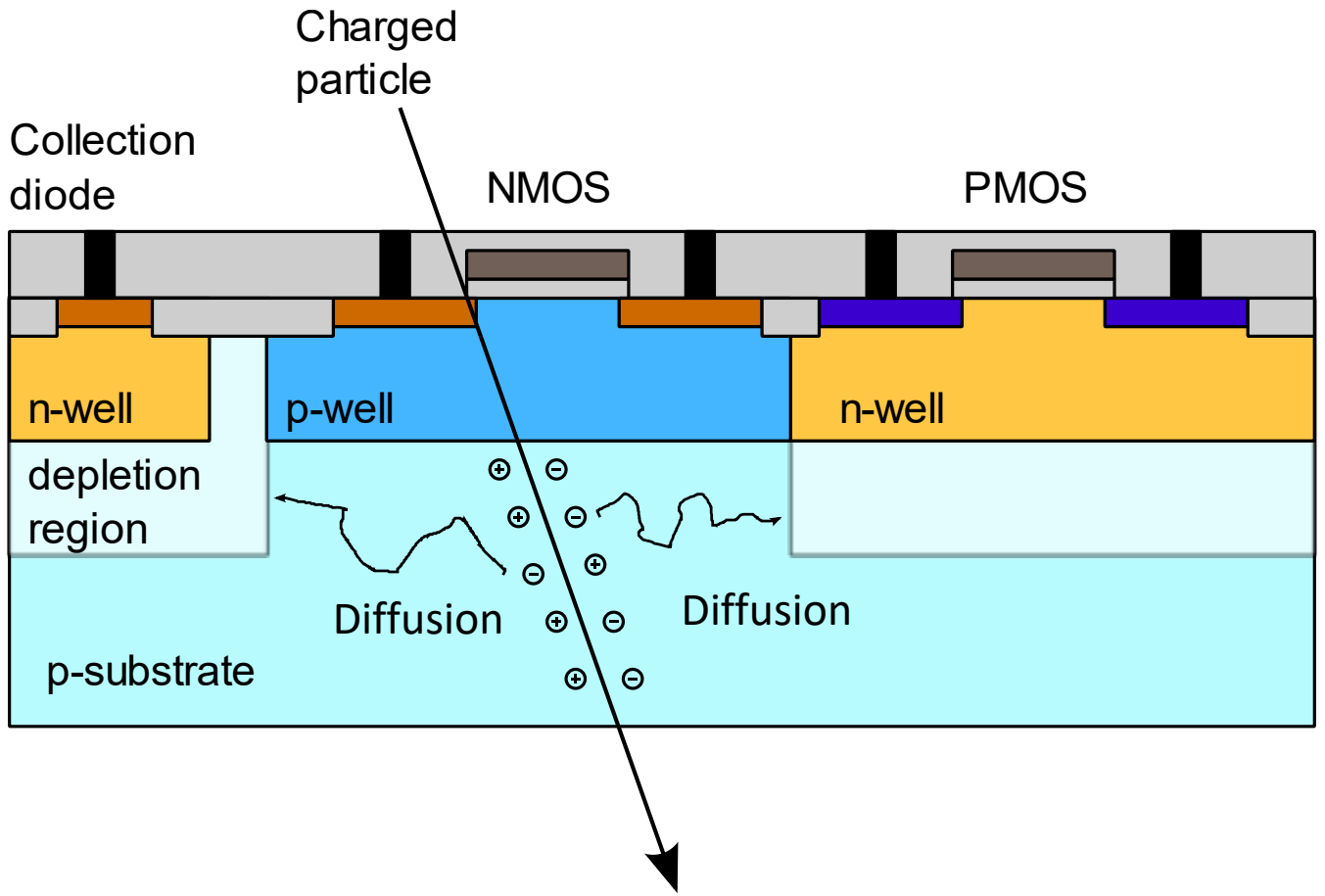
J. D. Segal, IEEE NSS 2010.



Simulated potential

Standard twin-well CMOS: features

- Twin wells: to host NMOS and PMOS transistor
- Sensor: implemented with nwells
- p-substrate with intermediate resistivity (typ. 10 Ohm cm): only a few μm depletion region for typical voltages
- Collection speed: **slow diffusion** in non-depleted substrate
- **Competitive collection** by nwells: low efficiency

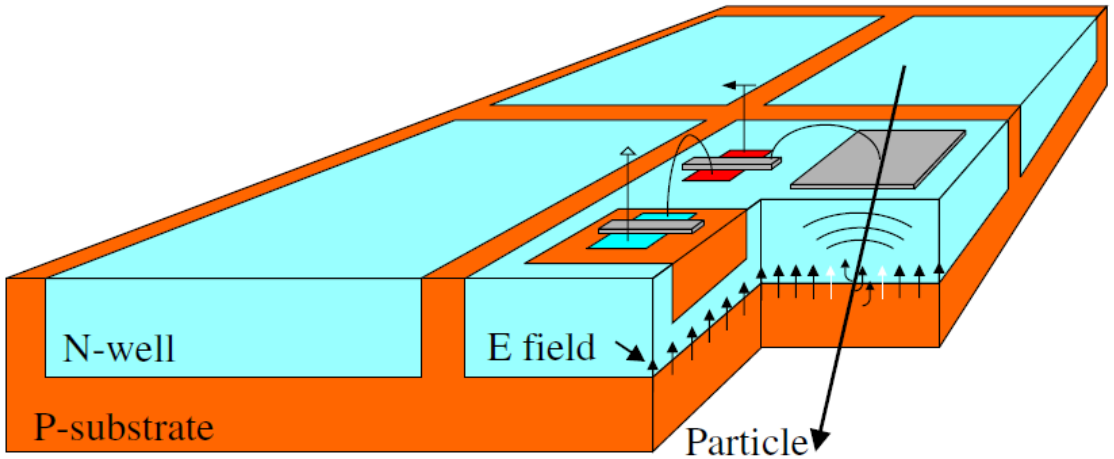


Customizing CMOS for improved MAPS performance

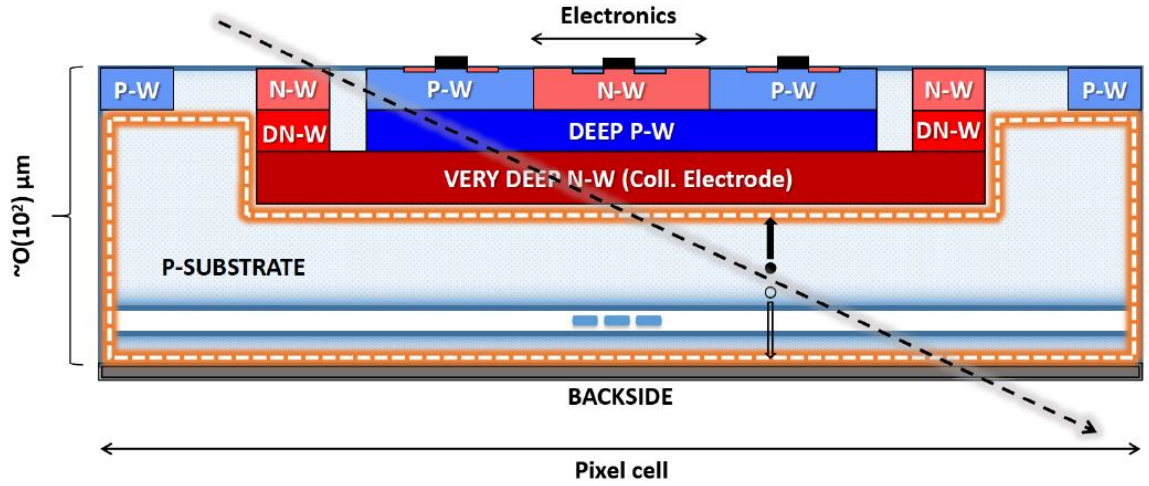
- Reduce the substrate doping: **high resistivity** silicon
- **High bias voltage** for large depletion region
- Avoid competitive charge collection. Three approaches:
  1. Put CMOS electronics inside the collection electrode: **large collection electrode**
  2. Isolating nwells other than collection electrodes with deep pwell: **small collection electrode**
  3. Isolate the electronics from the detectors with a buried oxide layer: **Silicon On Insulator (SOI)**

Large collection electrode: High Voltage CMOS

- The collection diode is a deep nwell.
- The CMOS electronics (pwells + nwells) is inside the deep nwell
- High voltage bias can be applied: large depleted volume



I. Peric et al., NIM A582 (2007) pp. 876-885



I. Caicedo et al 2019 JINST 14 C06006

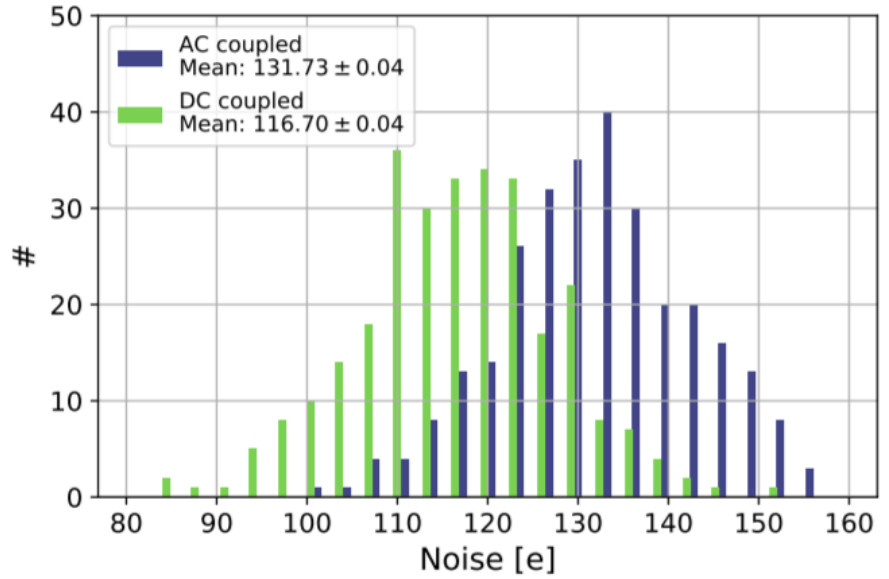
Large collection electrode with High-Resistivity substrate

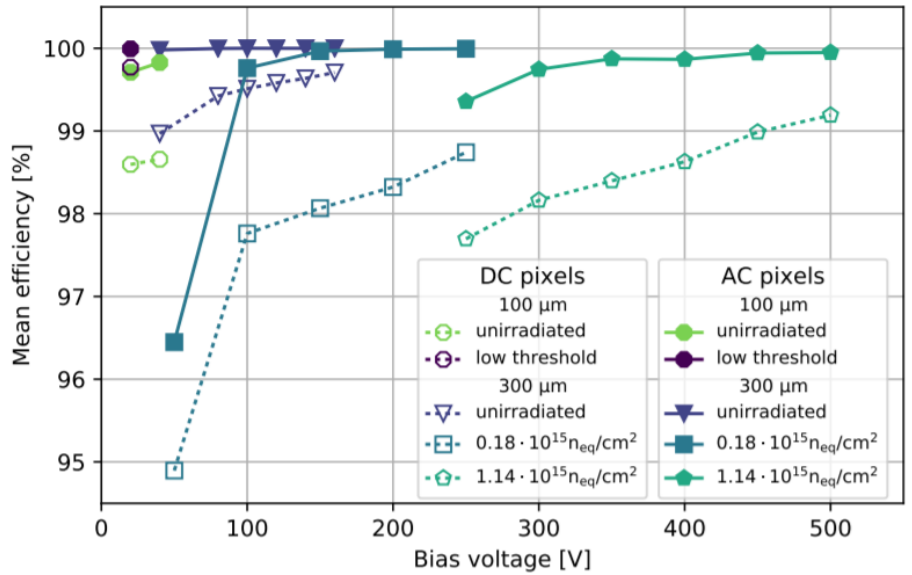
High resistivity substrates
(>2 kOhm/cm): depletion width > 250µm

- Uniform electric field
- Fast charge collection
- High efficiency
  at fluence > 10^{15} n_{eq}/cm^2

Main drawbacks:

- Parasitic capacitance: large noise

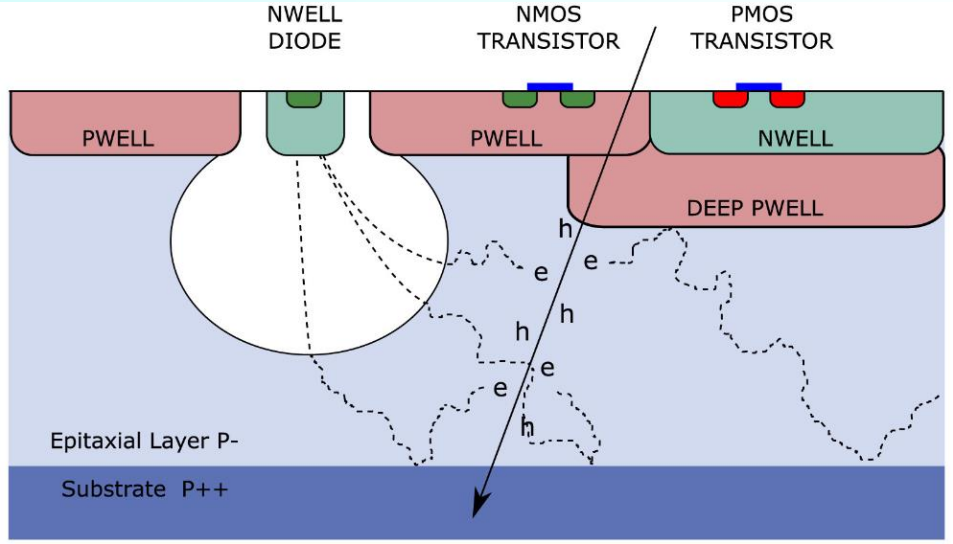




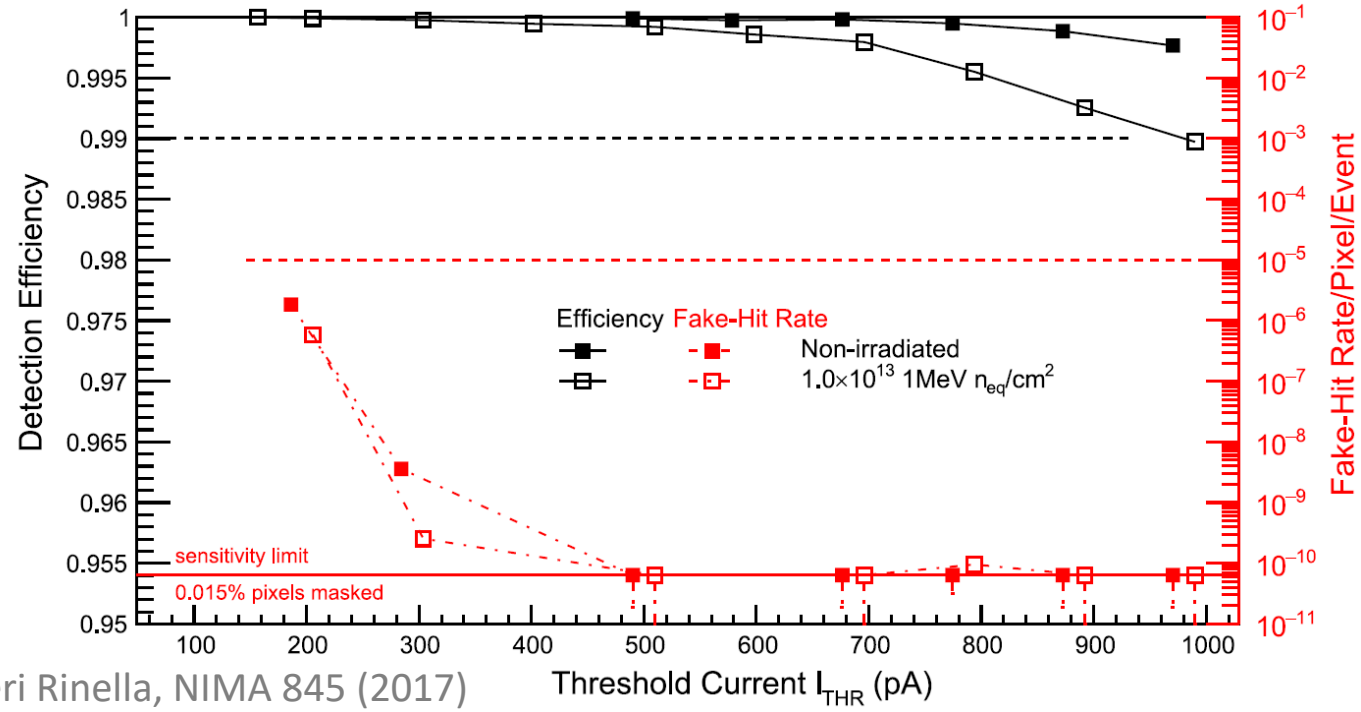
D.-L. Pohl, 2017 JINST 12 P06020

Small collection electrode: ALPIDE

- Installed on ALICE ITS
- Nwell shielded by **deep pwell** (J.P. Crooks et al. IEEE NSS 2007)
- **High resistivity** (> 1kΩ cm) p-type **epi-layer** with 25 µm thickness
- 28 x 28 µm^2 pixel size
- Small sensor capacitance: low noise
- **Partial depletion**: drift and diffusion
- Radiation tolerance: NIEL up to 10^{13} (1MeV n_{eq})/cm^2



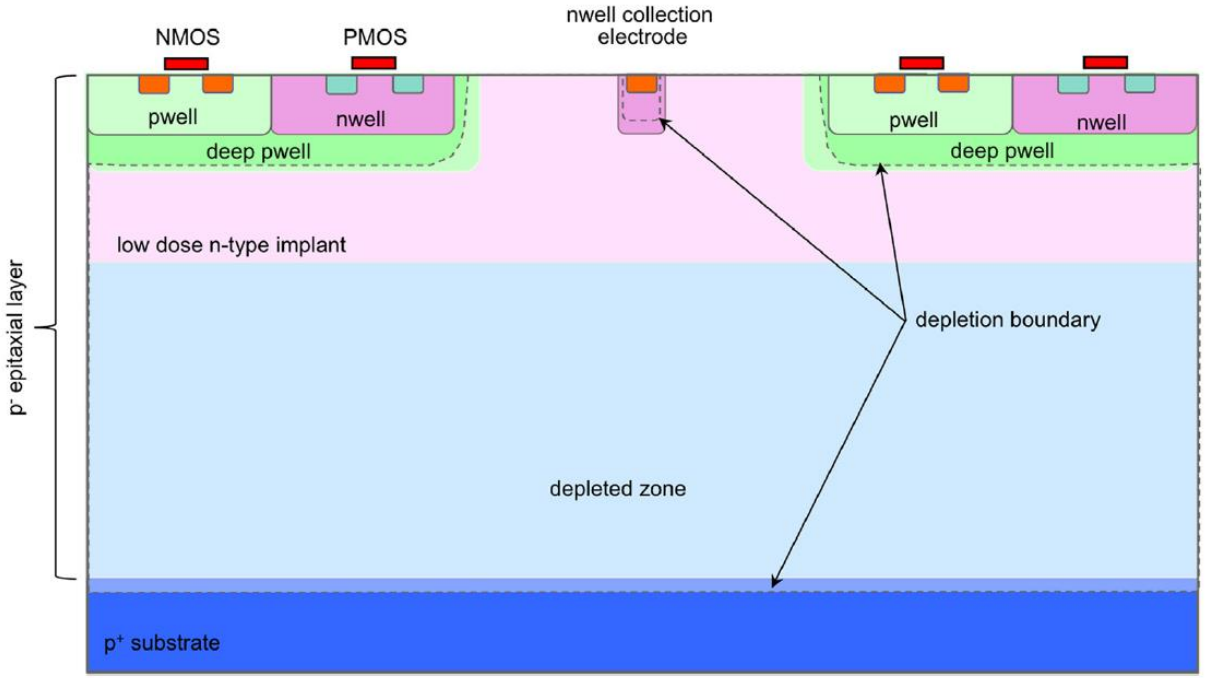
M. Mager, NIMA 824 2016



G. Aglieri Rinella, NIMA 845 (2017)

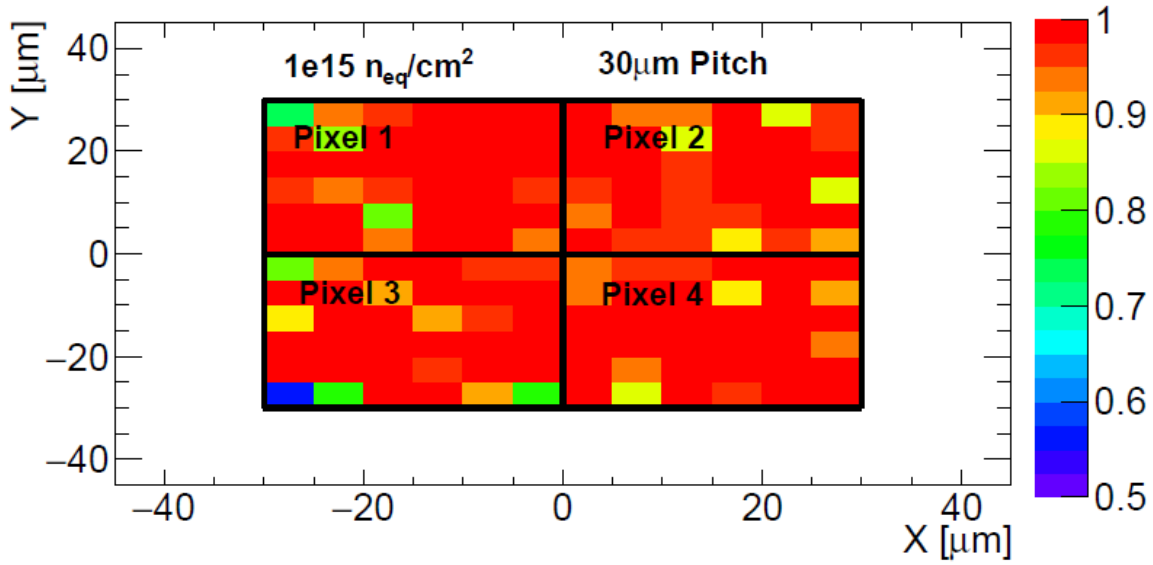
Depleted MAPS with small collection electrode

- Produced in CMOS 180nm process modified with a low-doped n-type deep implantation
- Fully depleted: charge collection by drift
- Fast charge collection: few ns
- Good efficiency and speed after irradiation at **10^{15} (1MeV n_{eq})/cm^2**



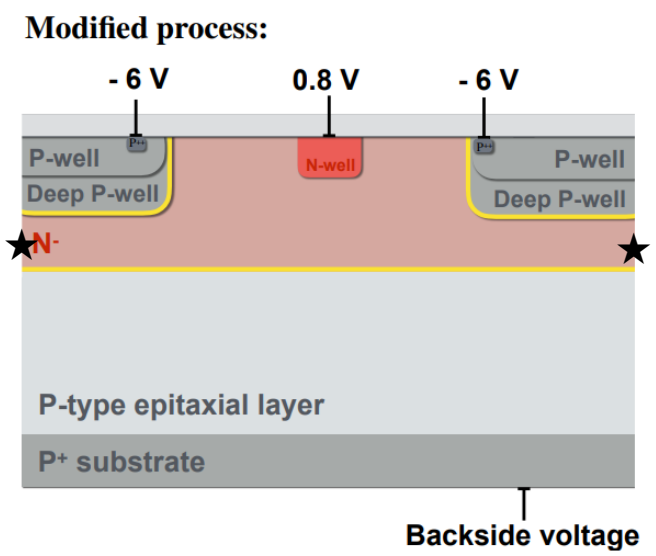
W. Snoeys et al., NIMA 2017

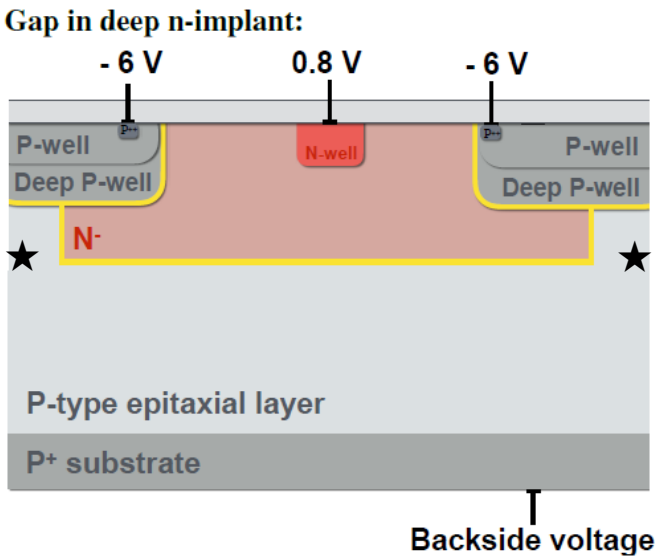
Efficiency vs. hit position

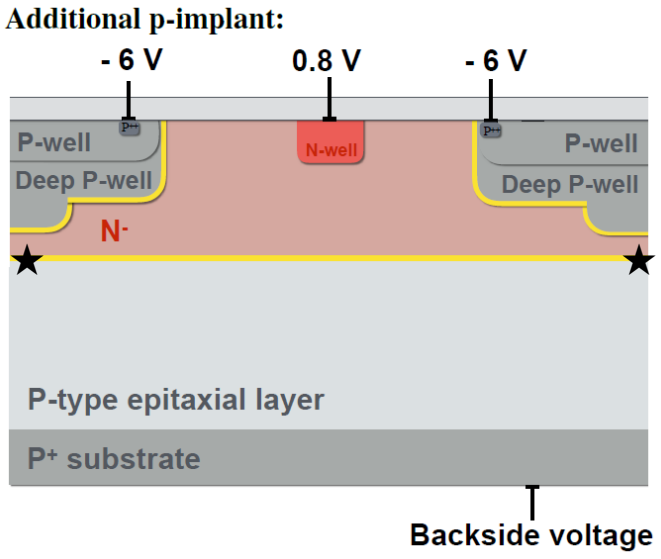


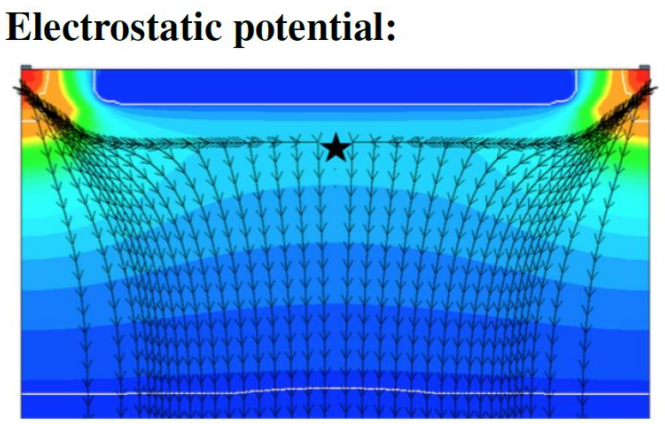
H. Pernegger et al., 2017 JINST 12 P06008

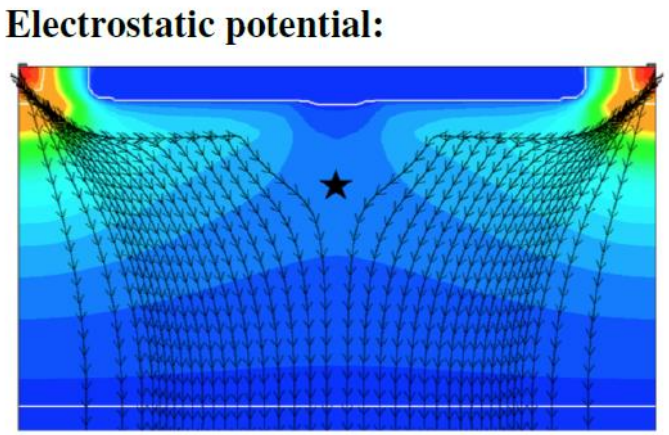
Depleted MAPS with small collection electrode: going faster

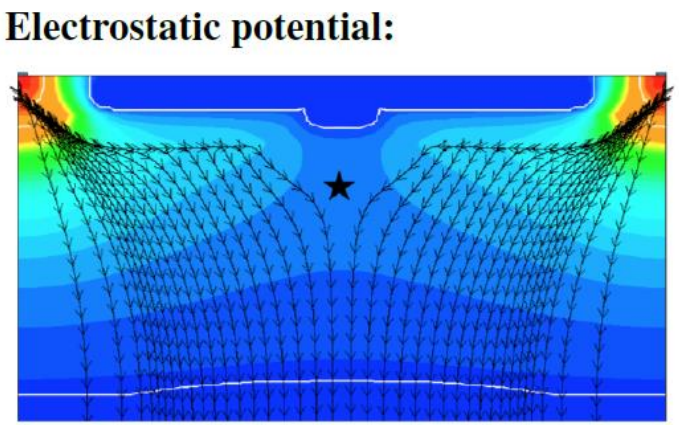






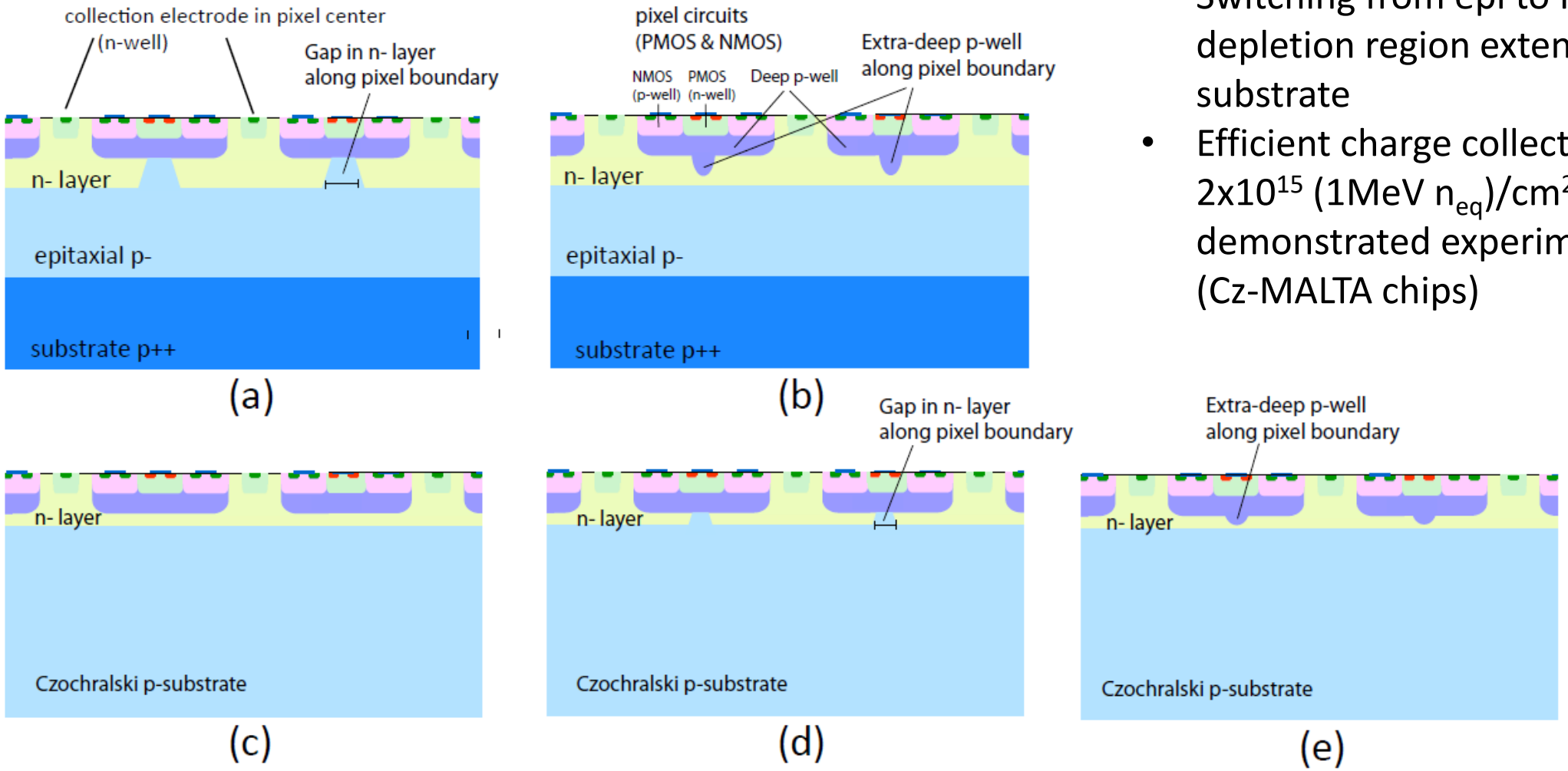






M. Munker et al 2019 JINST 14 C05013

Depleted MAPS with small collection electrode: going thicker

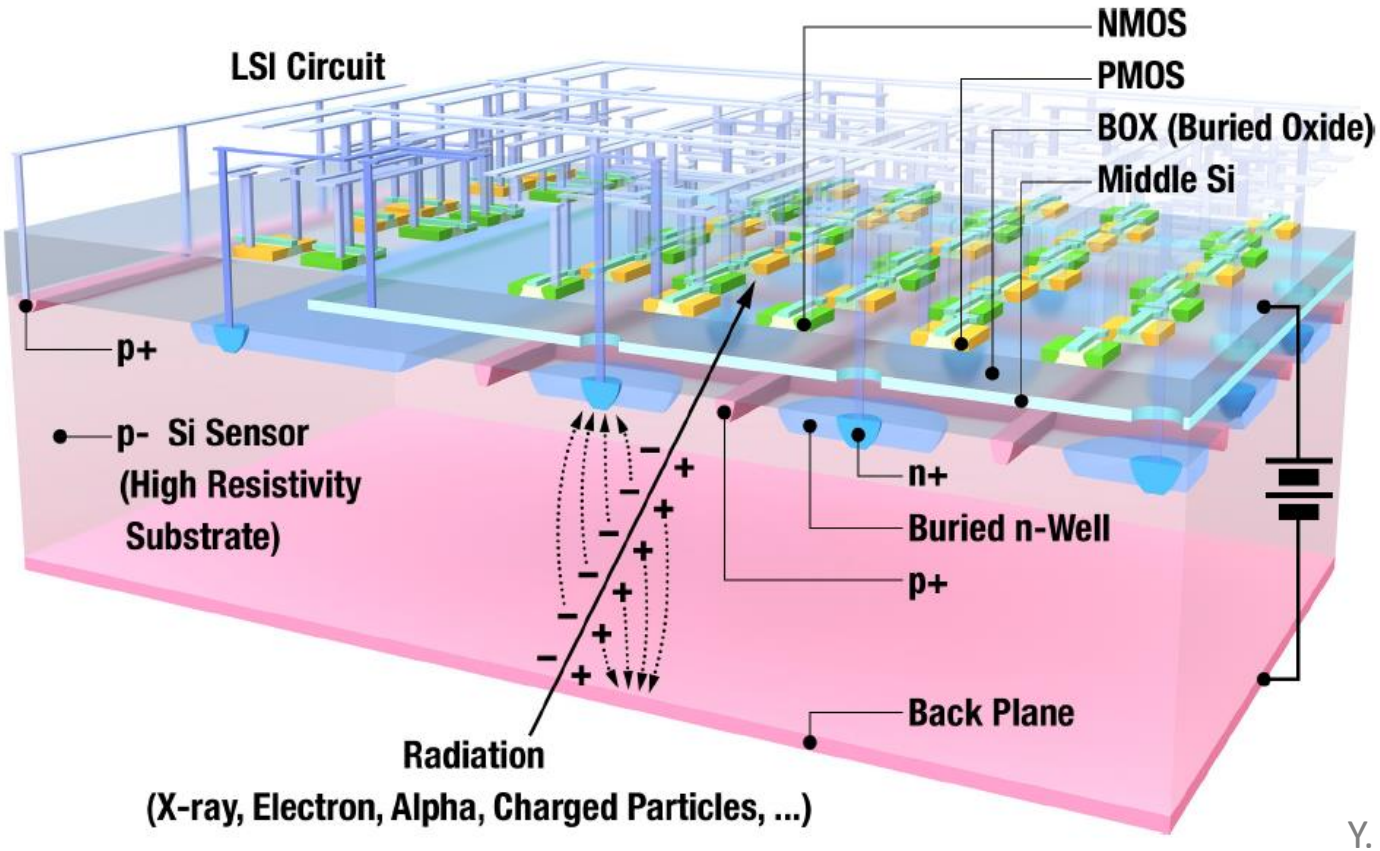


- Switching from epi to HR silicon: depletion region extends into the substrate
- Efficient charge collection up to $2x10^{15}$ (1MeV n_{eq})/cm^2 demonstrated experimentally (Cz-MALTA chips)

H. Pernegger et al 2023 JINST 18 P09018

Fully-Depleted SOI sensors

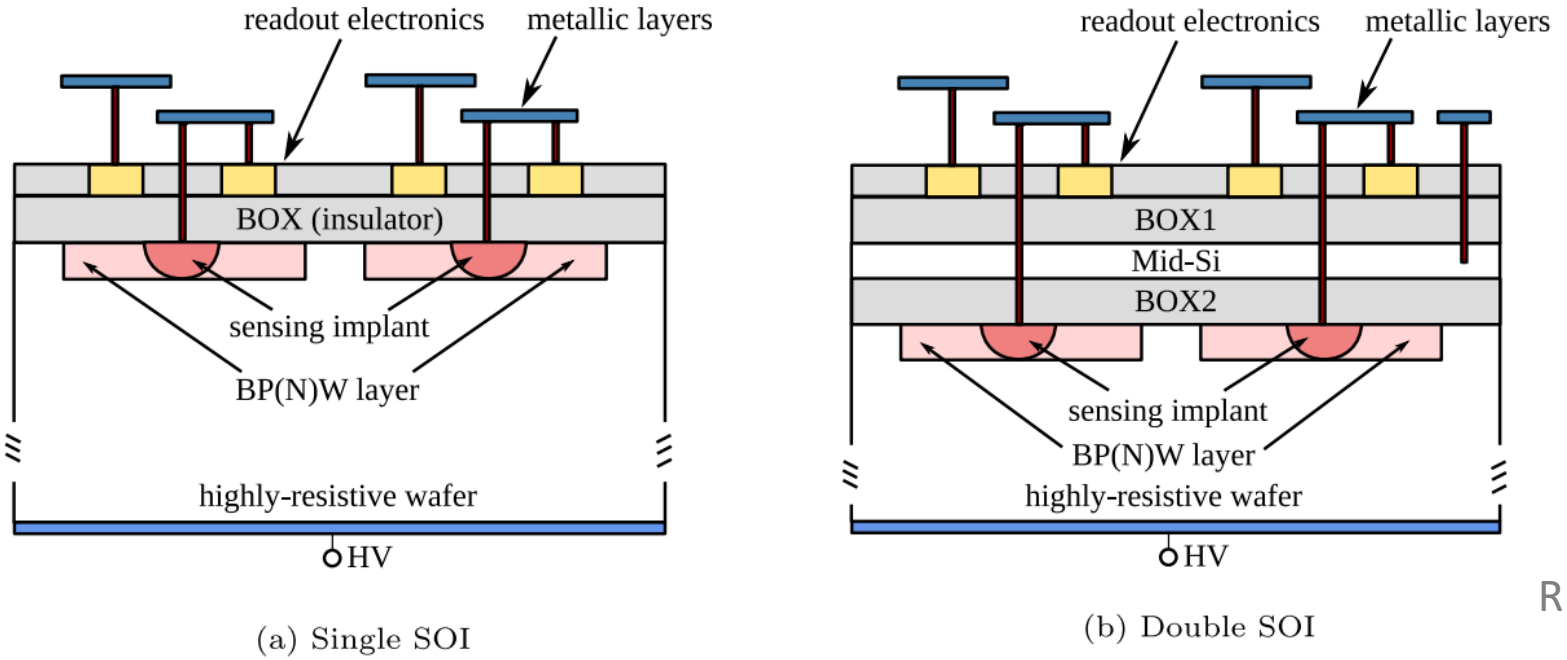
- Buried oxide layer: separates detectors from electronics
- High resistivity substrate: up to 500µm depleted thickness



Y. Arai, IEEE IEDM 2017

FD-SOI progress

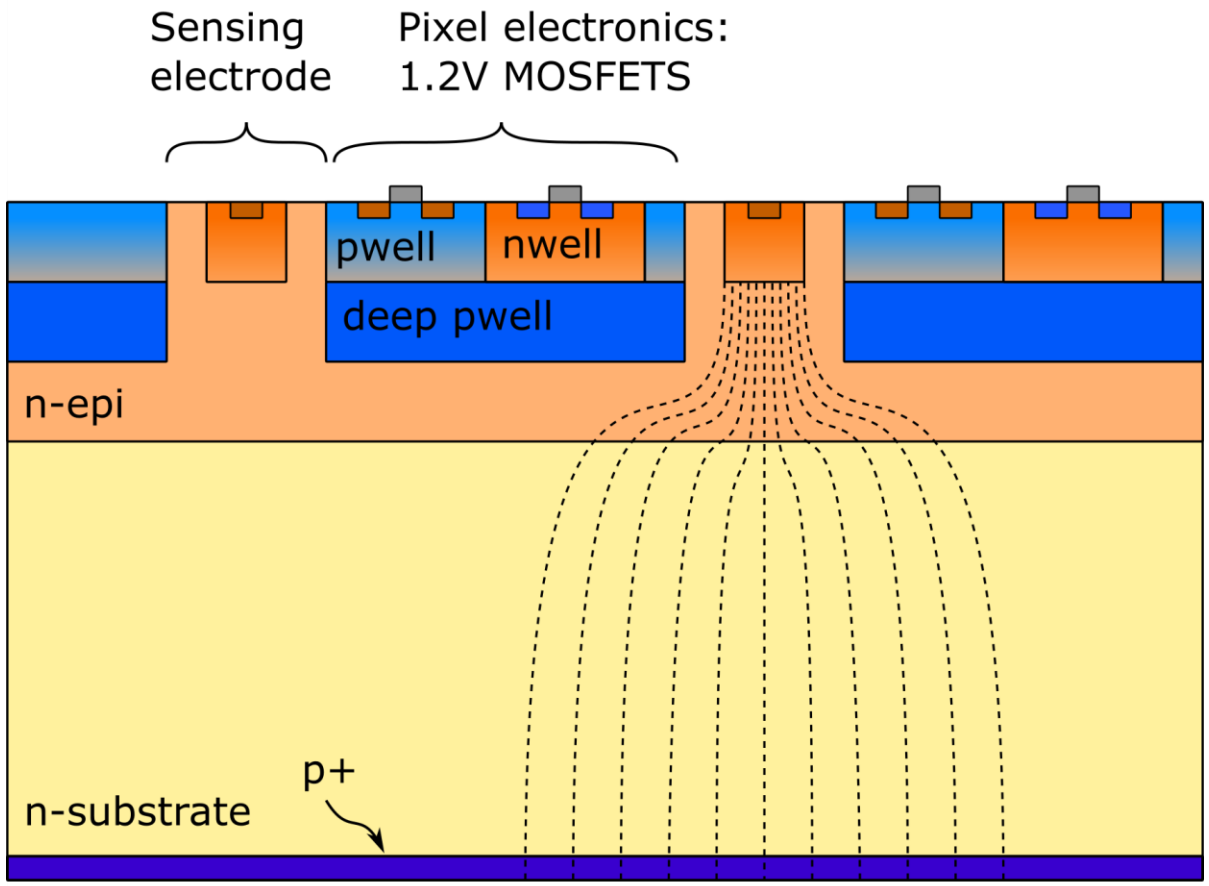
- Problem: buried oxide affects electronics → back-gate effect
- Solution: 2 buried oxide layers
- Ionizing radiation tolerance up to 100kGy (Y. Arai, IEEE IEDM 2017)
- Reduced electronic noise
- Issues: SOI wafer cost, single vendor



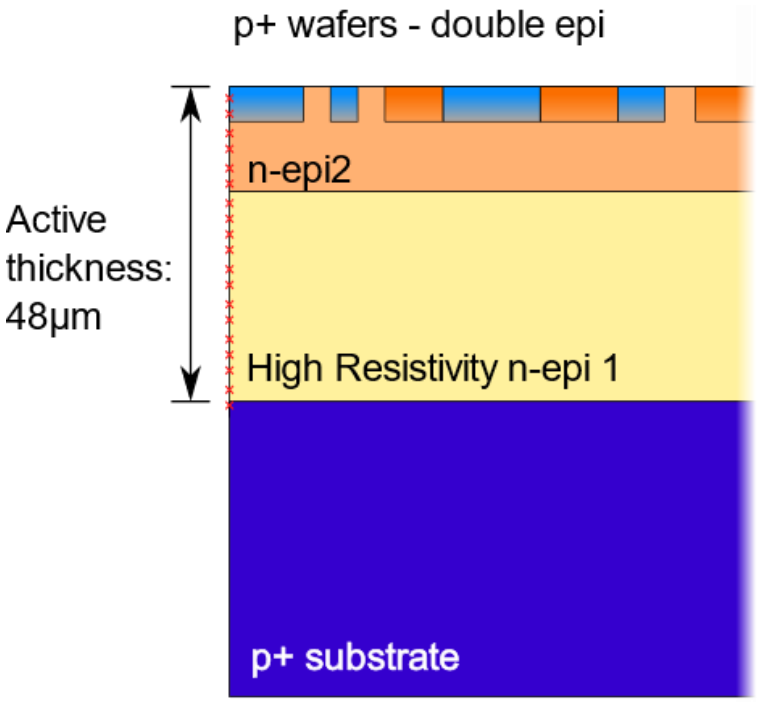
R. Bugiel, et al., NIMA 988, 2021

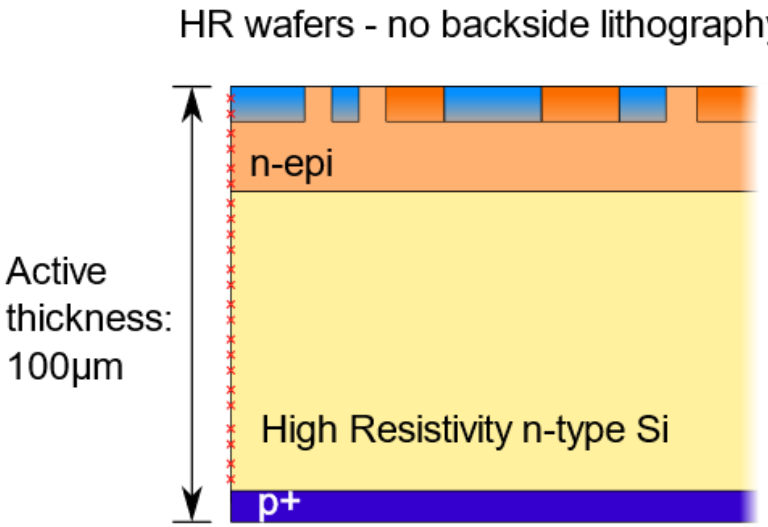
ARCADIA - Sensor concept

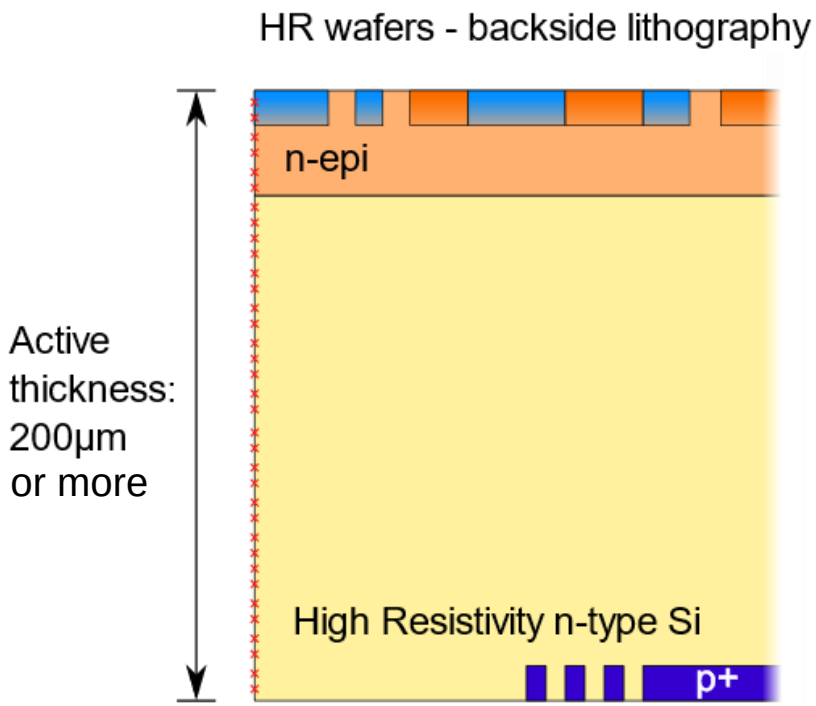
- Customized **110nm CMOS** process (LFoundry)
- Small Collection Electrodes
- **Deep pwells**
- n-type **high resistivity** active region
- Reverse-biased **junction at the bottom**: depletion grows from back to top
- **n-epi** layer: reduce **punch-through** current between p+ and deep pwells
- **Sensing** electrodes can be biased at **low voltage** (< 1V)



Wafer post-processing: starting material and backside process





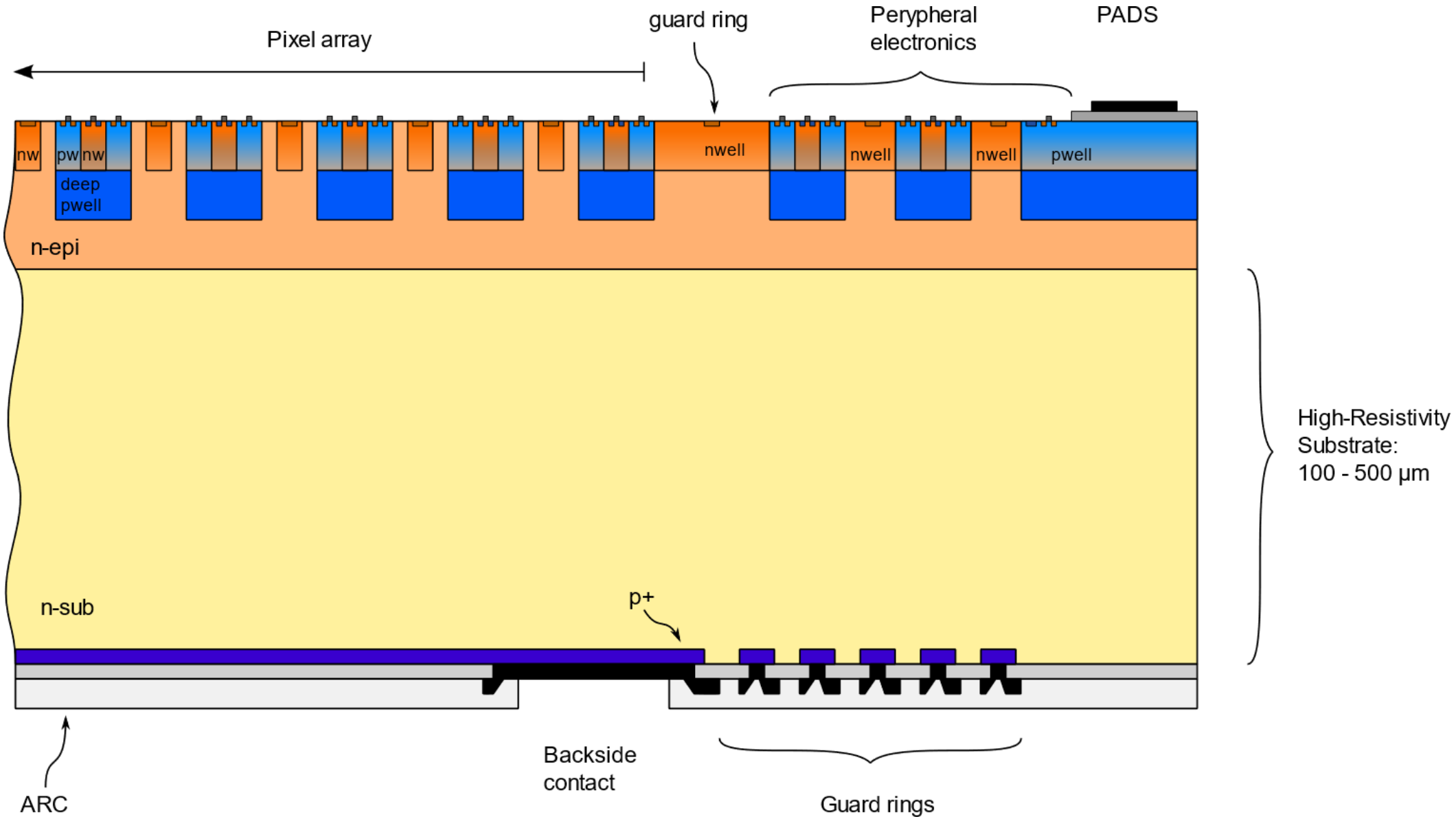


Type 1:
Post-processing: thinning to 100 or 300µm total thickness

Type 2:
Post-processing: thinning, backsided **p+ implantation** and laser annealing

Type 3:
Post-processing: thinning, **lithography**, backside **p+ implantation** and laser annealing, insulators and **metal** deposition

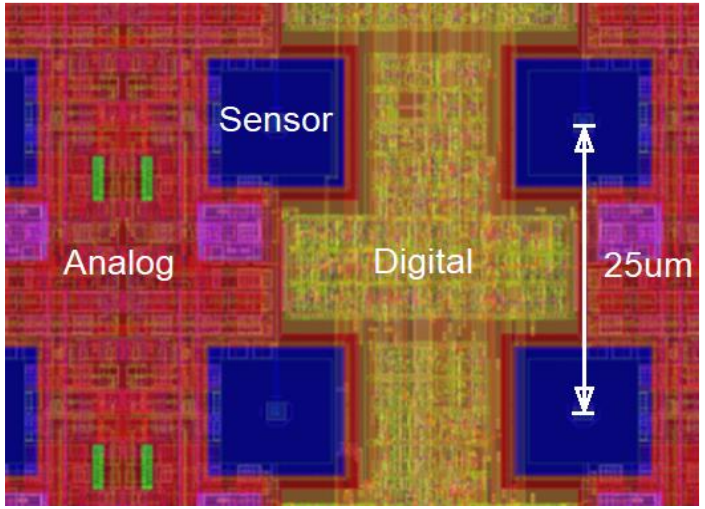
Pixel array cross section – backside lithography – type 3 substrates



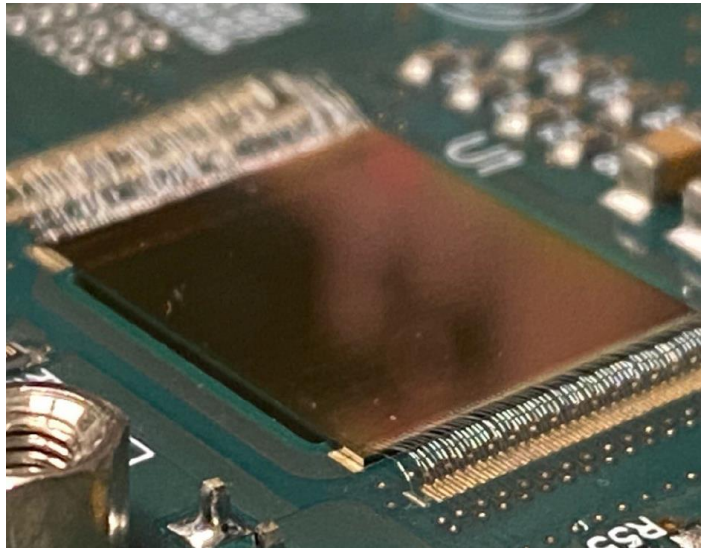
Main demonstrator: 512 x 512 pixel array for charged particle tracking

- Pixel pitch: 25µm – Array core area: 1.28cm x 1.28cm
- **Pixel** electronics: **analog and digital**. In-pixel threshold and data storage
- Architecture: **event-driven**. Pixel detecting events (charge pulses) send their address to the chip peripheral circuits
- Low **power** (20mW/cm^2) and high **event rate** (100 MHz/cm^2)

Layout M. Rolo



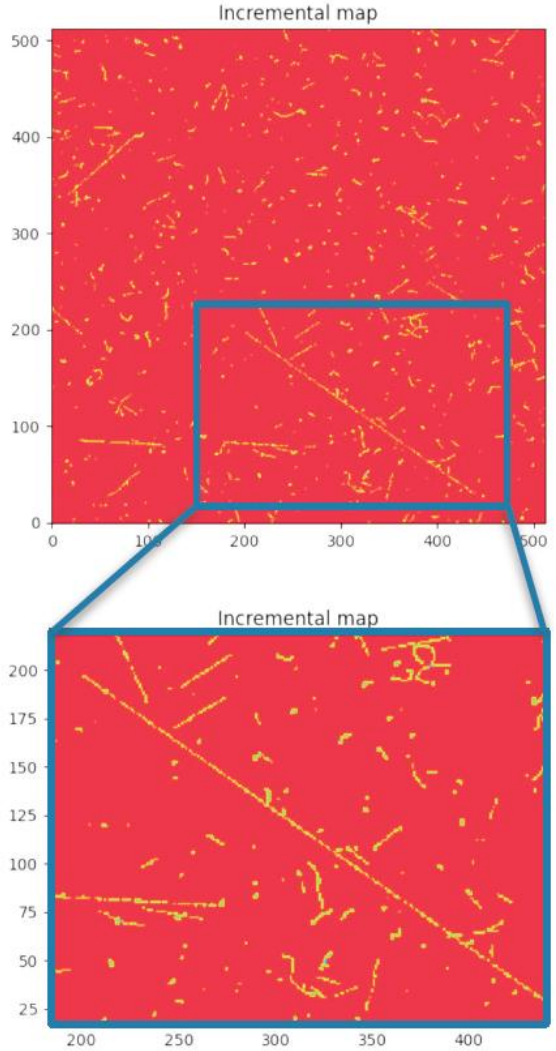
Detail of pixel layout



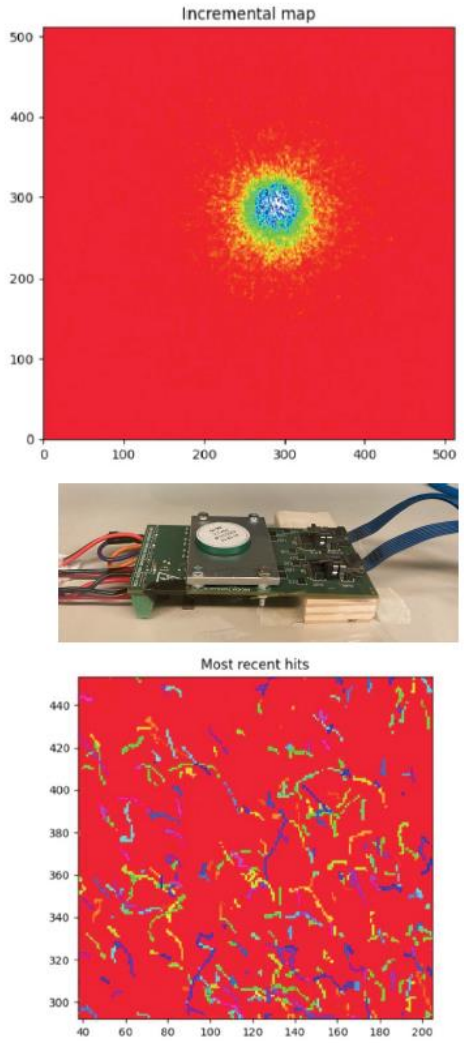
512 x 512 pixel sensor mounted on PCB

ARCADIA main demonstrator: detection of charged particles

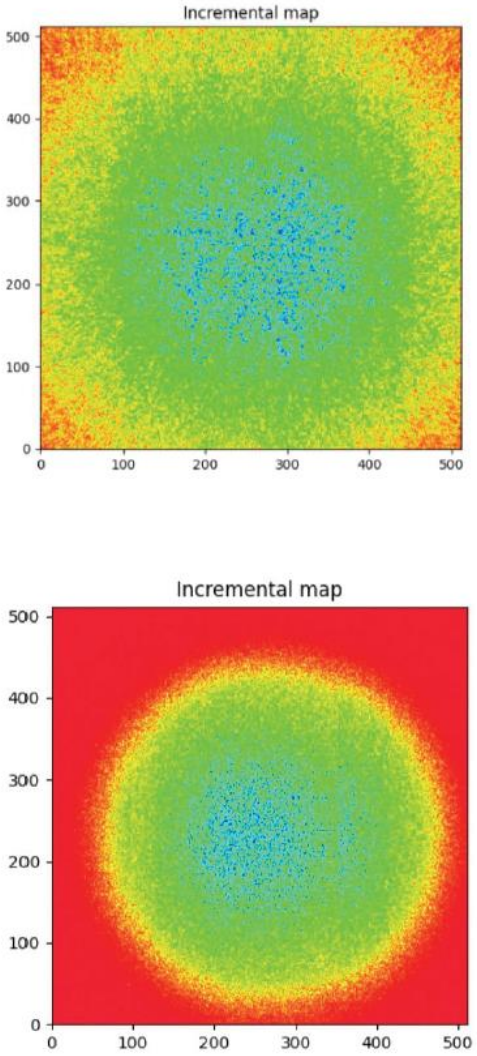
Cosmic rays
Tilted sensor



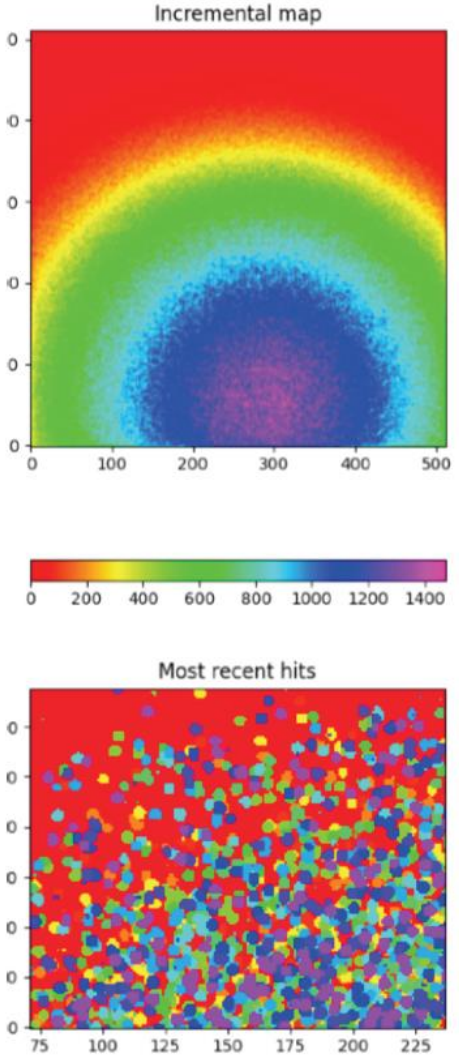
^{90}Sr beta source
collimated 1mm



^{90}Sr beta source



^{241}Am source

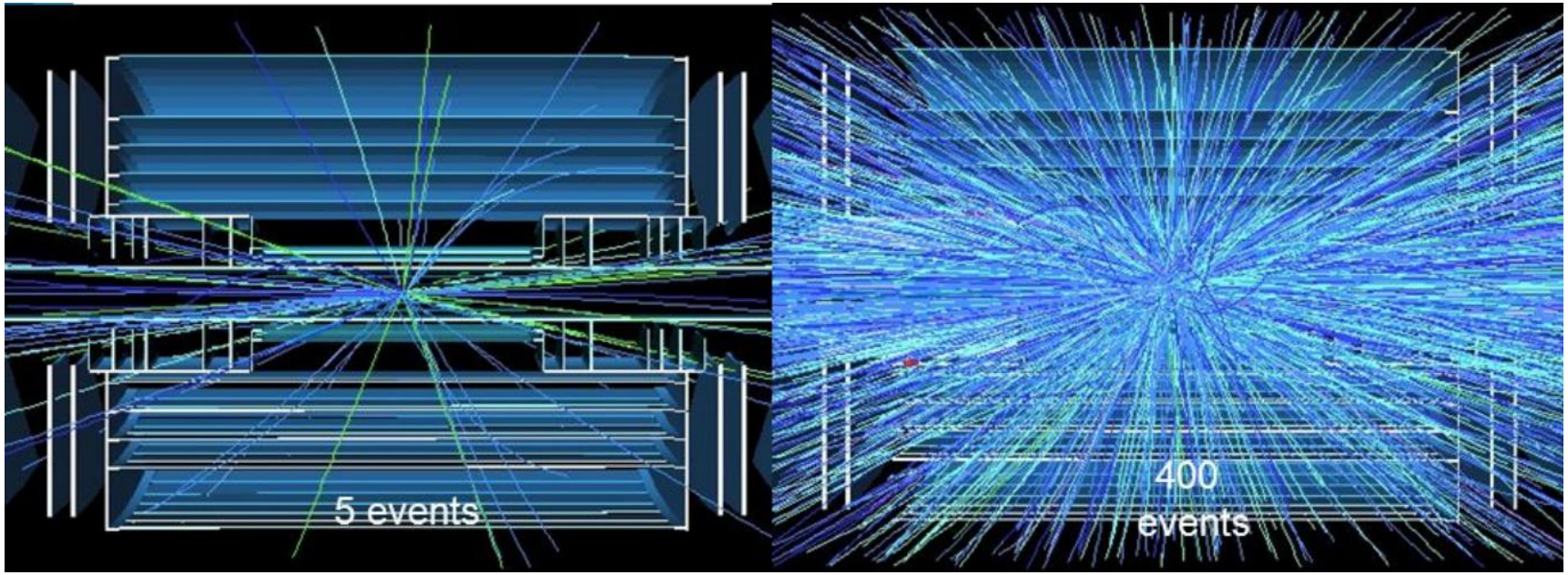


M. Rolo

Detectors for ps timing of charged particles

Applications:

- High Energy Physics: Time of Flight layers in High Luminosity experiments
- Space: ToF layers in astro-particle detectors
- Medical: time tagging of particles in therapeutic beams



M. Pierini, SOSC 2018

Sensor timing resolution

Fundamental limit

Non saturated velocity and non-uniform weighting field

Can be made **negligible**

$$\sigma_t^2 = \sigma_{\text{Time Walk}}^2 + \sigma_{\text{Landau Noise}}^2 + \sigma_{\text{Distortion}}^2 + \sigma_{\text{Jitter}}^2 + \sigma_{\text{TDC}}^2$$

Can be **corrected** (e.g. with Constant Fraction Discriminator, CFD)

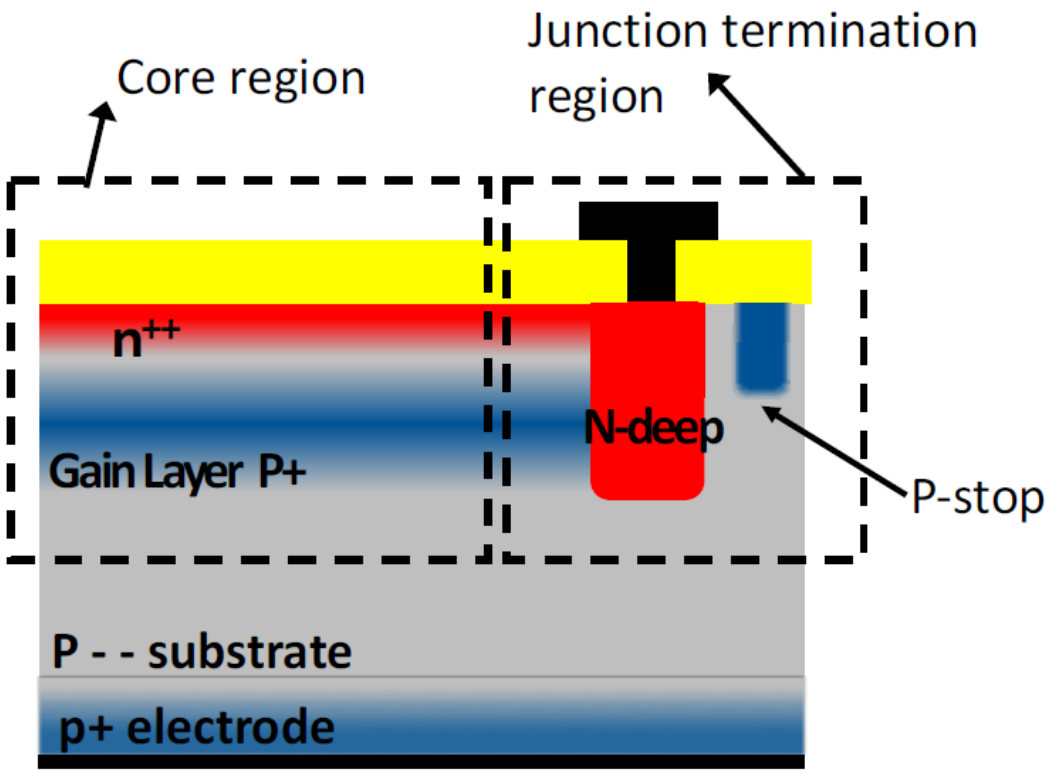
$$\sigma_{Jitter} \propto \frac{\sigma_V}{\frac{dV}{dt}}$$

- σ_V: Low input capacitance, High preamp. transconductance
- $\frac{dV}{dt}$: Large signal (gain); Short signal rise time

H. F.-W. Sadrozinski et al 2018 Rep. Prog. Phys. 81 026101

LGADs: operation

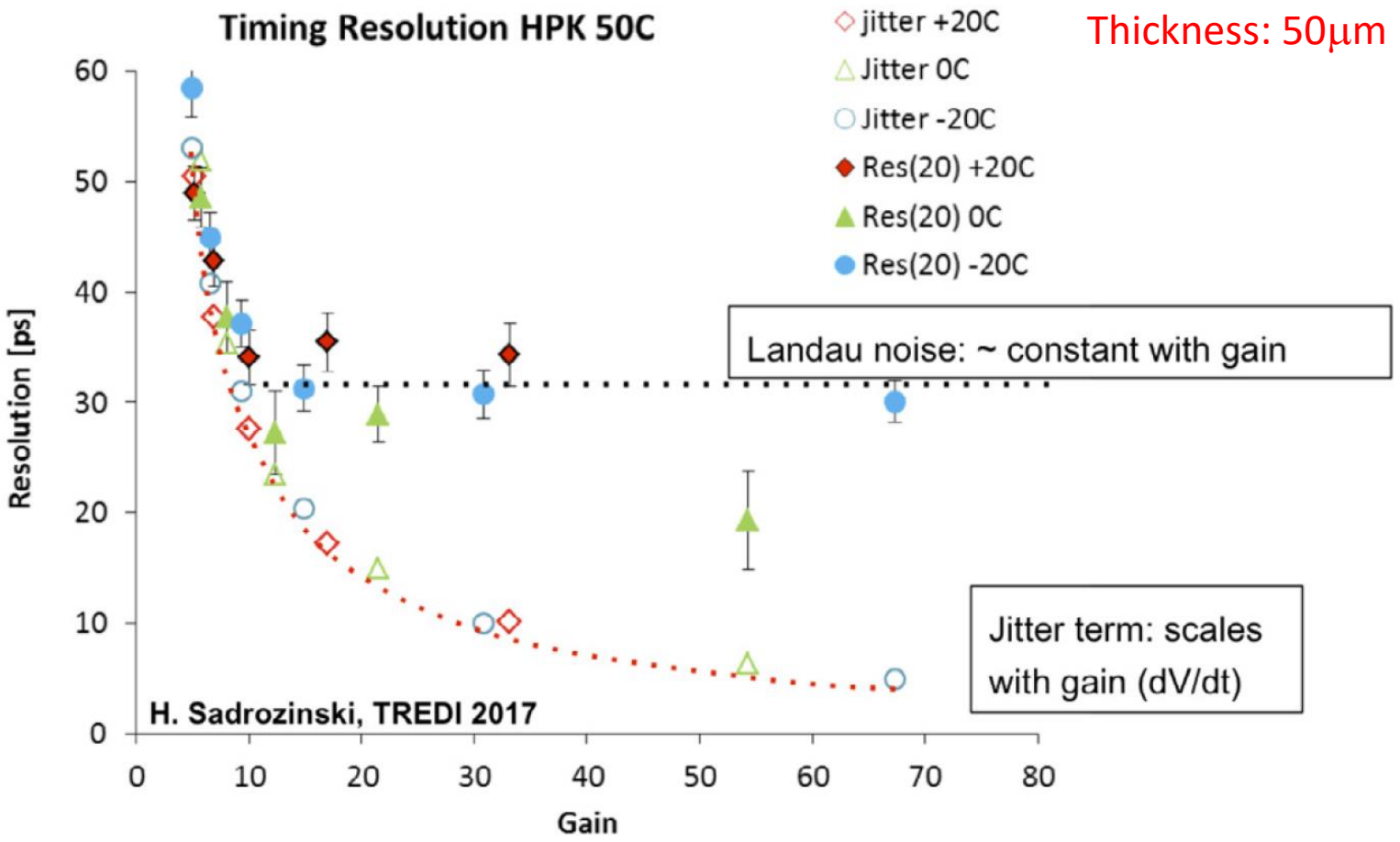
- Avalanche multiplication: linear-mode (sub-Geiger) operation
- Separate absorption-multiplication region:
  - Fully depleted HR substrate or epitaxial layer
  - P+ gain layer: high electric field
- Gain area termination needed: dead (no gain) region between the pixels



G. Paternoster et al., J. Instrum., vol. 12, no. 2, 2017, Art. no. C02077

LGADs: timing resolution

- Uniform electric field in a large area (~ mm^2): $\sigma_{distortion}$ is negligible
- The effect of electronics noise on timing resolution (σ_{jitter}) can be reduced by increasing the gain
- Fundamental limitation: **Landau noise**, due to fluctuations in the released charge



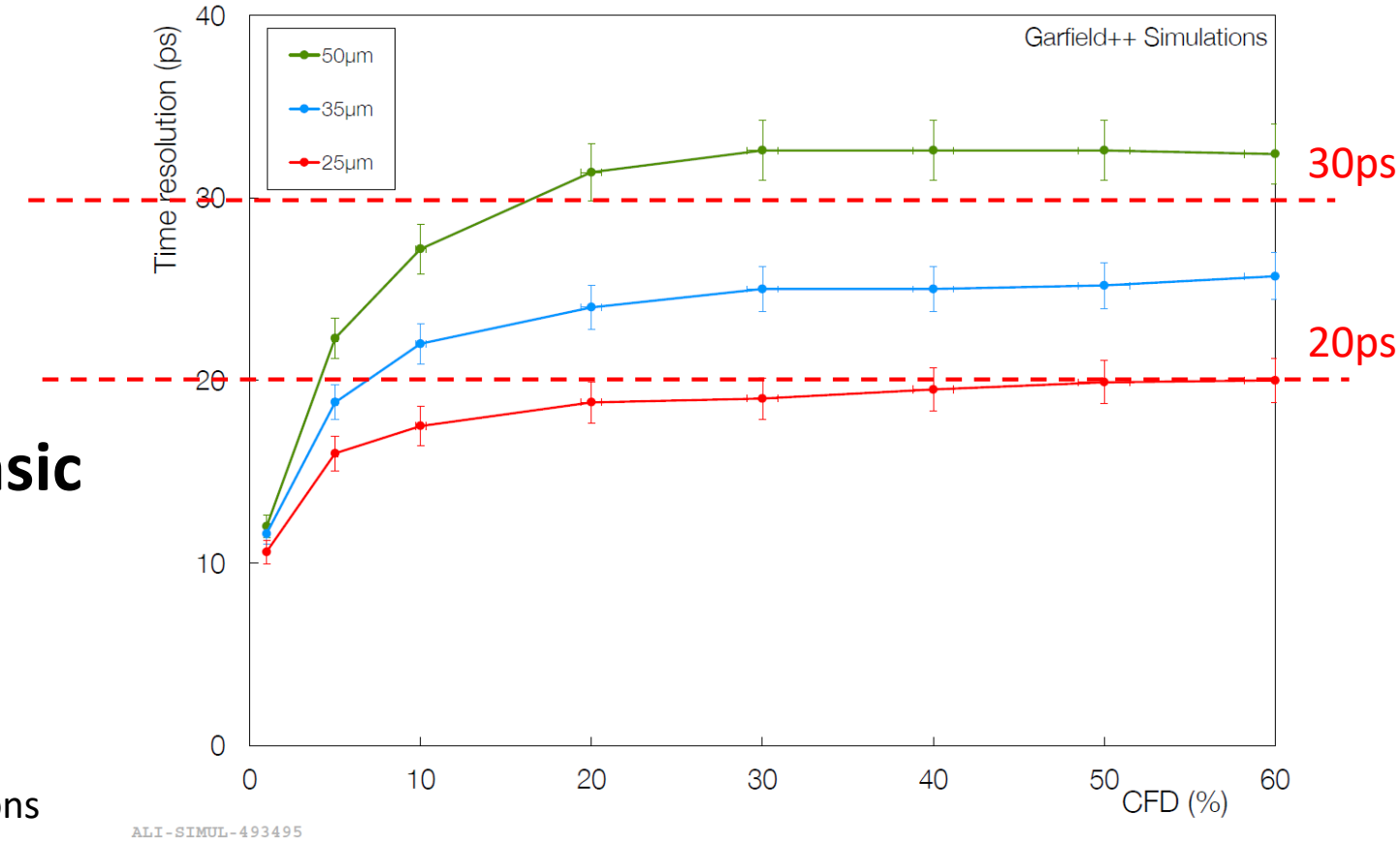
N. Cartiglia et al., NIM A 924 (2019) 350-354

How to go below 30ps with LGADs?

- Low threshold → practical limits in an array due to electronic noise, pixel non-uniformity and electrical cross-talk

- **Sensor thickness < 50µm**

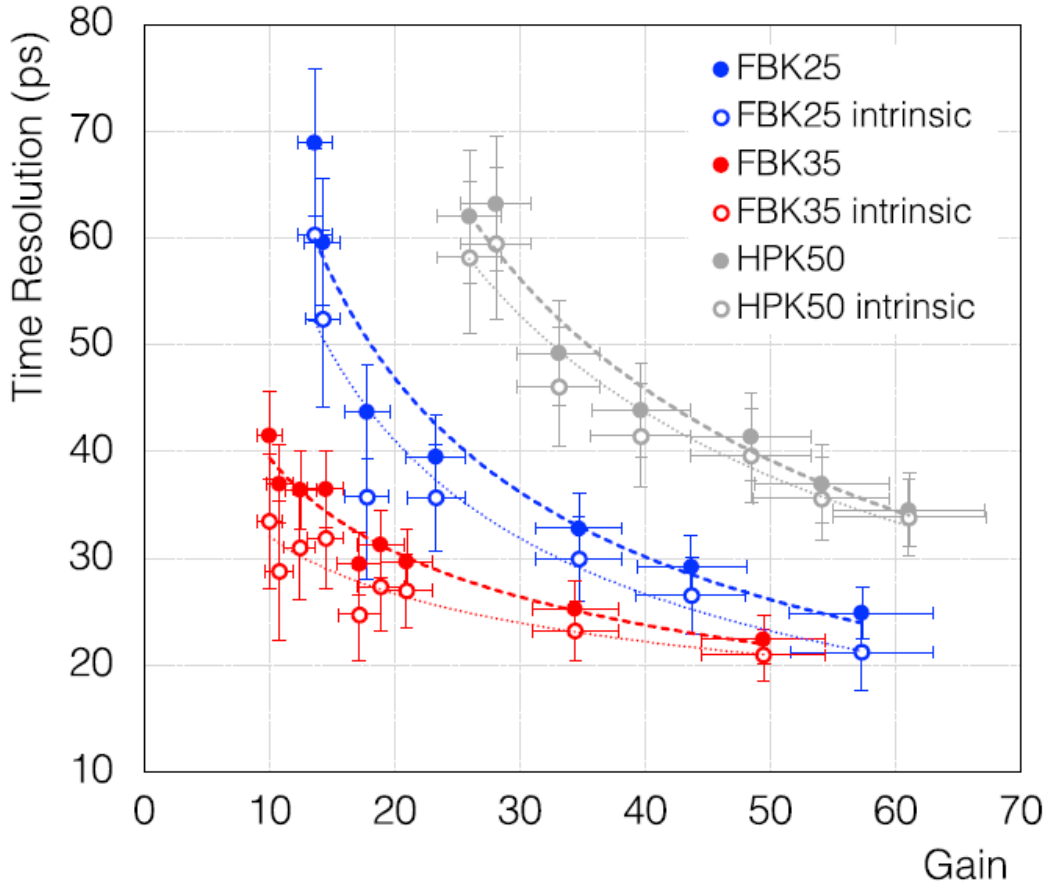
- Landau fluctuations: with 25um thickness the **intrinsic time resolution** for MIPs is ~20ps

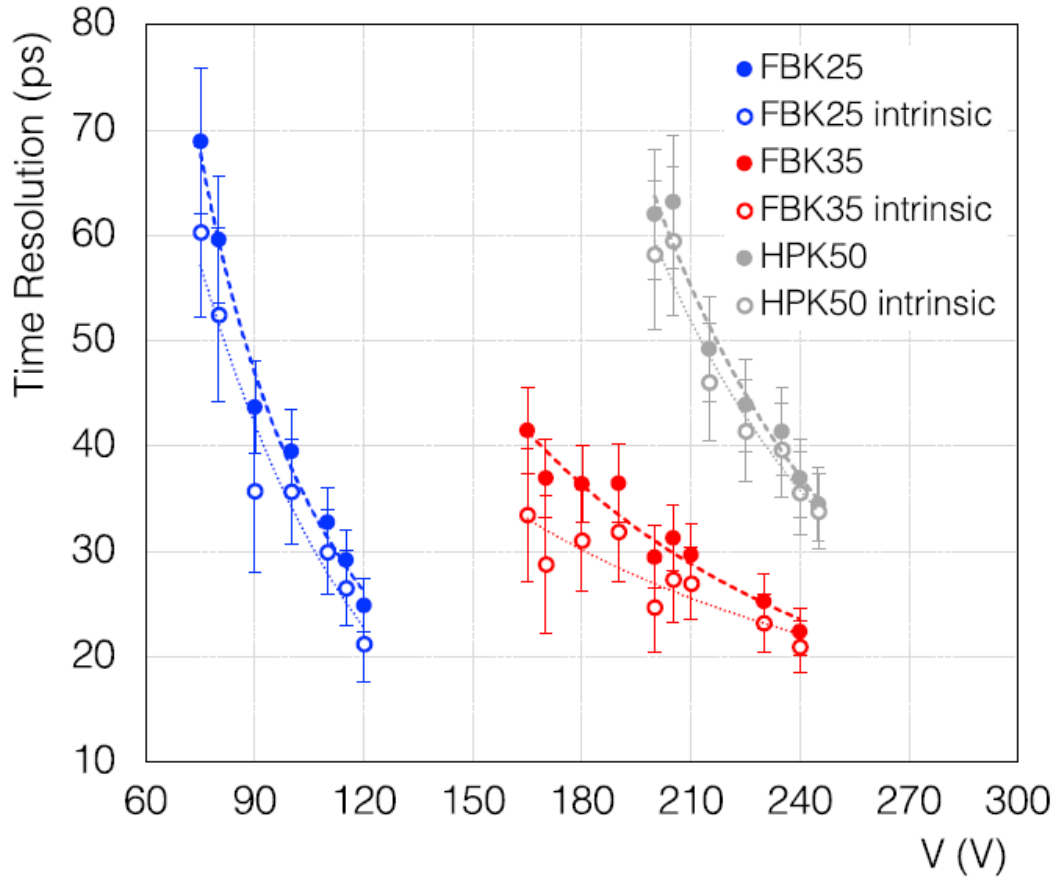


F. Carnesecchi – ALICE simulations
Landau noise for MIPs in LGADs

Thin LGADs – beam test

- Measurements on thin LGADs confirm the predicted time resolution
- Thin LGADs produced by several manufacturers are available

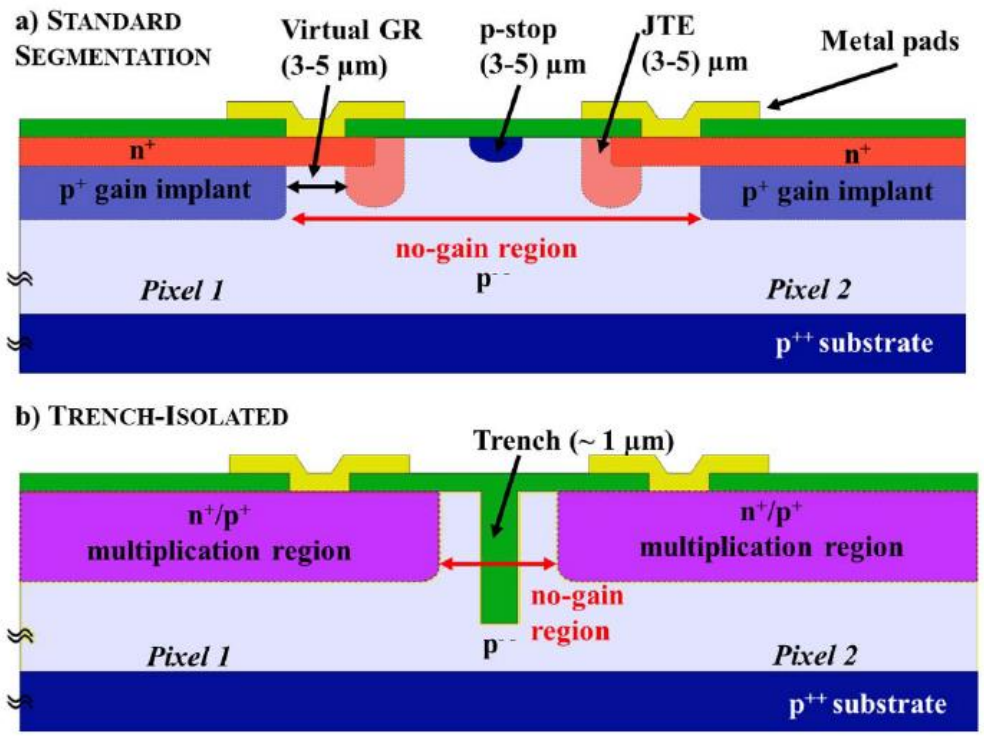




F. Carnesecchi et al., Eur. Phys. J. Plus (2023) 138:99

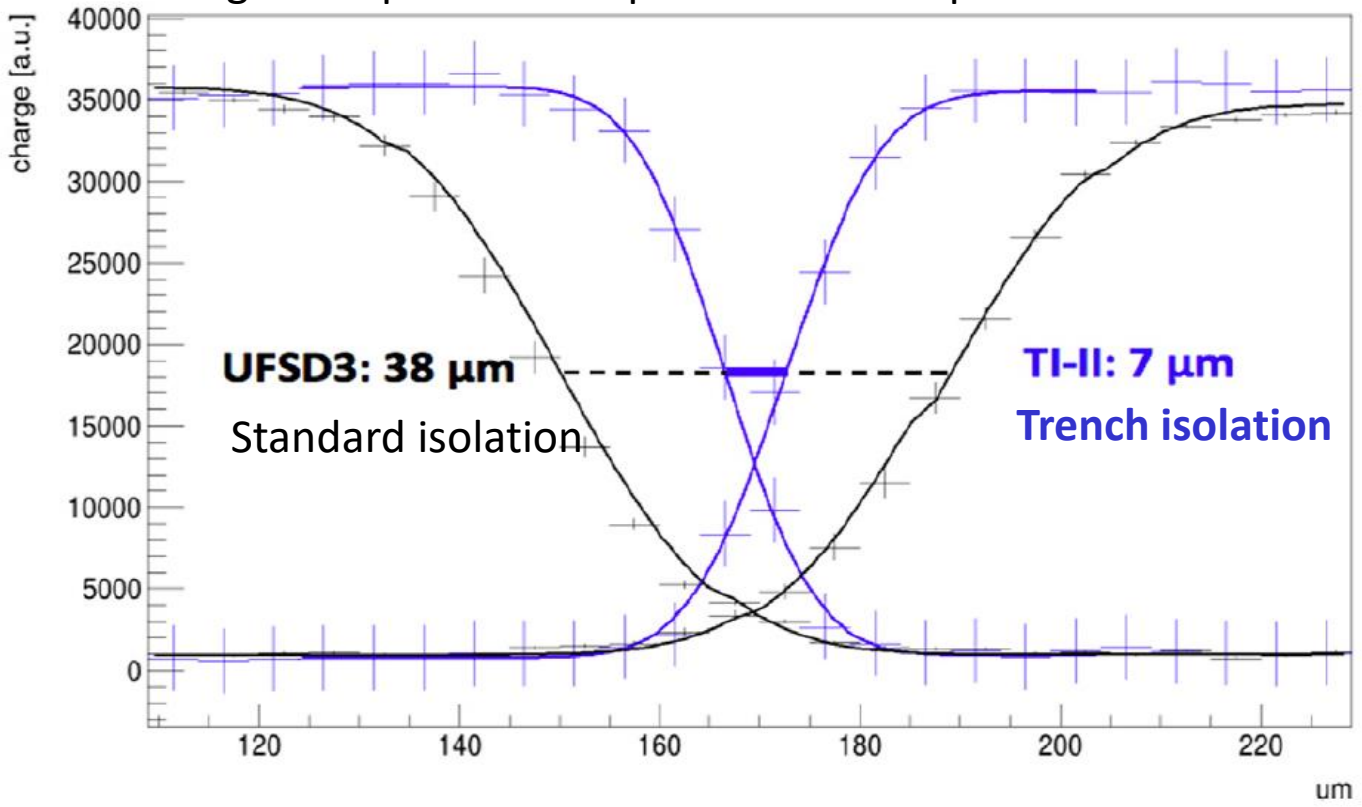
Reducing the dead area in LGADs: Trench Isolation

N-deep ring replaced with a trench: the no-gain area is reduced



G. Paternoster et al., IEEE Electron Dev. Lett., Vol. 41, No. 6, June 2020

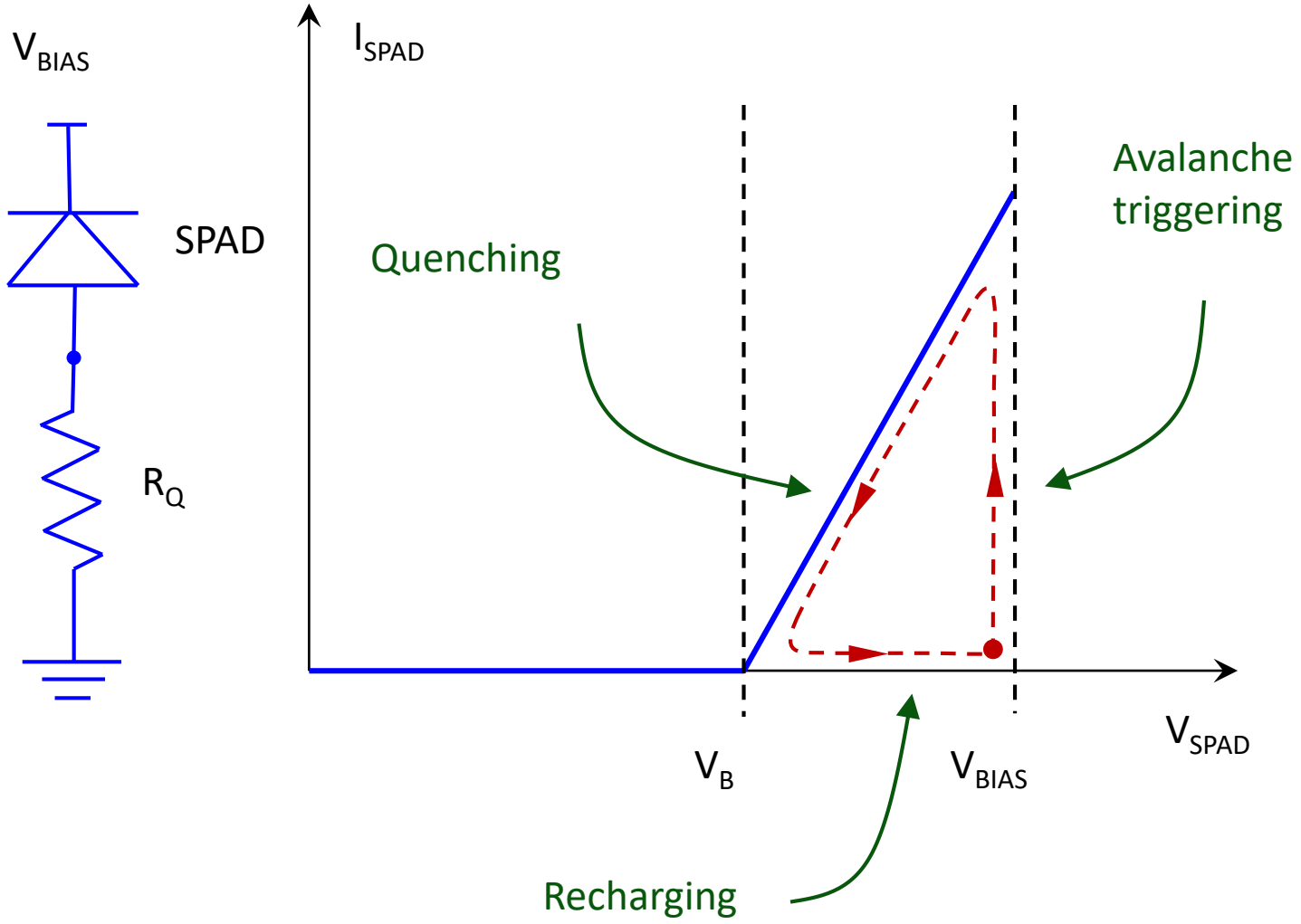
Signal amplitude with pulsed laser – top side illumination



R. Arcidiacono et al., NIMA 978 (2020) 164375

Single-Photon Avalanche Diodes (SPADs) and SiPMs: operation

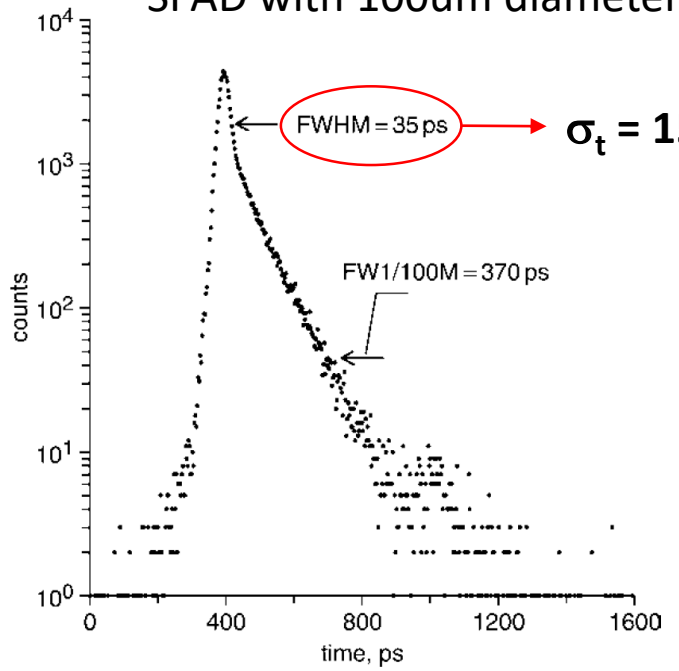
- Triggered (Geiger-mode) operation
- Available devices designed for photon counting and timing
- The best devices have a photon timing resolution σ_t < 20ps
- Dead time ~10 - 100ns
- High dark count rate:
  20 - 200 kHz/mm^2 at room temperature



Large Si SPADs: SoA photon timing resolution

- **Thin active region (a few μm)**, saturated drift velocity, response free from diffusion tails → Dedicated fabrication process
- Homogeneous electric field: circular area
- Low threshold: resolution independent from size

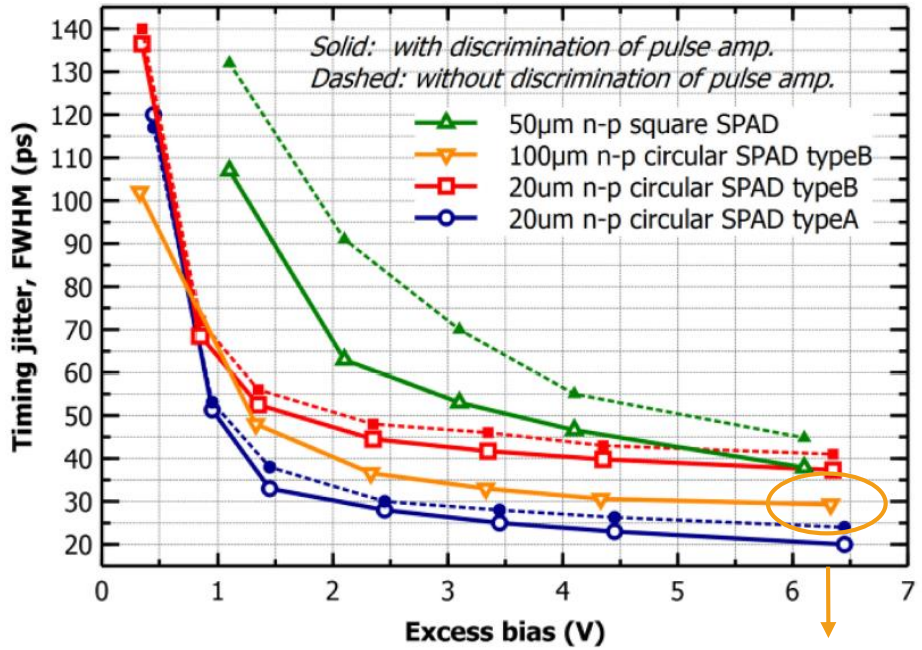
SPAD with 100um diameter at PoliMI



σ_t = 15ps

A. Gulinatti et al., Electronics Letters, Vol. 41 No. 5, 2005

SPAD with 100um diameter produced at FBK



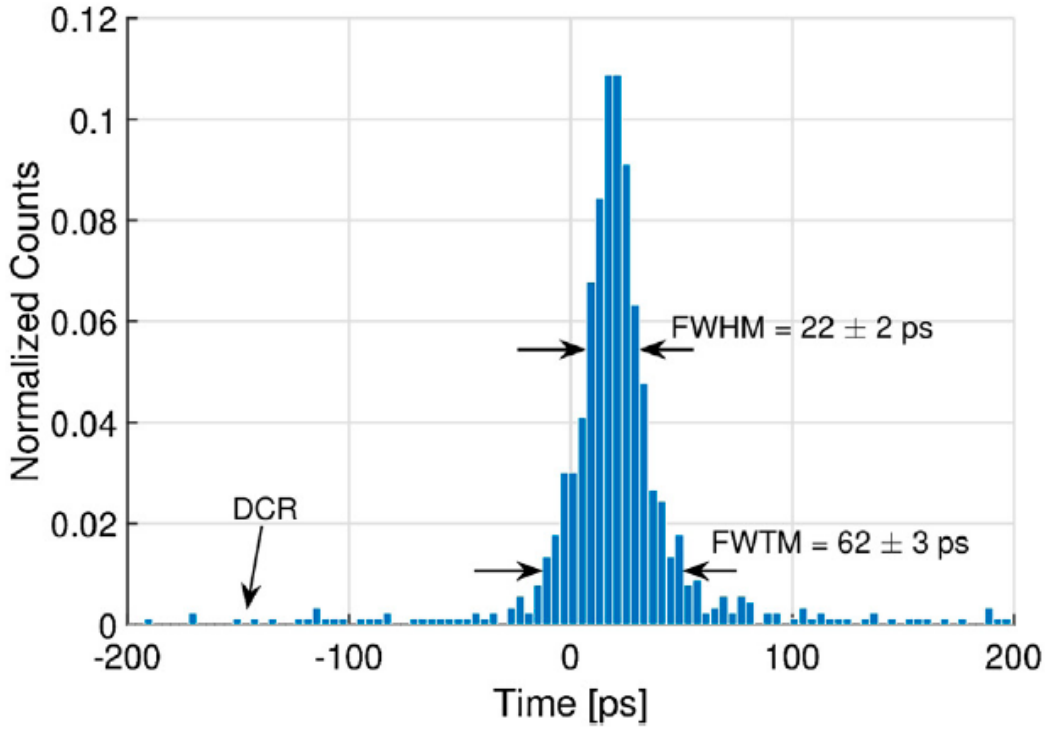
F. Acerbi et al., IEEE J. Selected Topics Quantum Electron., Vol. 20, No. 6, 2014

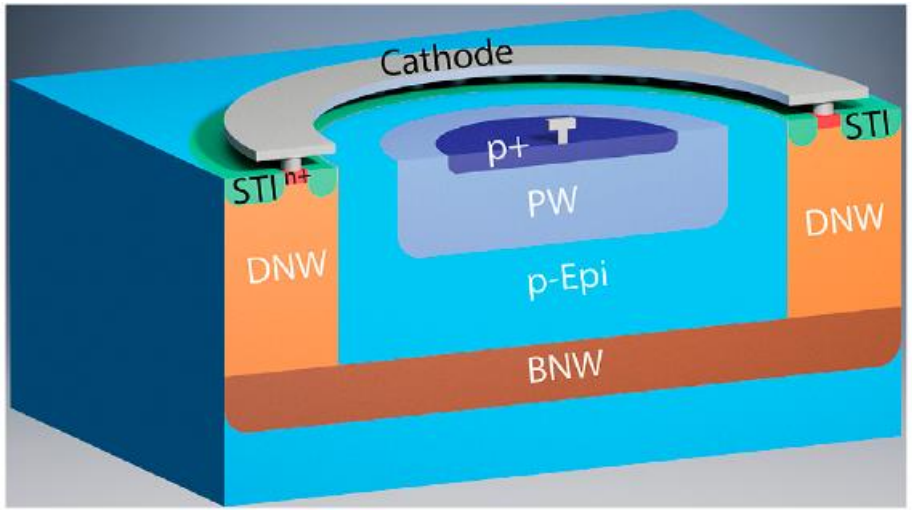
σ_t = 12.8ps

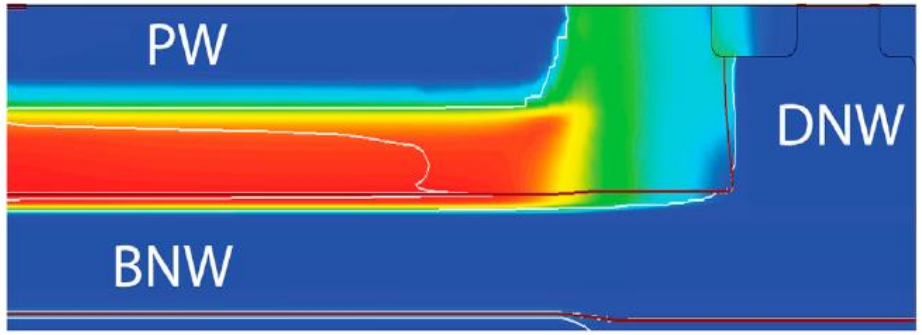
Si SPADs: timing resolution with charged particles

- SPADs with very uniform electric field in SiGe process
- Very fast amplifier
- Sub-10ps coincidence timing resolution for MIPs

2 aligned SPADs in coincidence
FWHM = 22ps, $\sigma_{single} = 9.4ps$ $\sigma_{single} = 6.6ps$



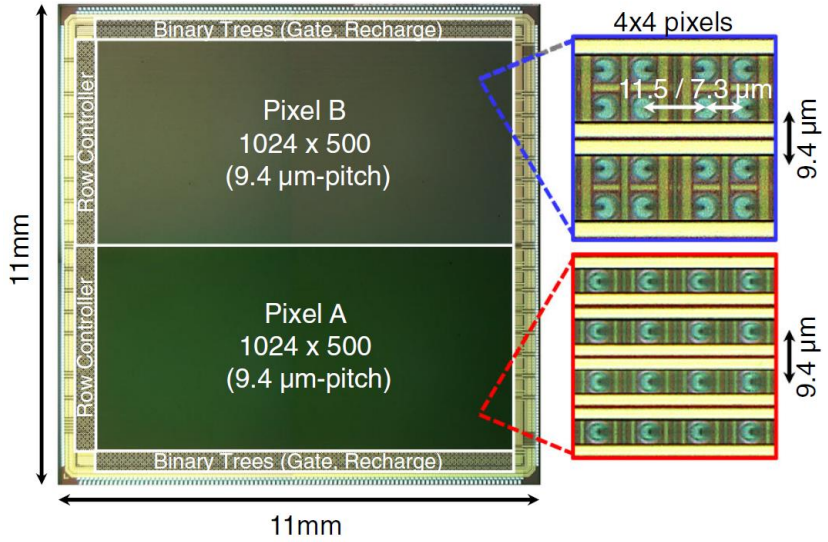




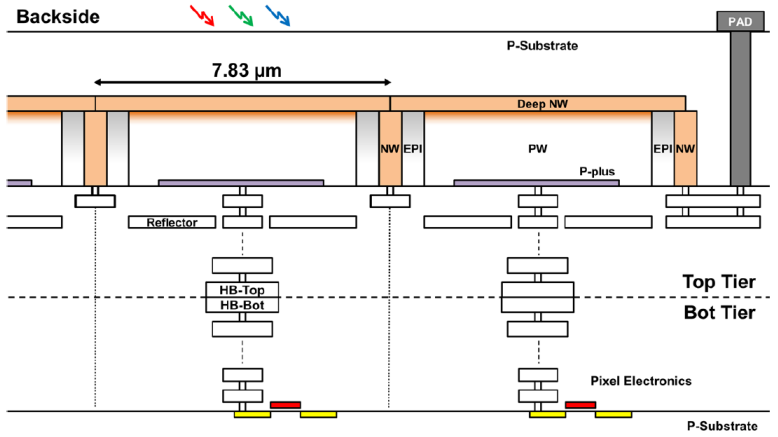
Gramuglia F, et al. 2022, Front. Phys. 10:849237.
doi: 10.3389/fphy.2022.849237

Monolithic and hybrid SPAD arrays

- Many designs demonstrated, up to 3.2Mpixel (Canon)
- Granularity: down to a few μm
- **SPAD arrays with 3D-stacked electronics** demonstrated (STM, Canon, Sony)
- A few demonstrations of direct particle detection in SPADs/SiPMs
- **Weakness: low radiation hardness**
  DCR increases considerably at fluences
  > 10^{10}- 10^{11} 1MeVn_{eq}/cm^2



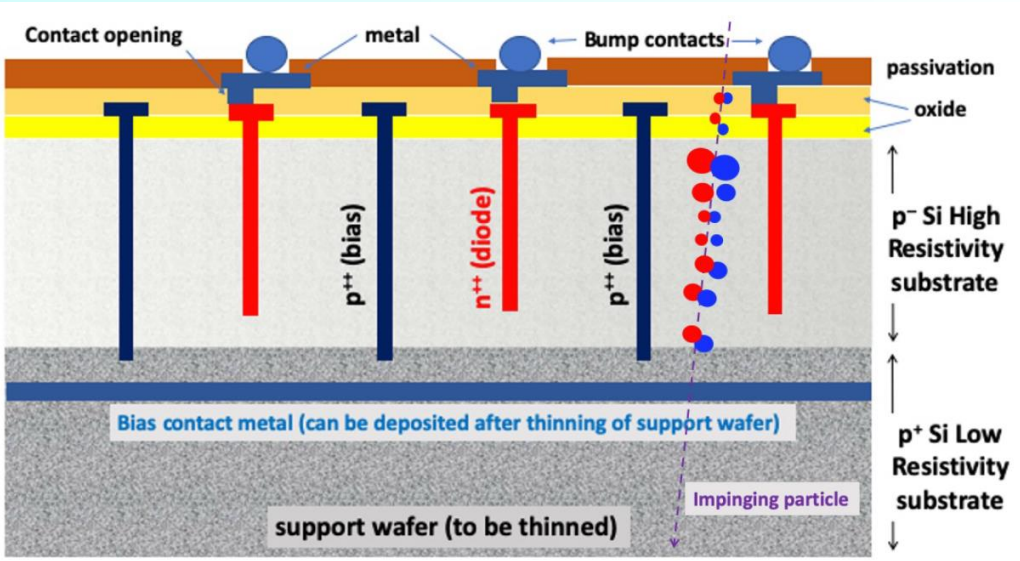
K. Morimoto et al., Optica, 7, 4, 346-354 (2020);

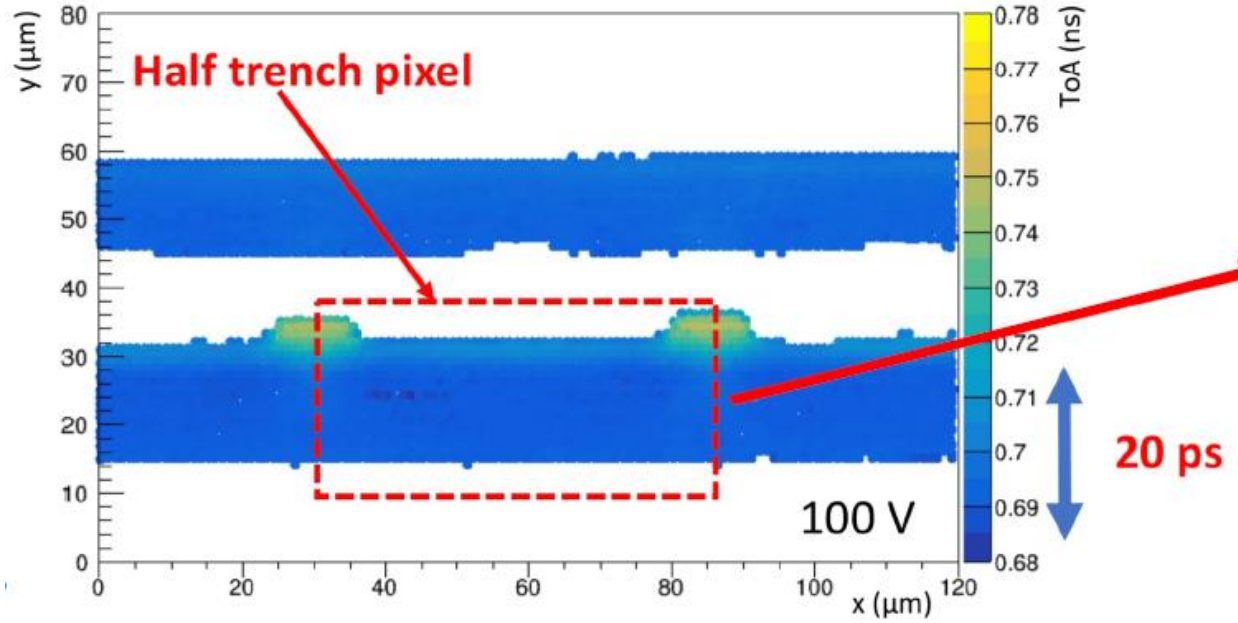


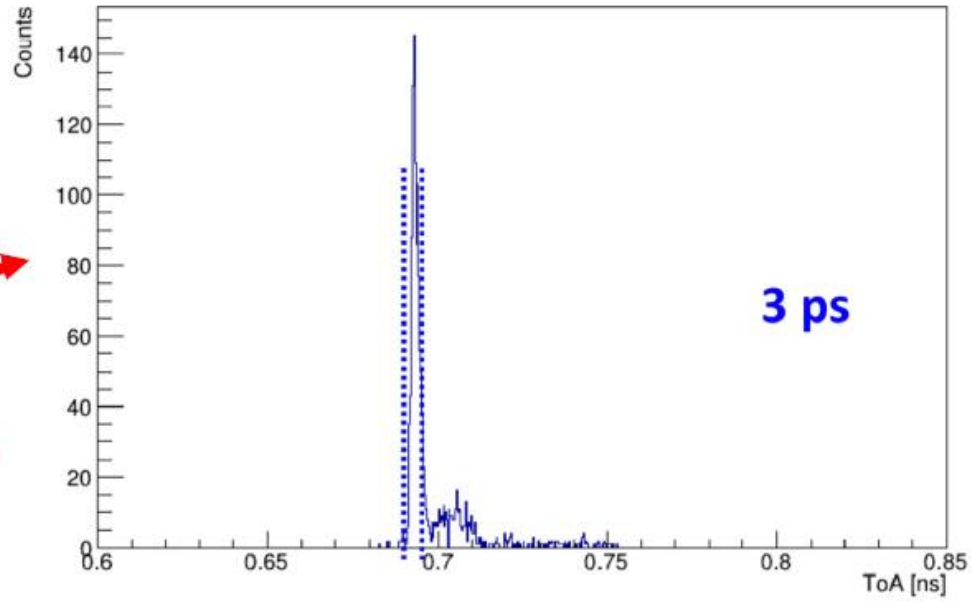
T. Al Abbas et al., IEEE IEDM 2016

Timing with 3D detectors: TimeSPOT

- **Thick active volume** but short drift length: combines large signal and large slope
- Trench geometry (**uniform electric field**): very narrow Time of Arrival distribution



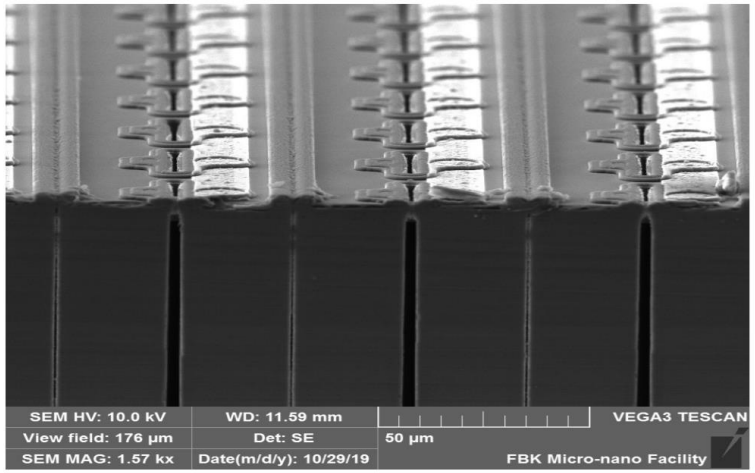


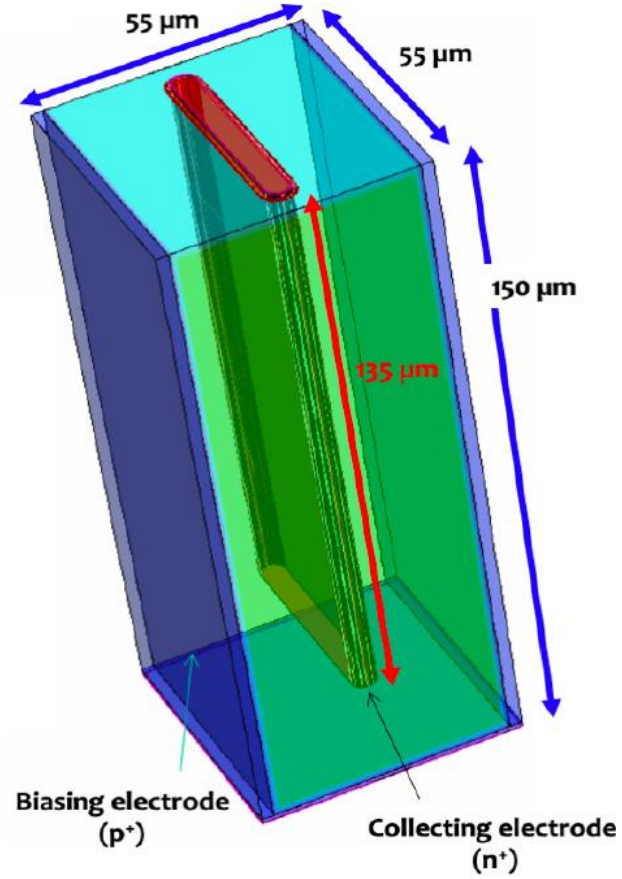


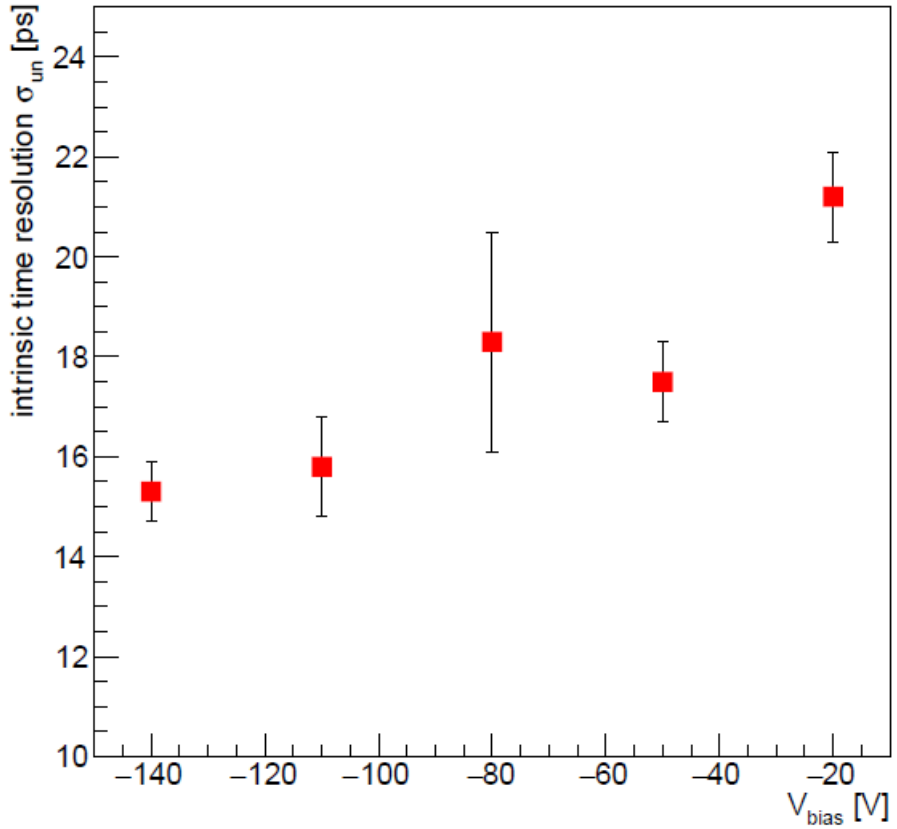
A. Lai, Vertex 2021

Timing with 3D detectors: TimeSPOT

- Trench distance: ~20μm
  saturated velocity v_{sat} :
  $t_{coll} = D/v_{sat} \sim 200ps$
- Weakness:
  complex fabrication process,
  mechanical stability of
  wafers (yield)







L. Anderlini et al 2020 JINST 15 P09029

Timing with MAPS: challenges and opportunities

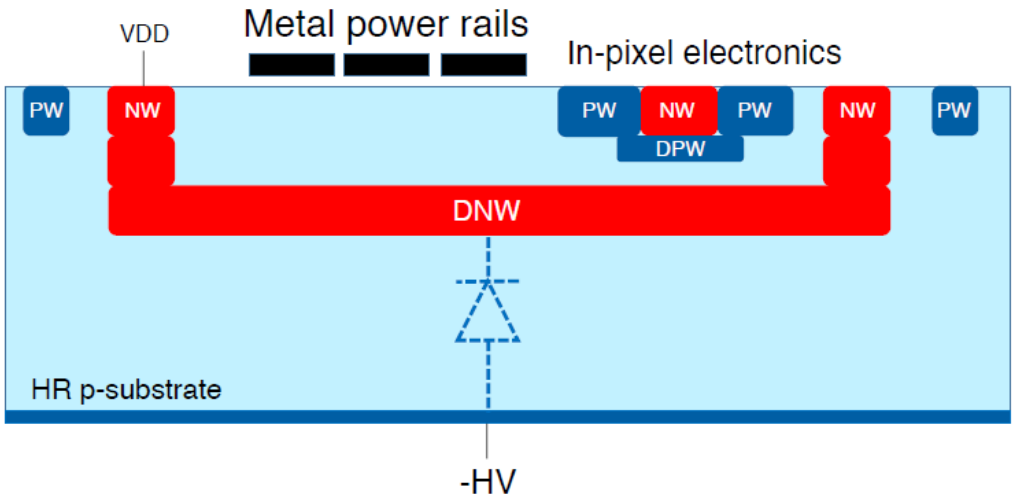
- **Advantages:**
  - Potentially **100% efficiency**
  - Excellent **radiation hardness** demonstrated for several processes
  - **Cost**-effectiveness

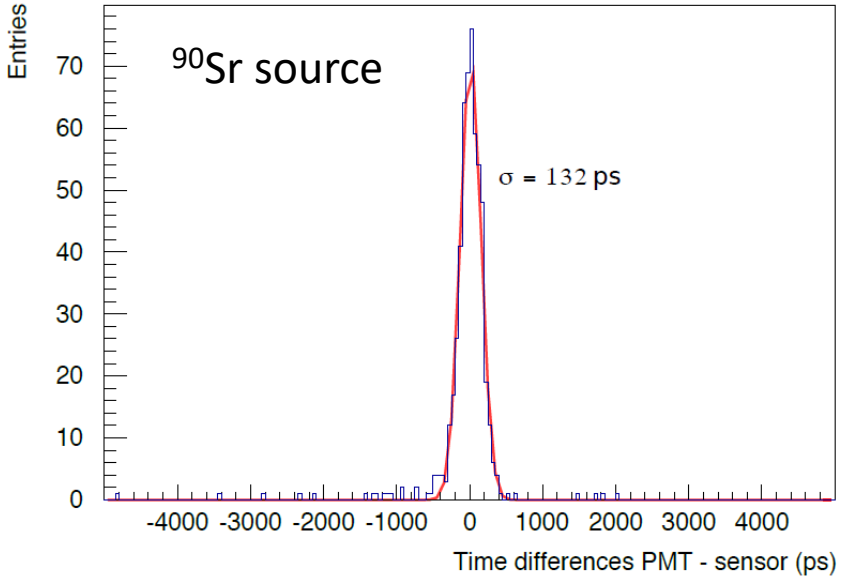
- **Challenges:**
  - Fast collection (100s of ps), uniform field and low noise at the same time
  - Low **jitter** with acceptable **power** consumption

CMOS with large collection electrode for timing: CACTUS

- Deep nwell collection diode
- FE electronics inside the pixel
- Fast and uniform charge collection
- Substrate thickness: 200μm, pixel size: 0.5 – 1 mm^2
- Pixel capacitance: 1 – 1.5 pF

- Noise limited by the large diode capacitance

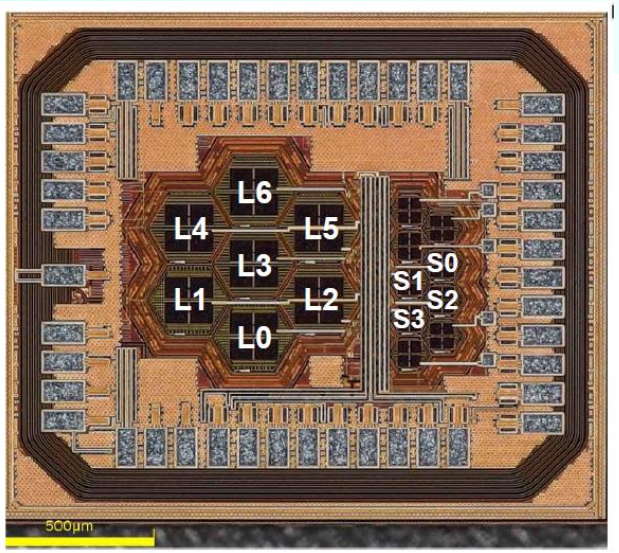


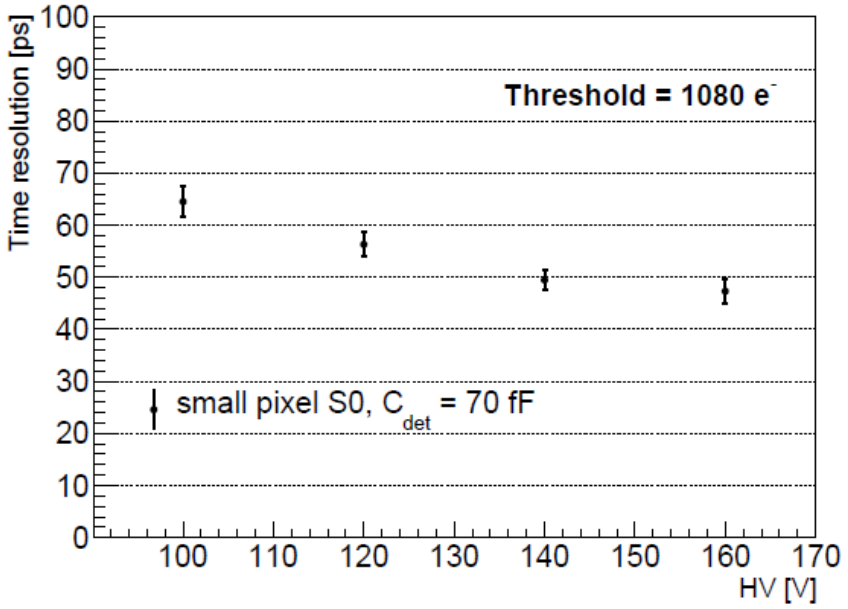


Y. Degerli et al., 2020 JINST 15 P06011

SiGe approach

- SiGe process modified (HR substrate) for the integration of planar silicon detector
- High speed – low noise on-chip SiGe preamplifiers placed outside the pixels
- Hexagonal pixels with 130 and 75 μm side
- Depletion depth: 26μm at -140V
- Large detector capacitance (70 - 220 fF)
- Nearly 100% collection efficiency
- ~ 50ps timing resolution demonstrated with ^{90}Sr source

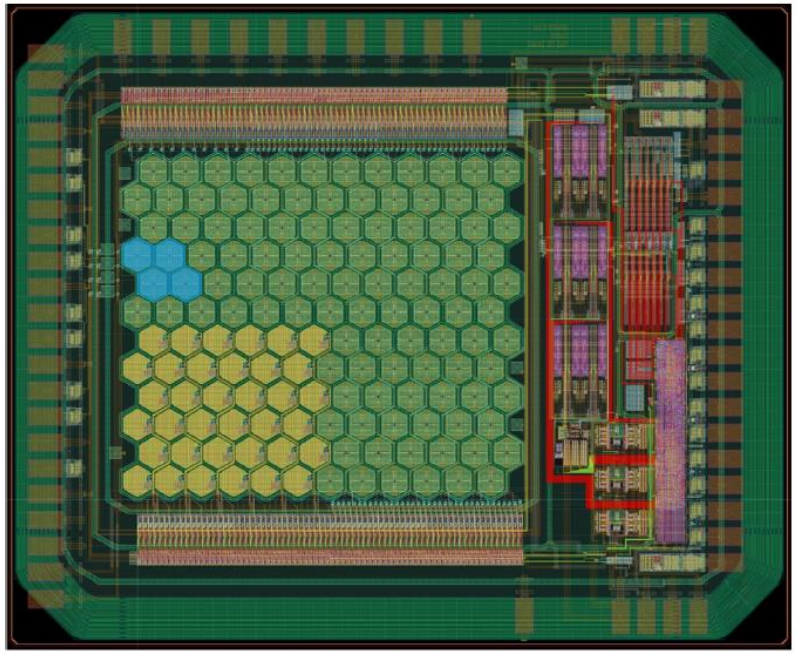




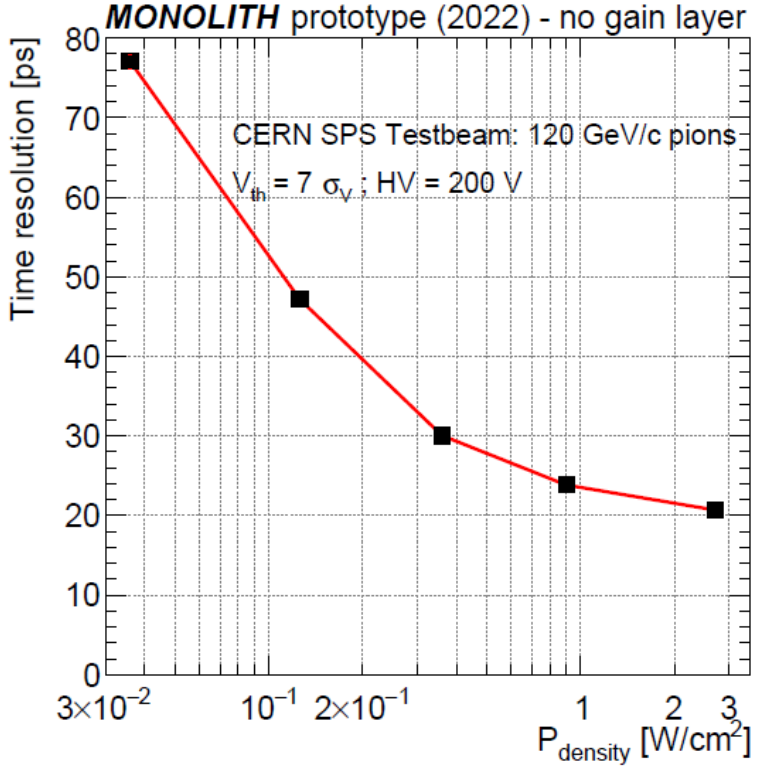
G. Iacobucci et al., 2019 JINST 14 P11008

SiGe approach: Monolith chip

- Epitaxial silicon with 50 μm thickness
- 100 μm pixel pitch
- On-chip amplifiers with variable optical power
- 20ps time resolution can be reached at high power densities

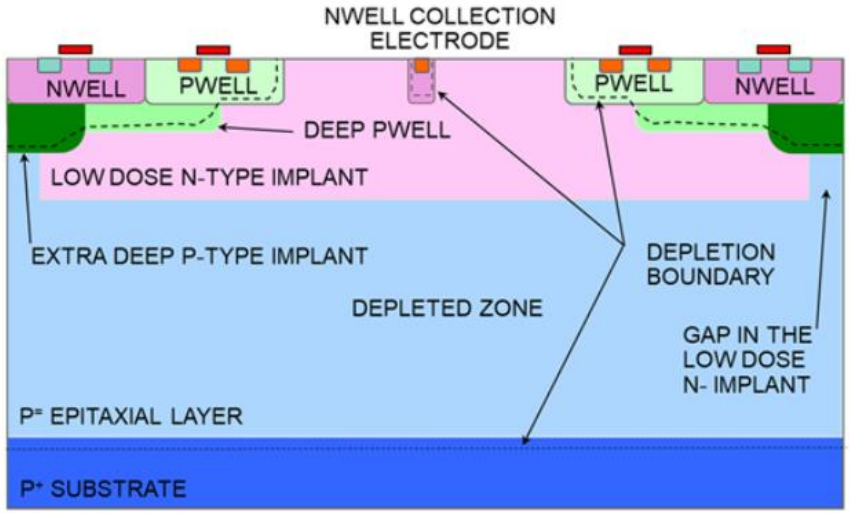


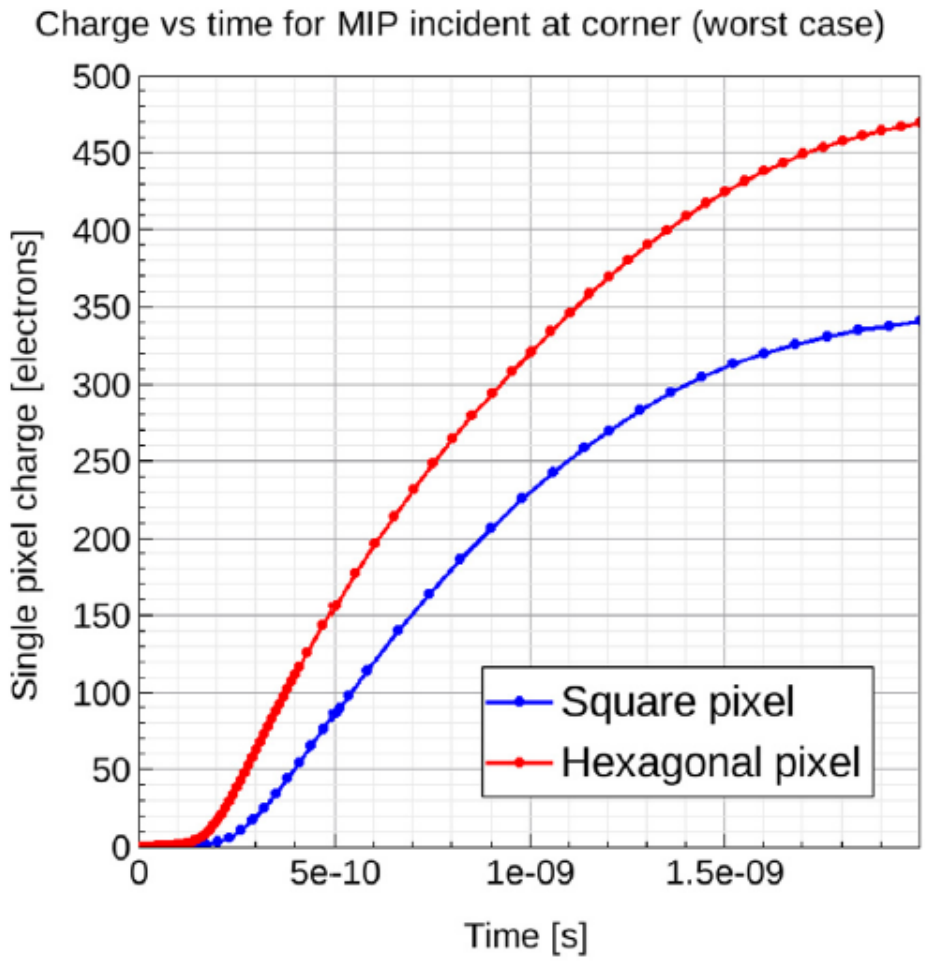
S. Zambito et al 2023 JINST 18 P03047



Fastpix

- Evolution of the MAPS developed for the ALICE tracker: full depletion + speeding up the electron lateral drift
- Test chip with small pixel pitches (10 - 20 μm)
- Very low electrode capacitance (< 1fF)
- Expected jitter (electronics): 20ps @ Q_{in} =1000 e^-

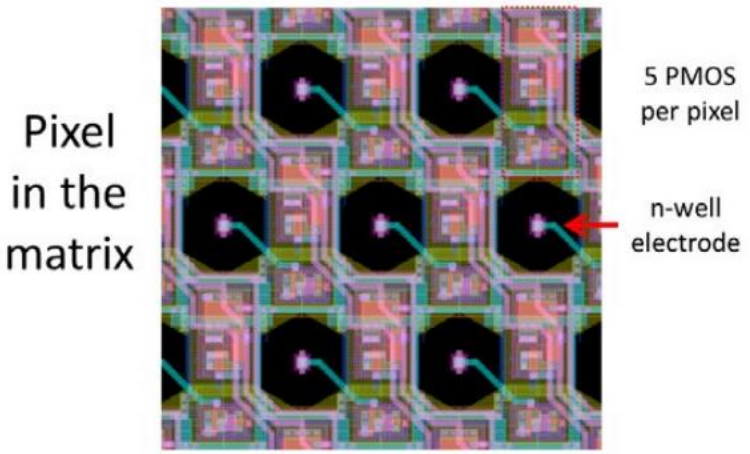


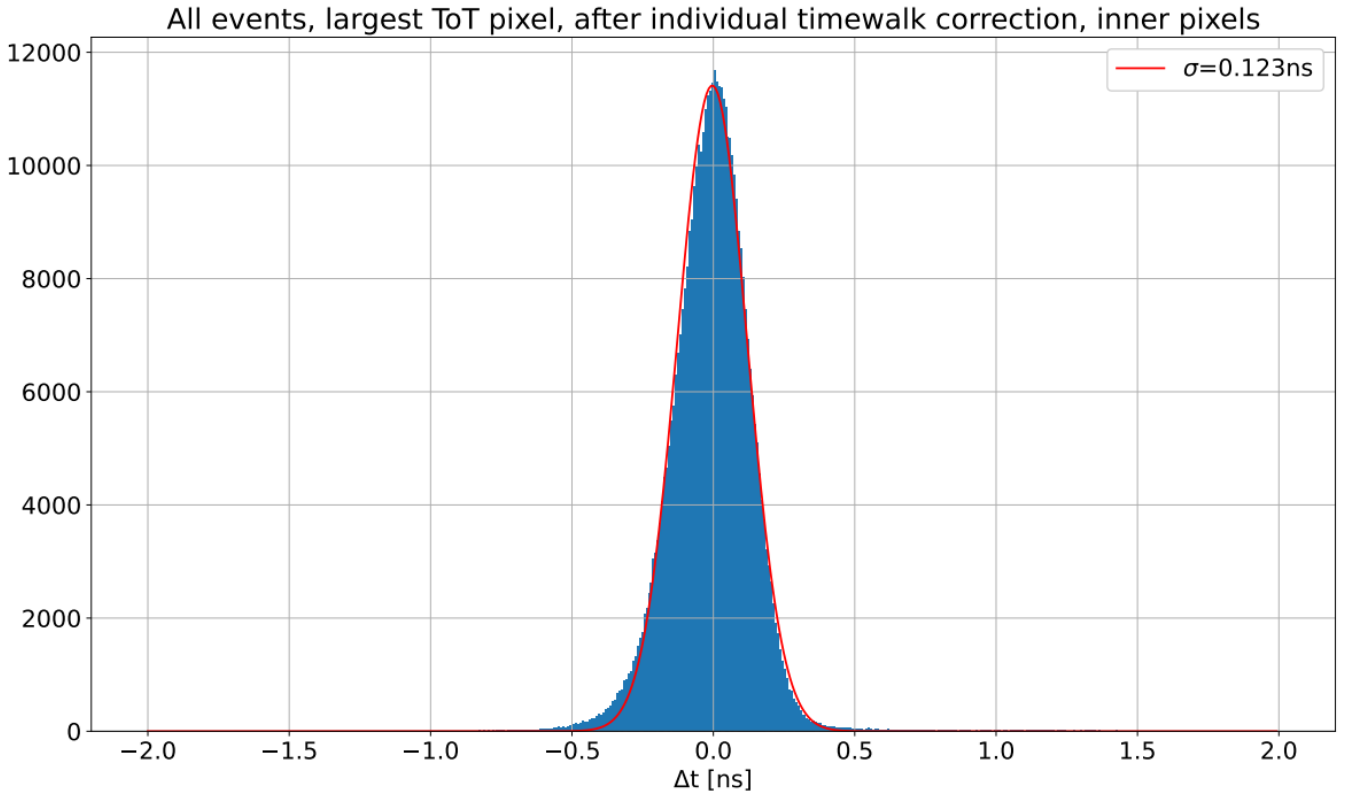


T. Kugathasan et al., Nucl. Inst. Meth. A Vol. 979, Nov. 2020

Fastpix – test beam results

- Time walk correction
- Pixel-by-pixel correction for best results
- 70e- threshold for 20μm and 50e- threshold for 10μm pixels





E. Buschmann et al., 2021

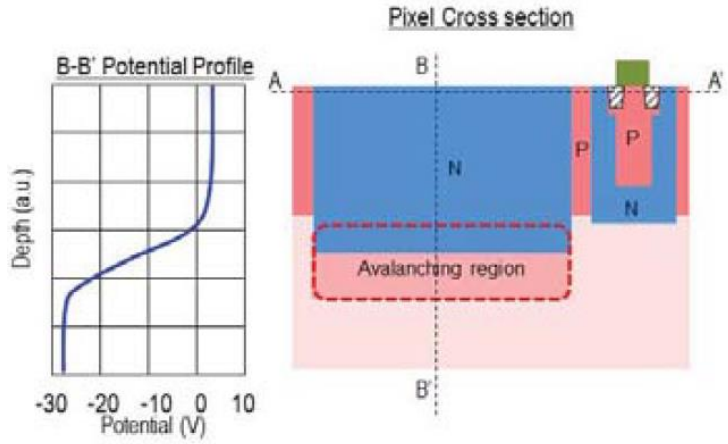
Test beam: timing resolution < 140 ps for both 10 and 20μm pitch

Monolithic avalanche detectors

Several recent examples of **avalanche gain integrated in CMOS** sensors:

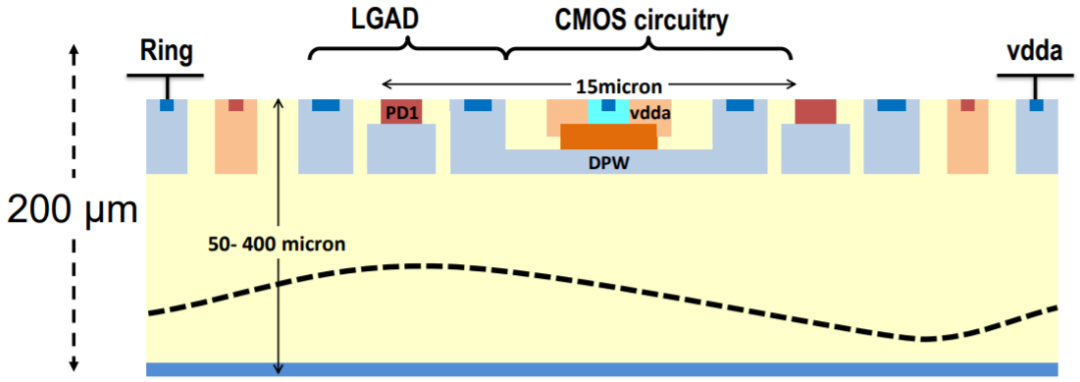
- The feasibility of structures designed for **photonics applications** can be verified for particle detection
- Foundries may be available to implement simple **process modifications**, needed to add gain to CMOS sensors

Fine-pitch avalanche pixels with 6um pitch (Panasonic)



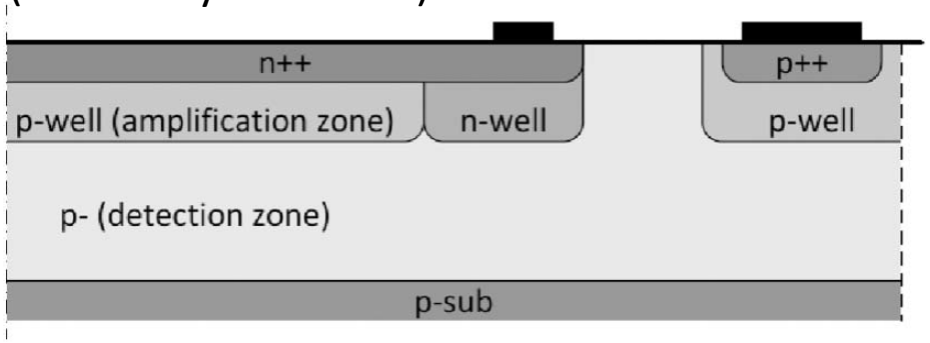
Y. Hirose et al., IEEE ISSCC 2019

LGADs on thick fully depleted substrates (Sensor Creations Inc.)



S. Lauxtermann et al., Pixel 2018, Taiwan

CMOS-integrated APDs with > 1GHz bandwidth (University of Vienna)

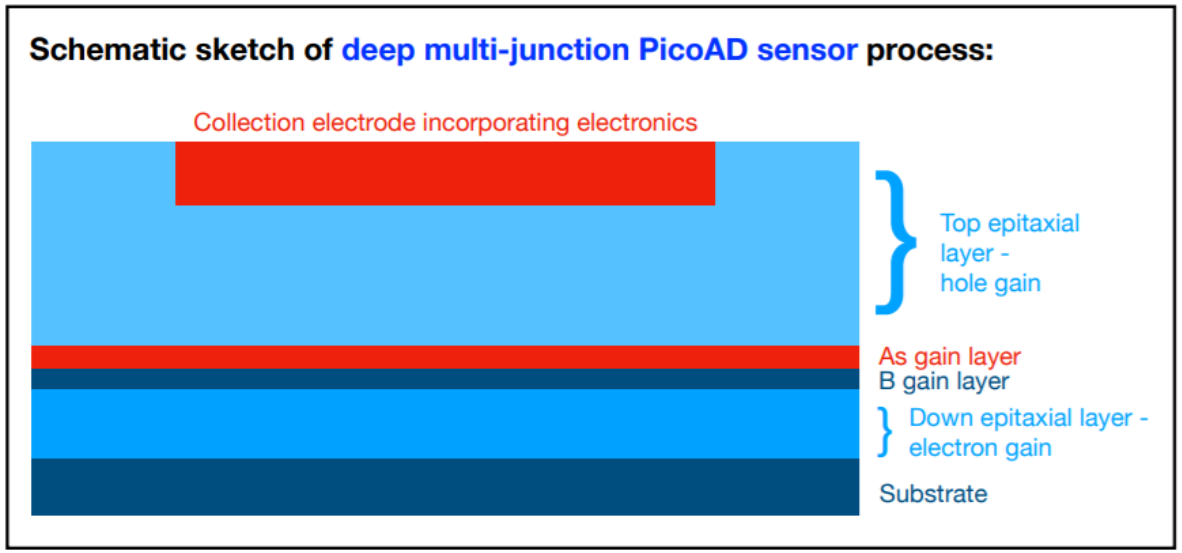


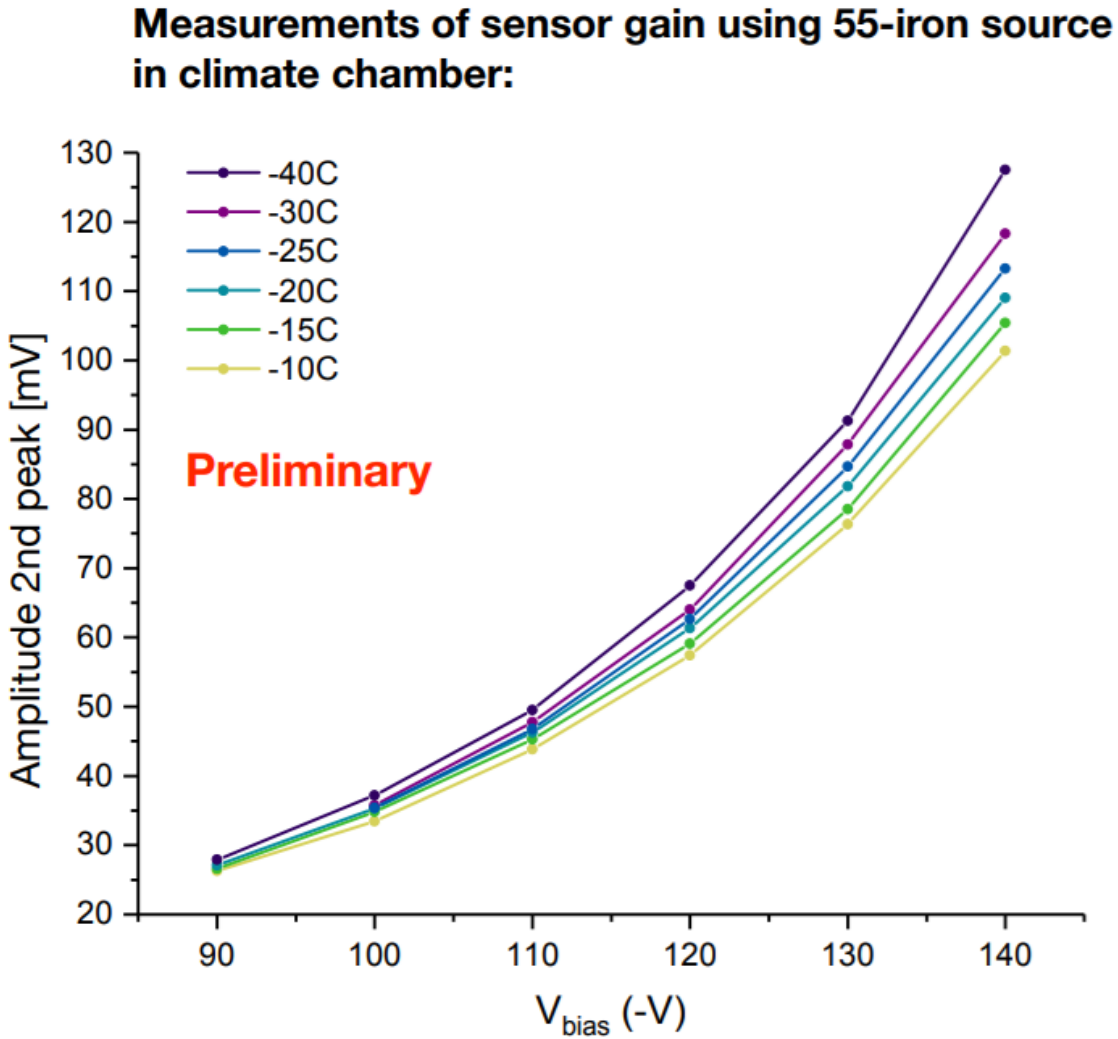
W. Gaberl et al., Opt. Lett., Vol. 39, No. 3, 2014

Monolithic sensors with gain @ University of Geneva

Avalanche gain in monolithic CMOS sensors:
may be the key for **combining very high resolution and acceptable power consumption**

Picosecond Avalanche Detector (PicoAD): EU Patent EP18207008.6

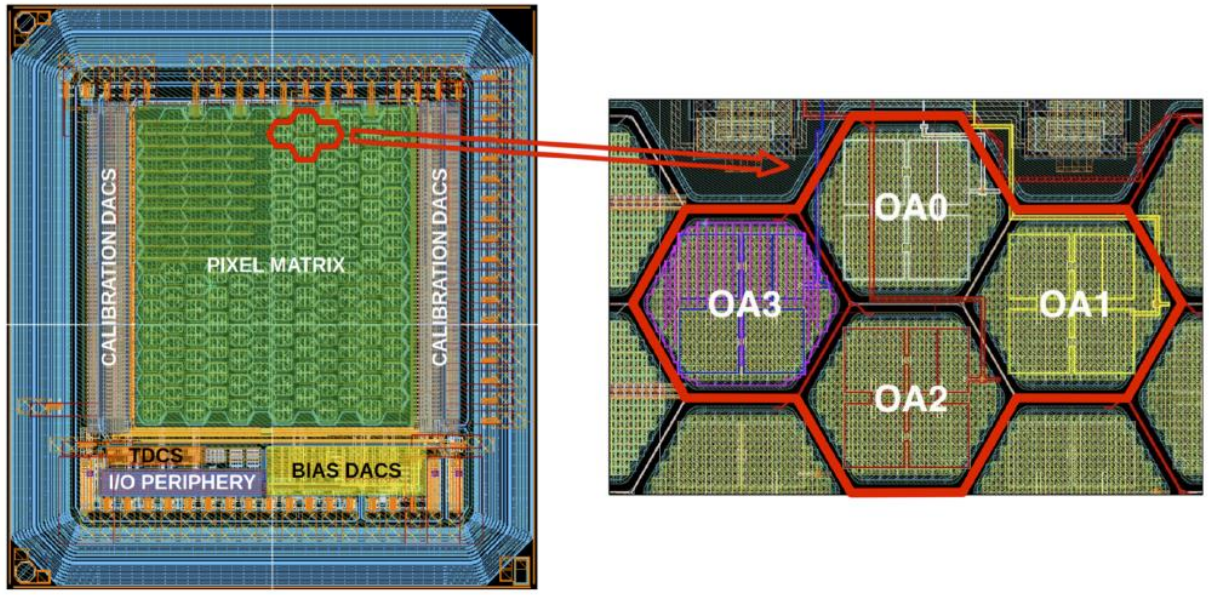


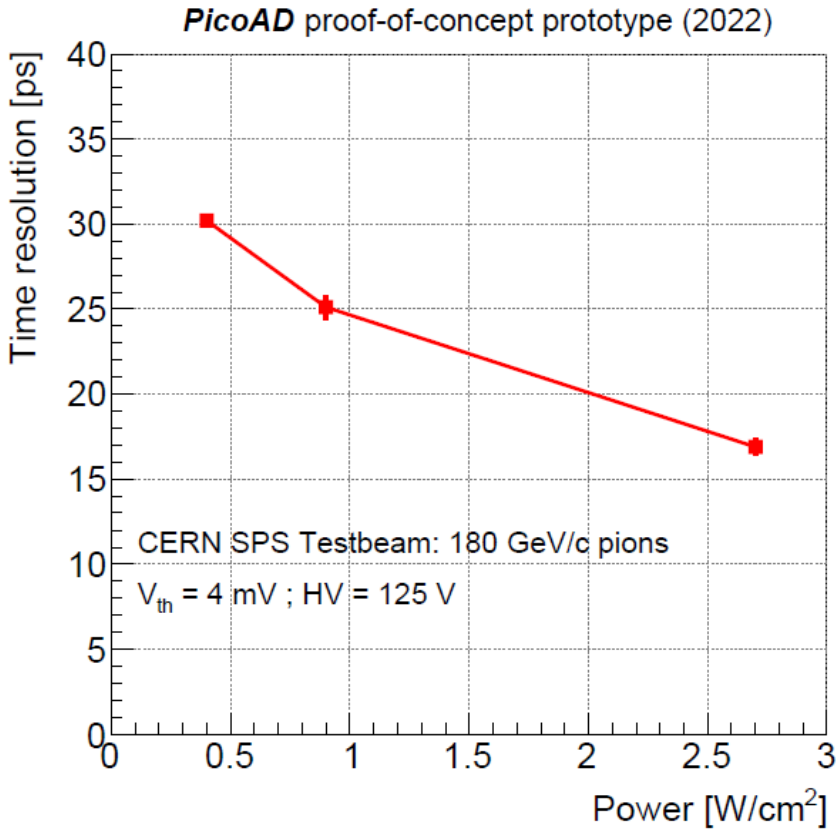


M. Munker et al., Vertex, September 2021

Monolithic sensors with gain @ University of Geneva

Test beam: time resolution of 30ps achieved with a power density < 0.5 W/cm^2

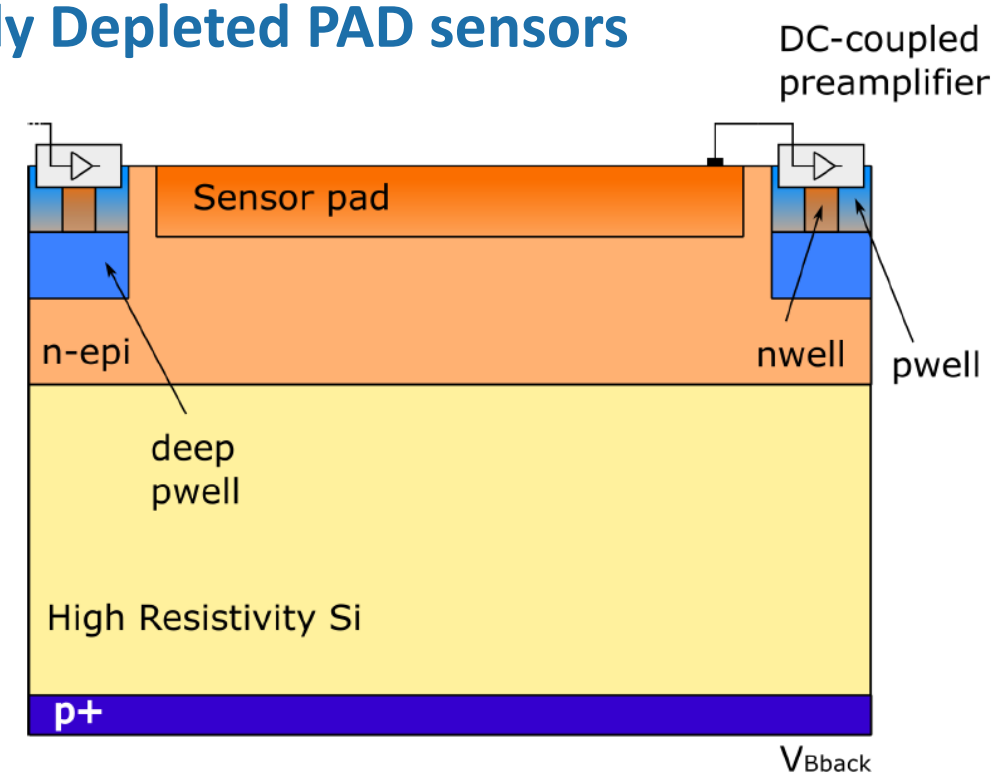




G. Iacobucci et al 2022 JINST 17 P10040

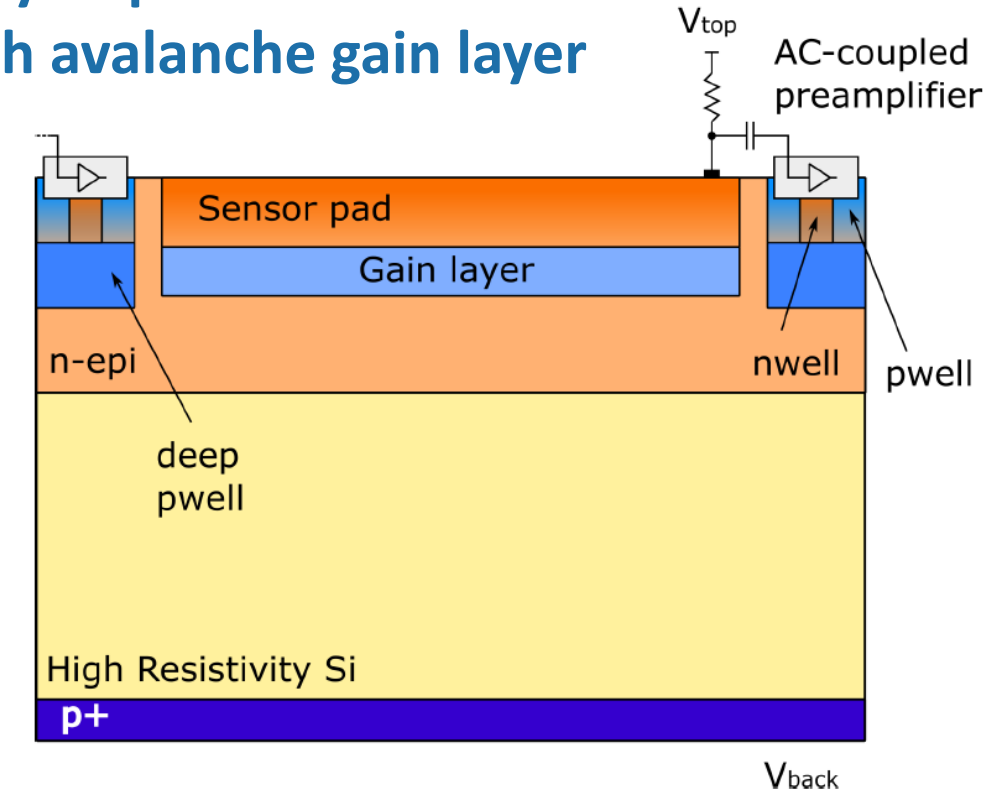
ARCADIA MAPS: gain add-on option

Fully Depleted PAD sensors



- Sensors can be biased at low voltage
- DC coupling with front-end amplifier is possible

Fully Depleted PAD sensors with avalanche gain layer

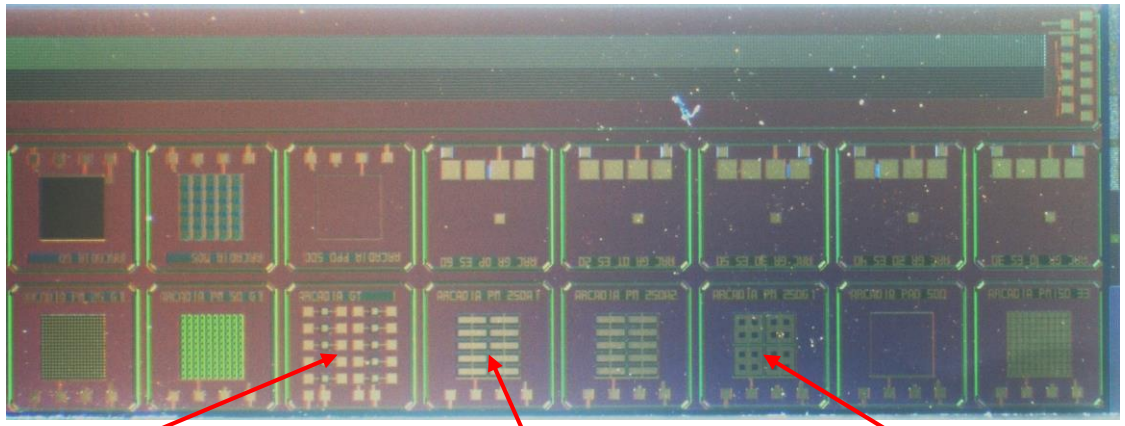


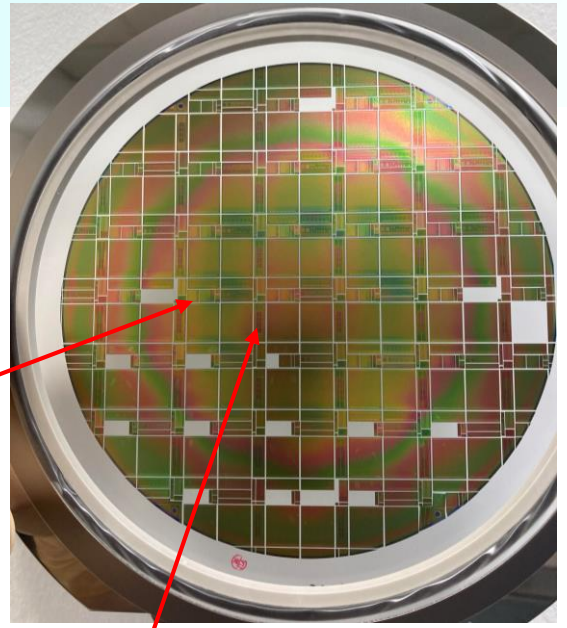
- High voltage is needed on the top side
- AC coupling of front-end amplifier is needed

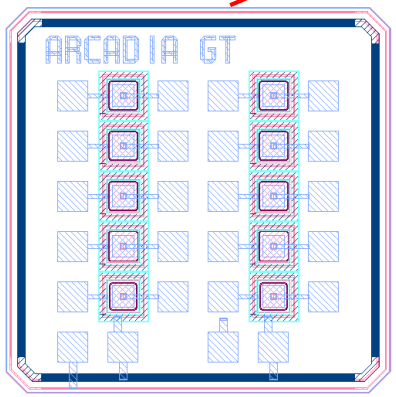
L. Pancheri, Proc. IEEE EUROCON 2023

Passive sensors with gain - test structures

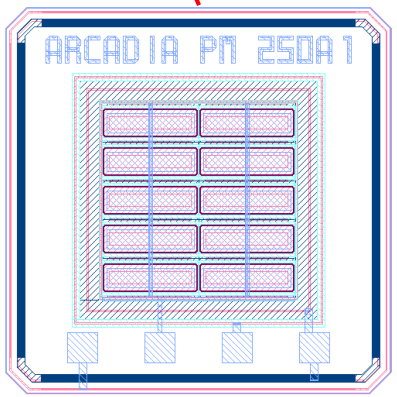
Monolithic test devices with gain included in the last **ARCADIA engineering run**



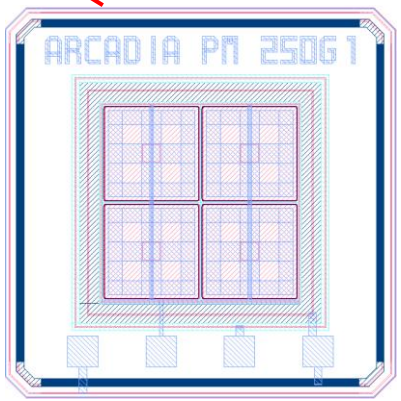




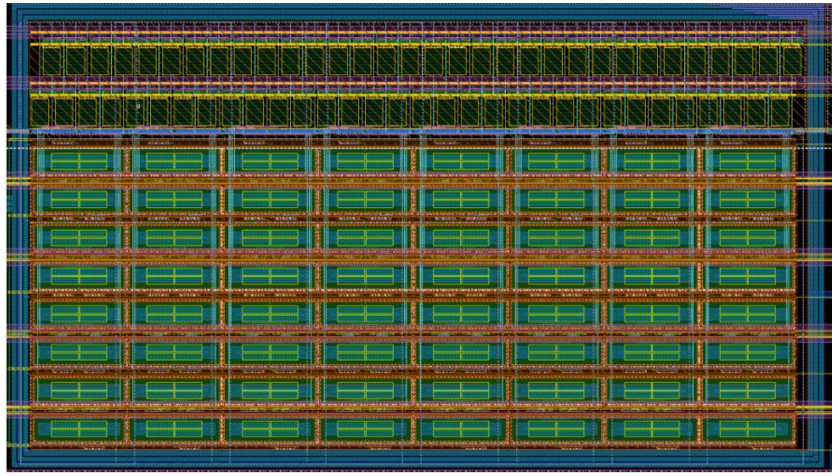
Devices with different terminations



Rectangular pad sensors



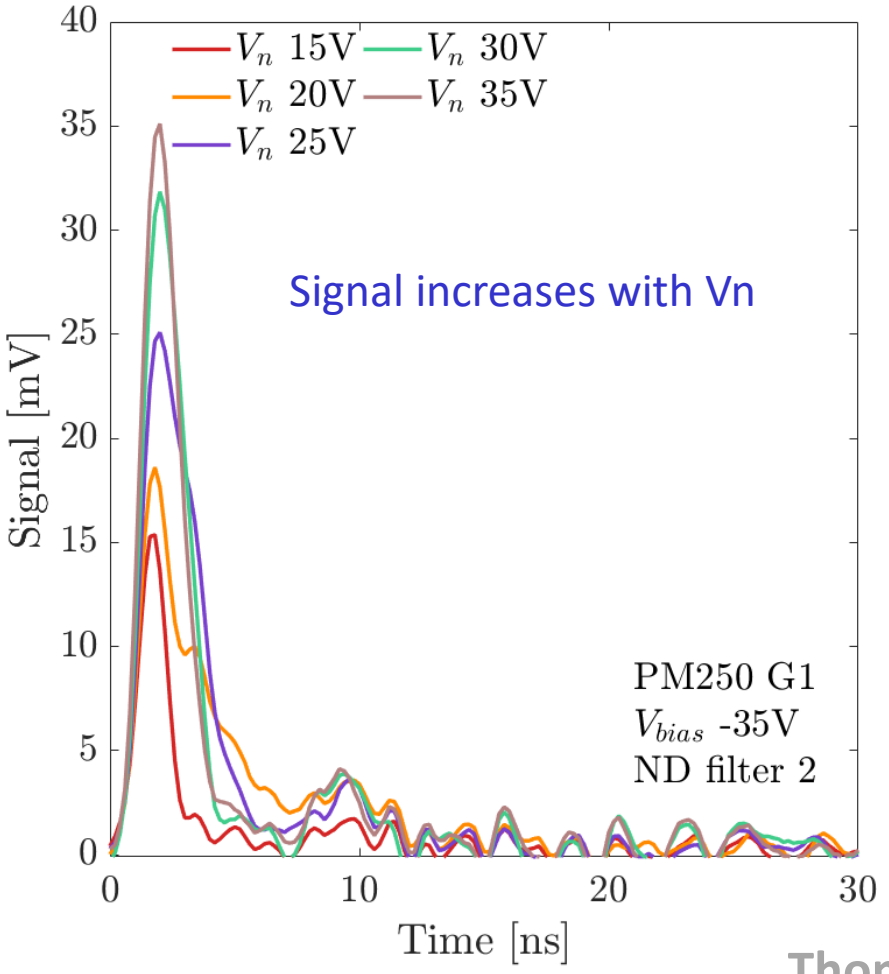
Square pad sensors



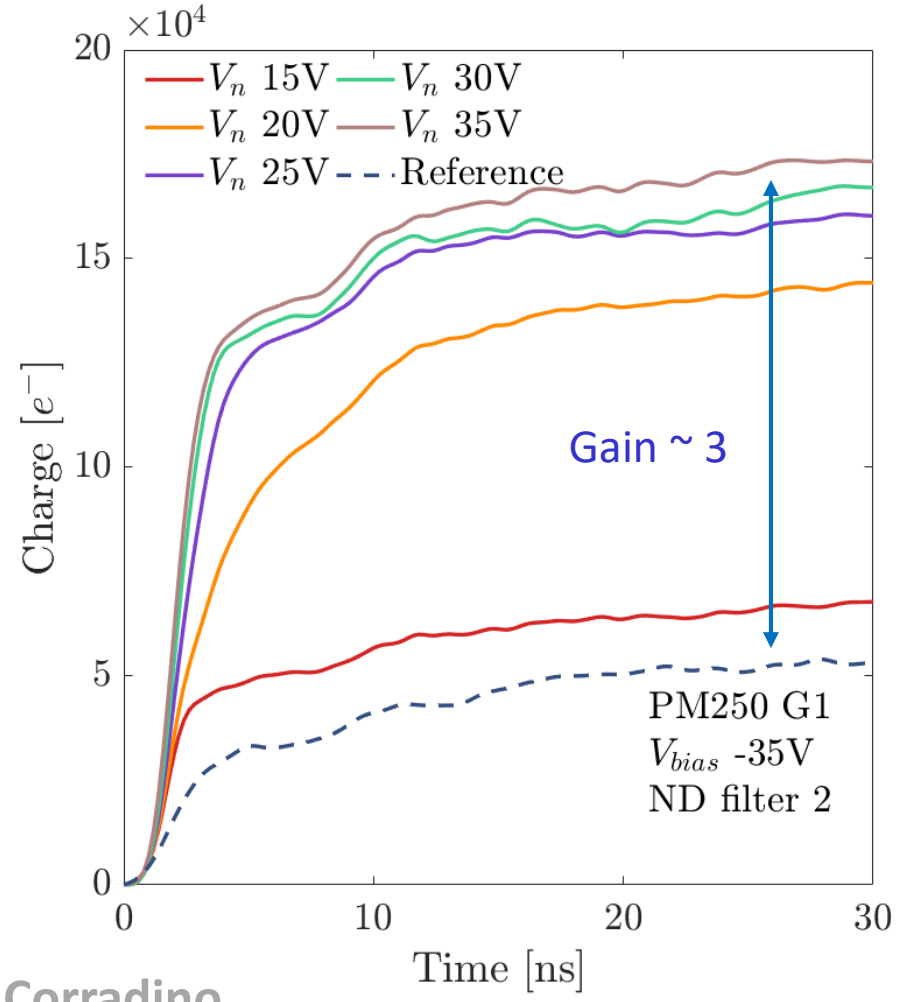
8x8 active pixel matrix

Optical signal with NIR pulsed laser

Sensors test structures:
effect of **Vtop** - Bottom-side illumination

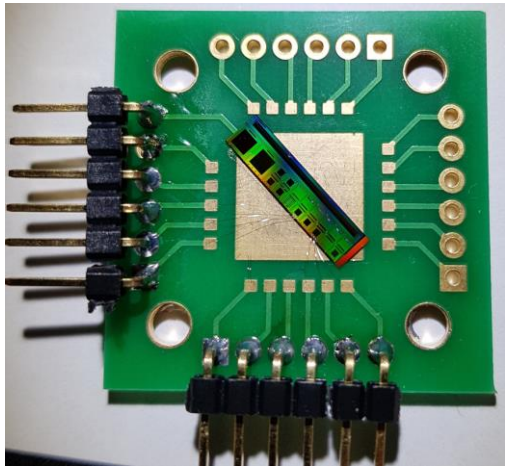


Test-beam with active pixels is on-going



Laser pulse width
< 100ps

Wavelength:
1060nm



Thomas Corradino

Conclusion

Depleted Monolithic active pixel sensors:

- Several versions providing valid cost-effective alternatives to hybrid sensors for tracking applications
- Scaling to smaller process nodes is not straightforward: custom substrates and implants are not always granted by foundries
- Meanwhile 3D integration technologies are evolving…

Picosecond timing applications - several **alternative possibilities** are under investigation:

- LGADs with hybrid readout
- Monolithic or hybrid SPADs/SiPMs
- Hybrid sensors with 3D electrodes
- Monolithic sensors with gain (or CMOS LGADs?)

Thank you