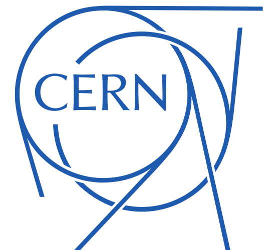
Tutorial on radiation issues in microelectronics

Days of Detection

Padova - 2023/10/23

G. Borghello
giulio.borghello@cern.ch



OUTLINE

- introduction (~ 2 min)

- cumulative effects
  - ionizing effects (total ionizing dose [TID])
    - basic mechanisms (~ 25 min)
    - TID effects in microelectronics for particle detectors (~ 25 min)

break! (5 min)

  - non-ionizing effects (displacement damage [DD]) (~ 5 min)

- stochastic effects (~ 25 min)
  - ionizing effects (single event effects [SEE])

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the impact of a single interaction may be almost negligible, but the damage accumulates over time leading to measurable effects

➢ the higher the radiation level, the greater the effects!

- stochastic effects
  - ionizing effects (single event effects [SEE])

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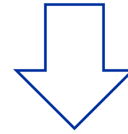
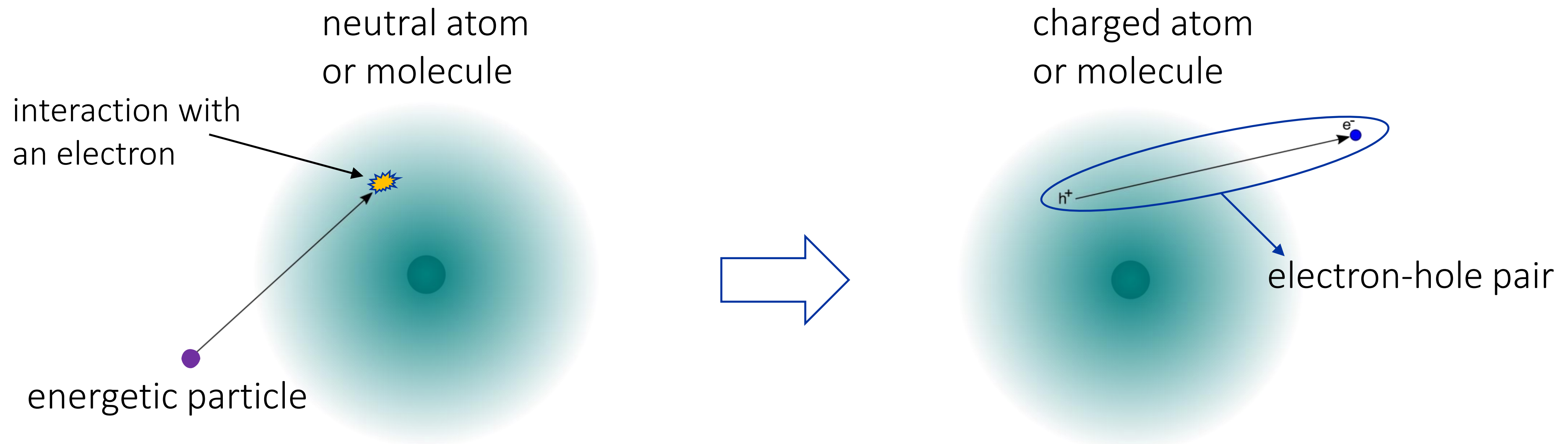
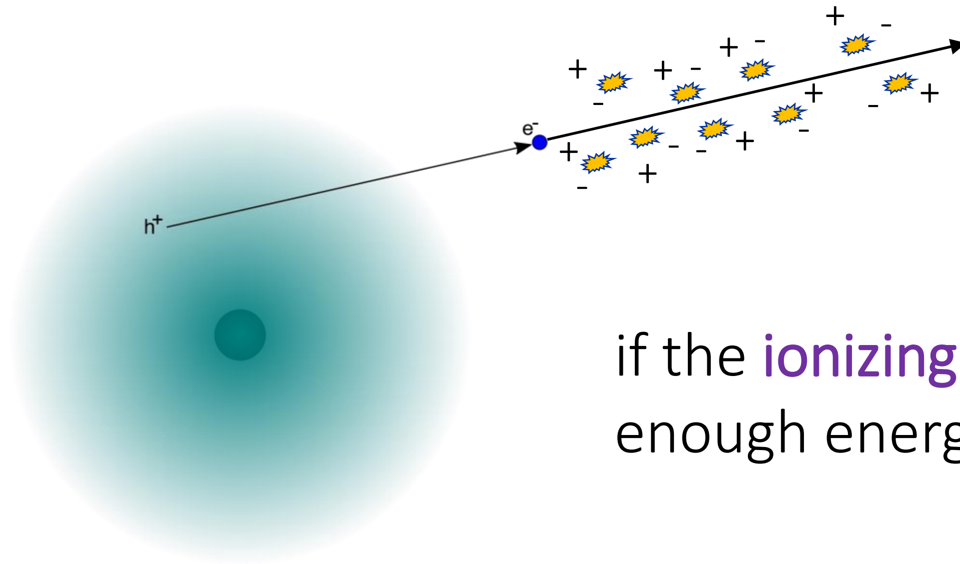
how is charge generated?

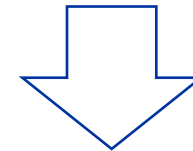


ionization!





if the ionizing particle and/or the emitted electron have enough energy, they can ionize other atoms along their path



multiple electron-hole pairs

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Total Ionizing Dose effects

$\approx$

accumulation of charge in the oxides of an electronic device

example: charge build-up in the gate oxide of a MOS transistor

yet another particle

particle

another particle

GATE

charge accumulated in the gate oxide!

POLY

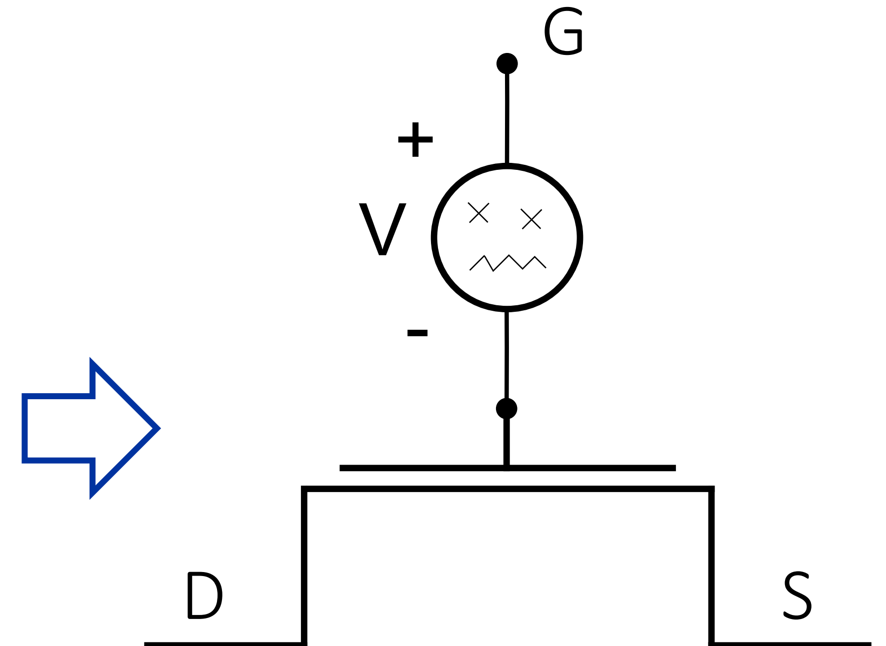
DRAIN

SOURCE

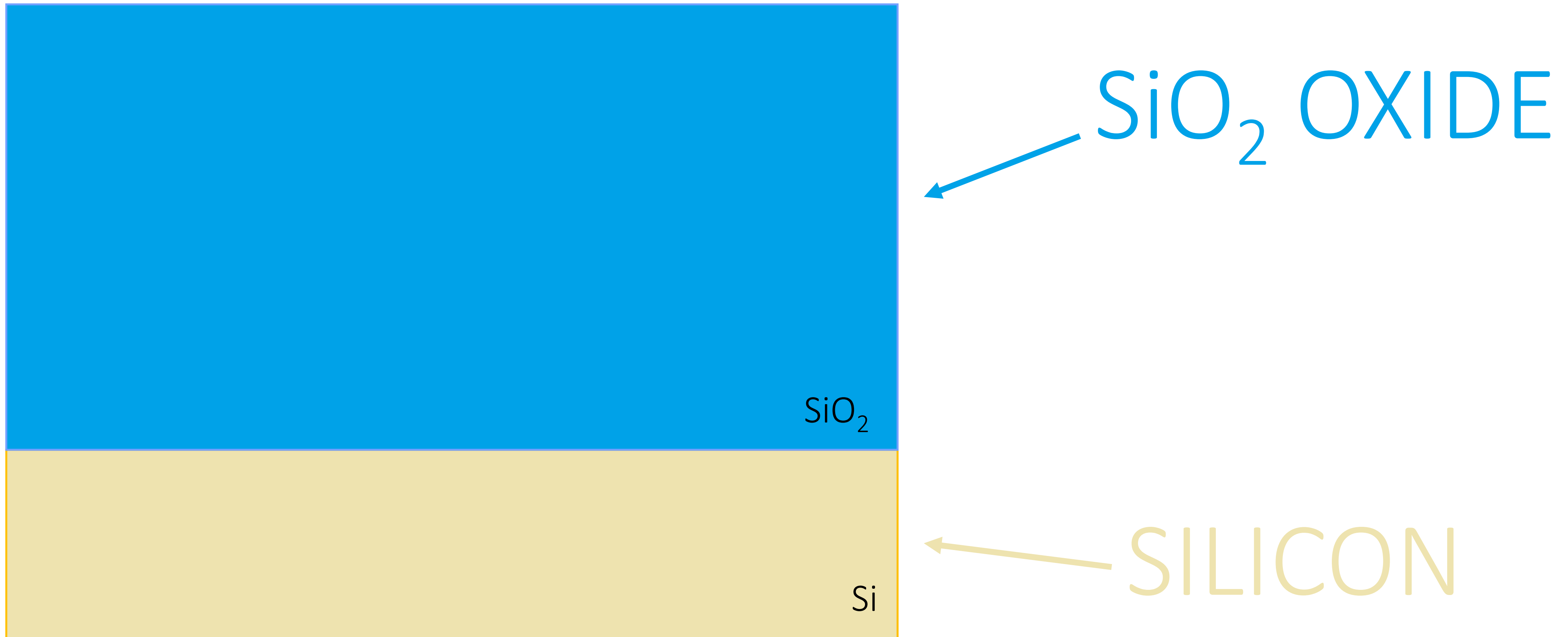
n+

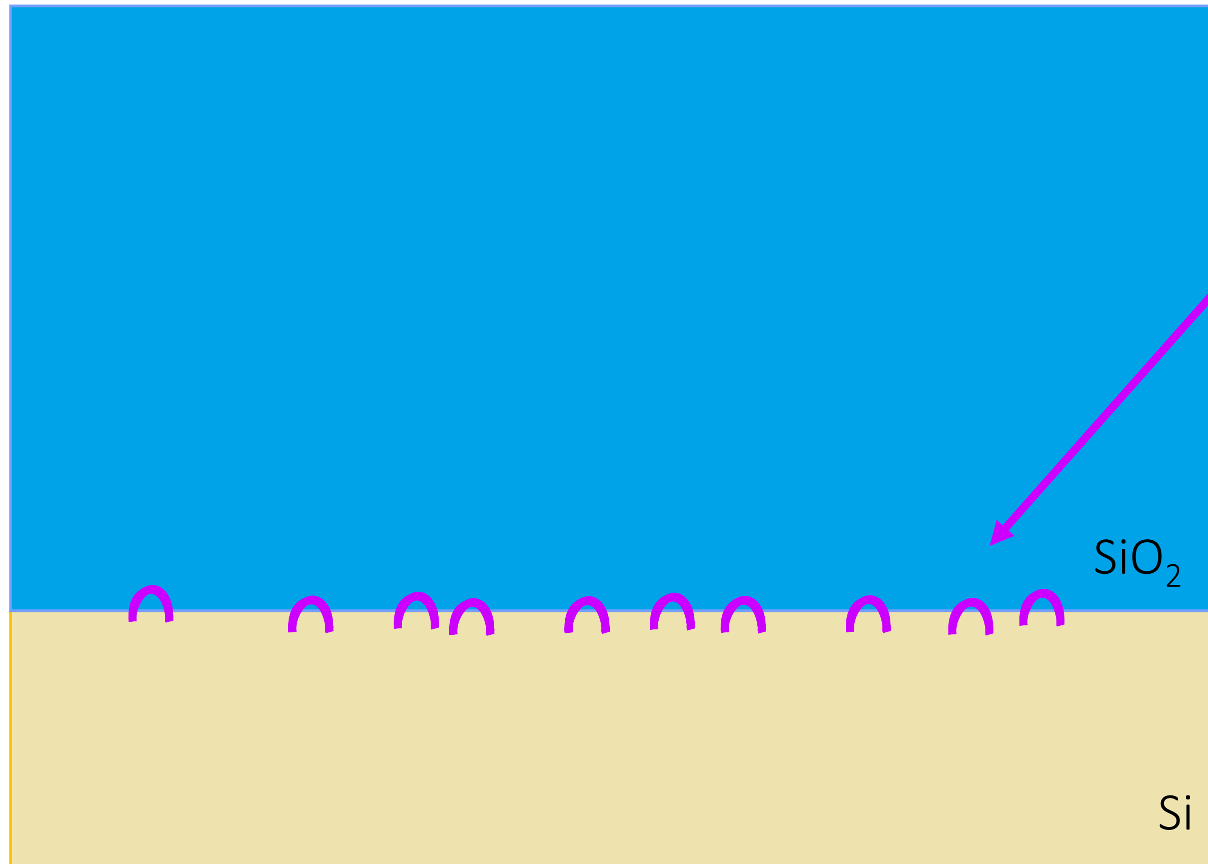
gate oxide

p+

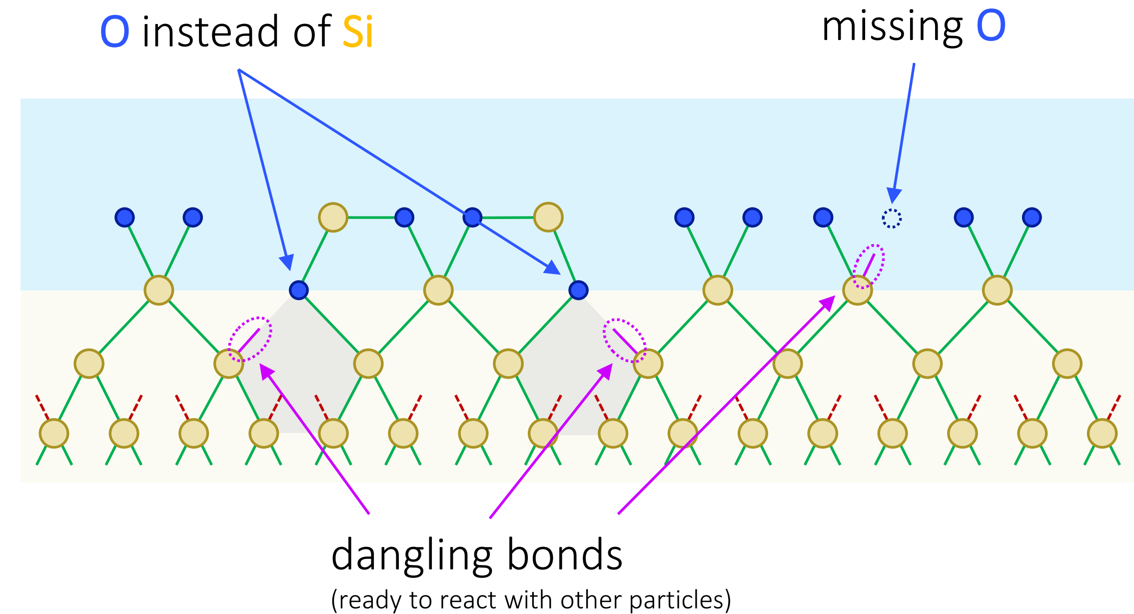


how do we accumulate charge in the oxides?

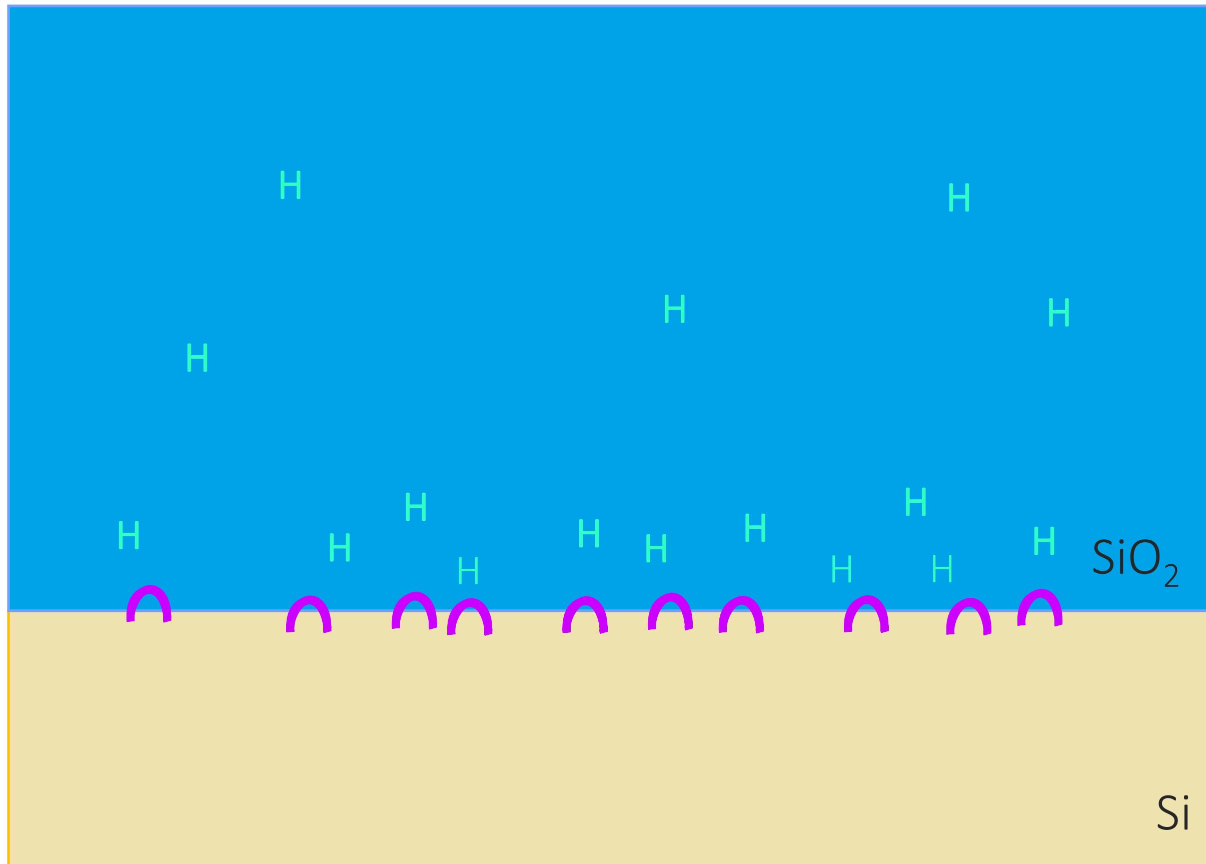

SiO_2 OXIDE
SILICON
SiO_2
Si



The Si/SiO_2 of any real device is not perfect but contains **defects** capable of exchange charge with the silicon substrate.

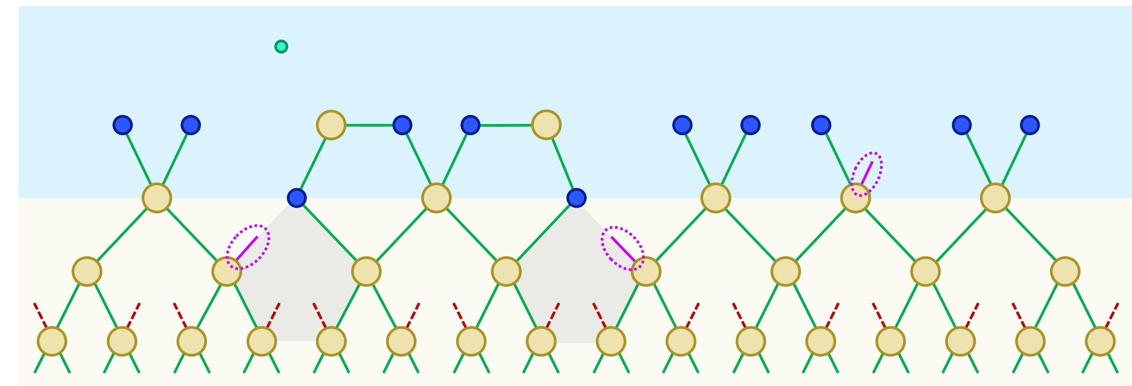


[1] Poindexter, Edward H., et al. "Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers." *Journal of Applied Physics* 52.2 (1981): 879-884.
[2] https://www.iue.tuwien.ac.at/phd/goes/dissse19.html#x43-560005.1
[3] Brower, K. L. "Kinetics of H2 passivation of P b centers at the (111) Si-SiO2 interface." *Physical Review B* 38.14 (1988): 9657.



any real SiO_2 used in CMOS technology contains hydrogen atoms H.

H atoms can **passivate** the interface **defects**



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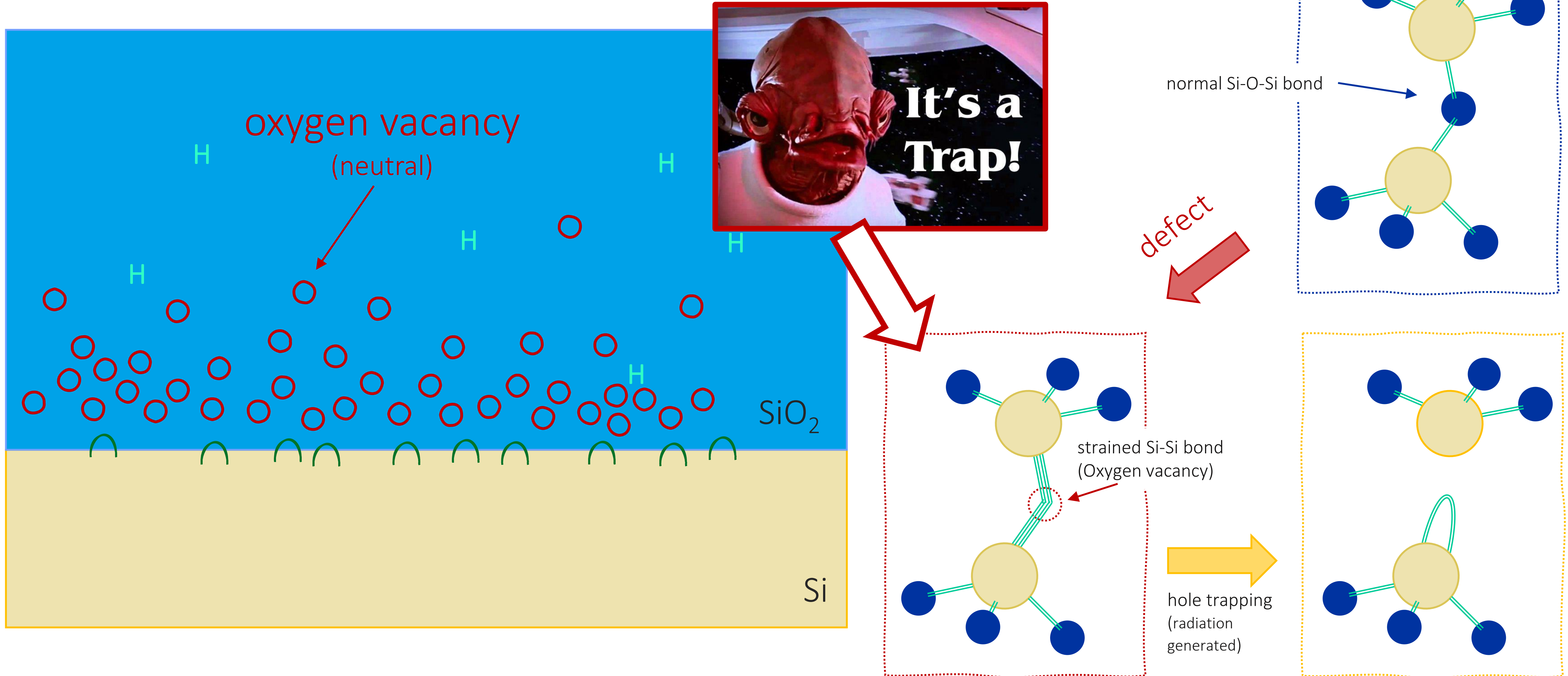
any real SiO_2 used in CMOS technology has some defects, typically missing O, that are prone to retrain **holes**.



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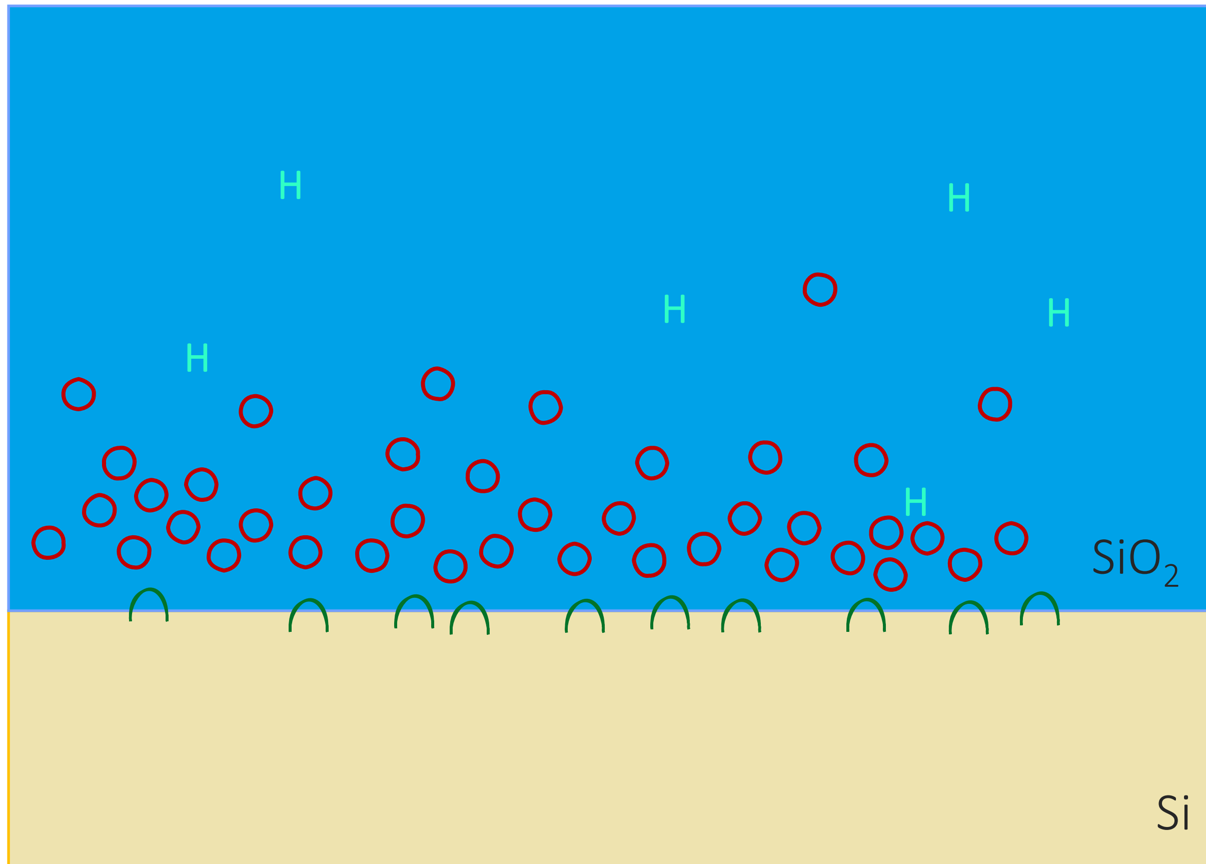
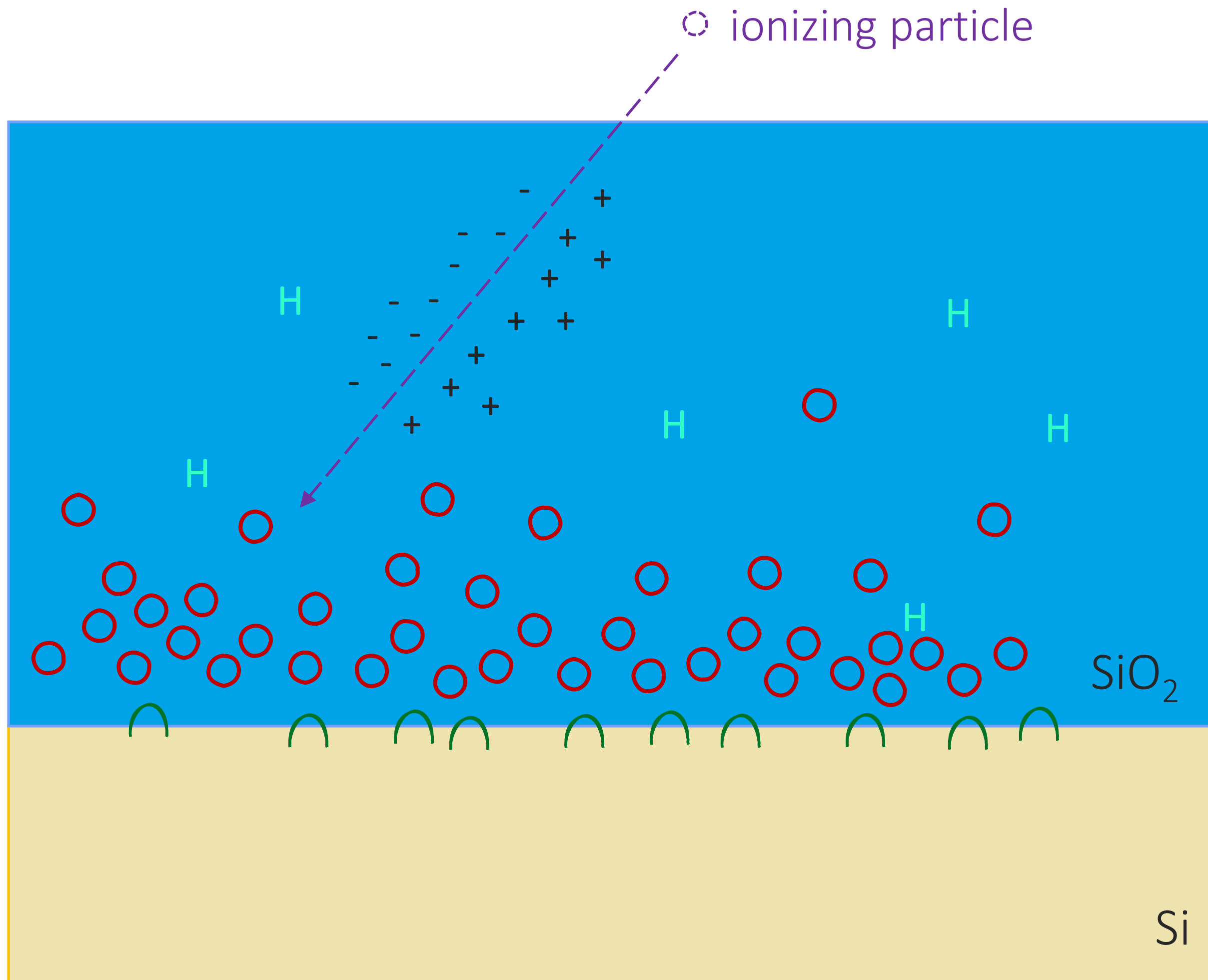
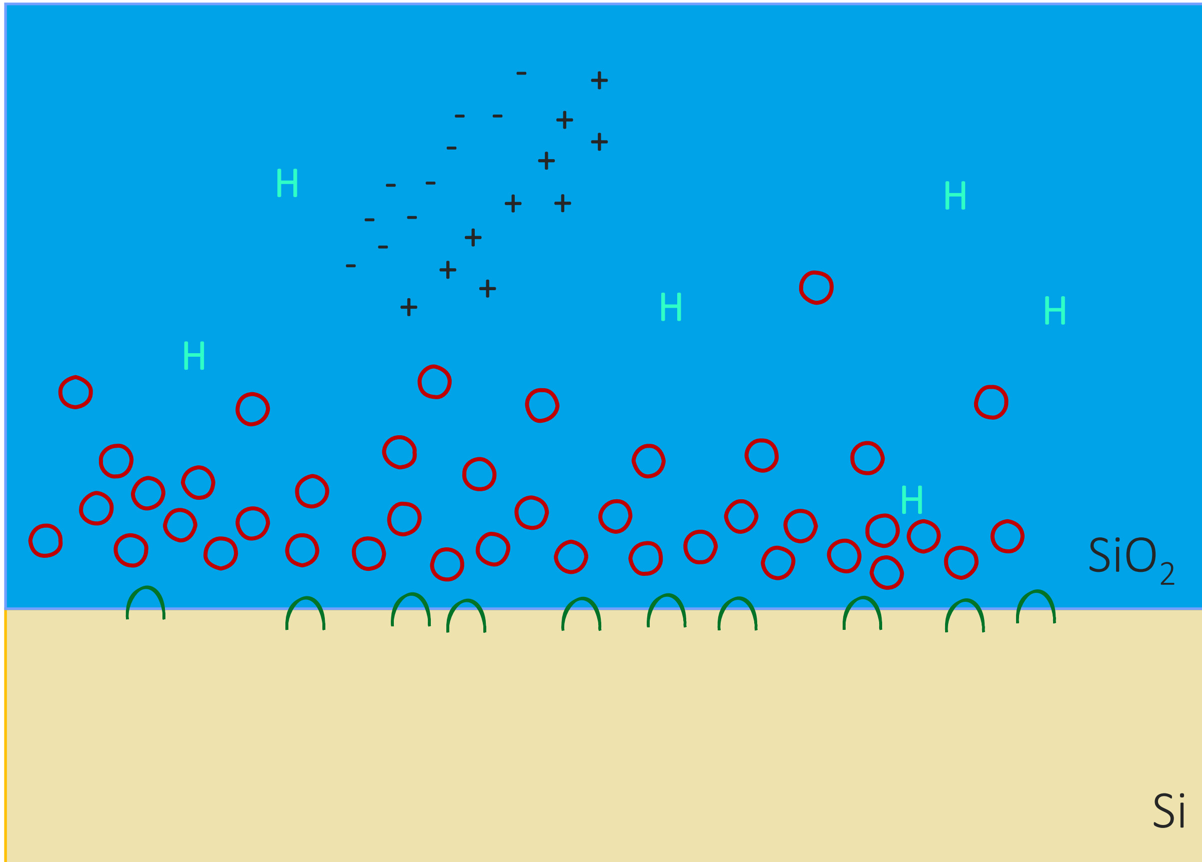
- ionizing particle

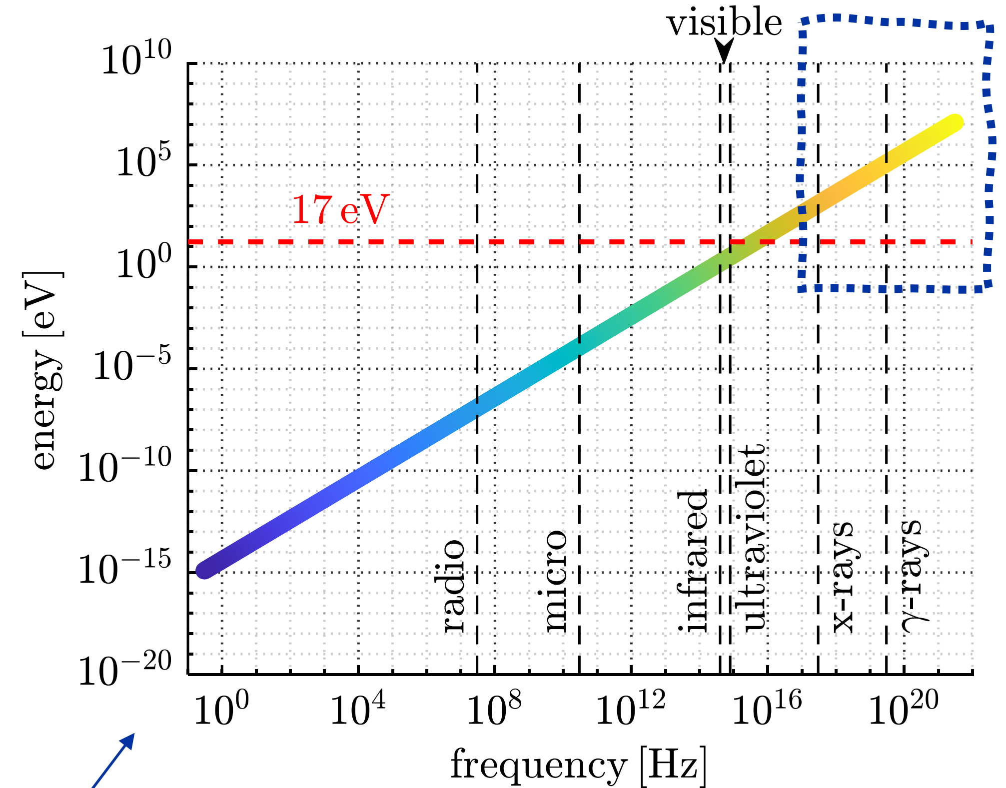



ionizing particle
H
H
H
H
H
H
SiO_2
Si

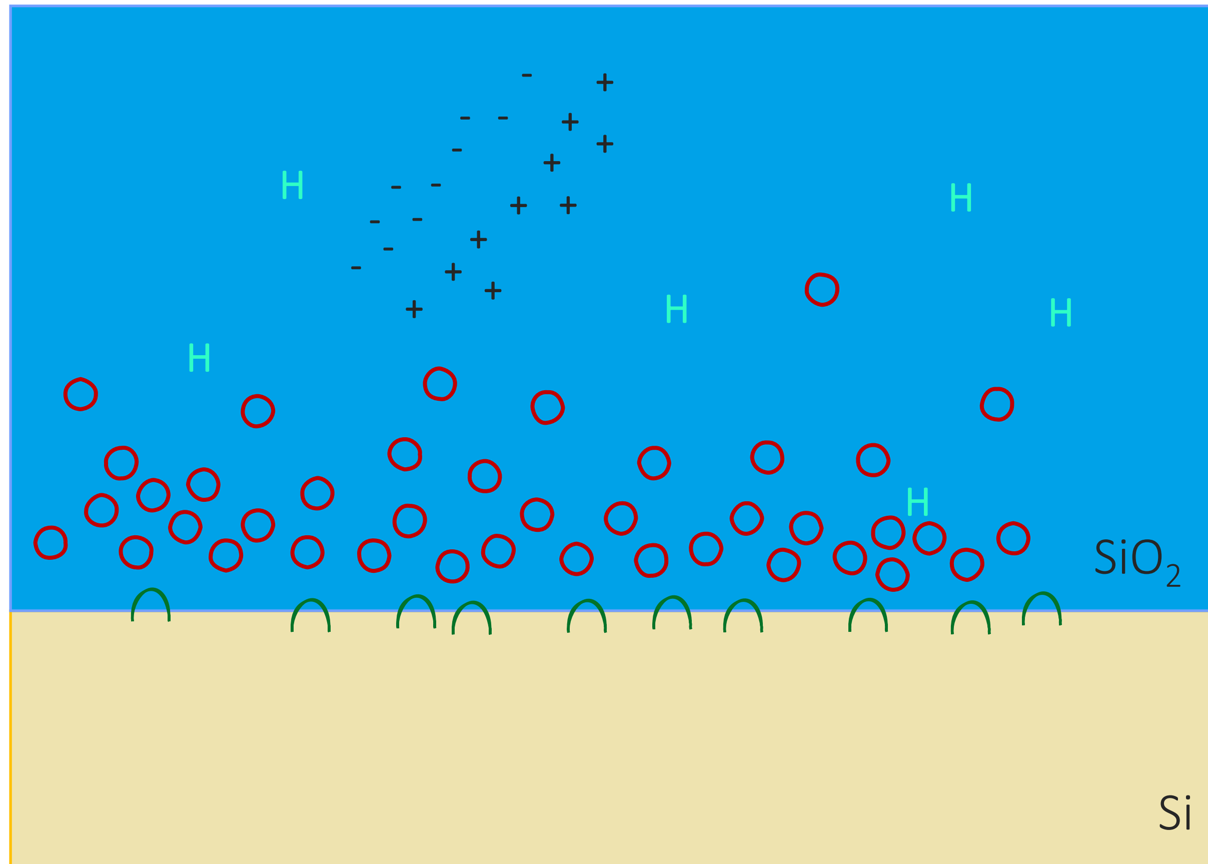


e-h pair creation energy in SiO2 ~17eV

You need x- or γ-rays if you want to generate many e-h pairs

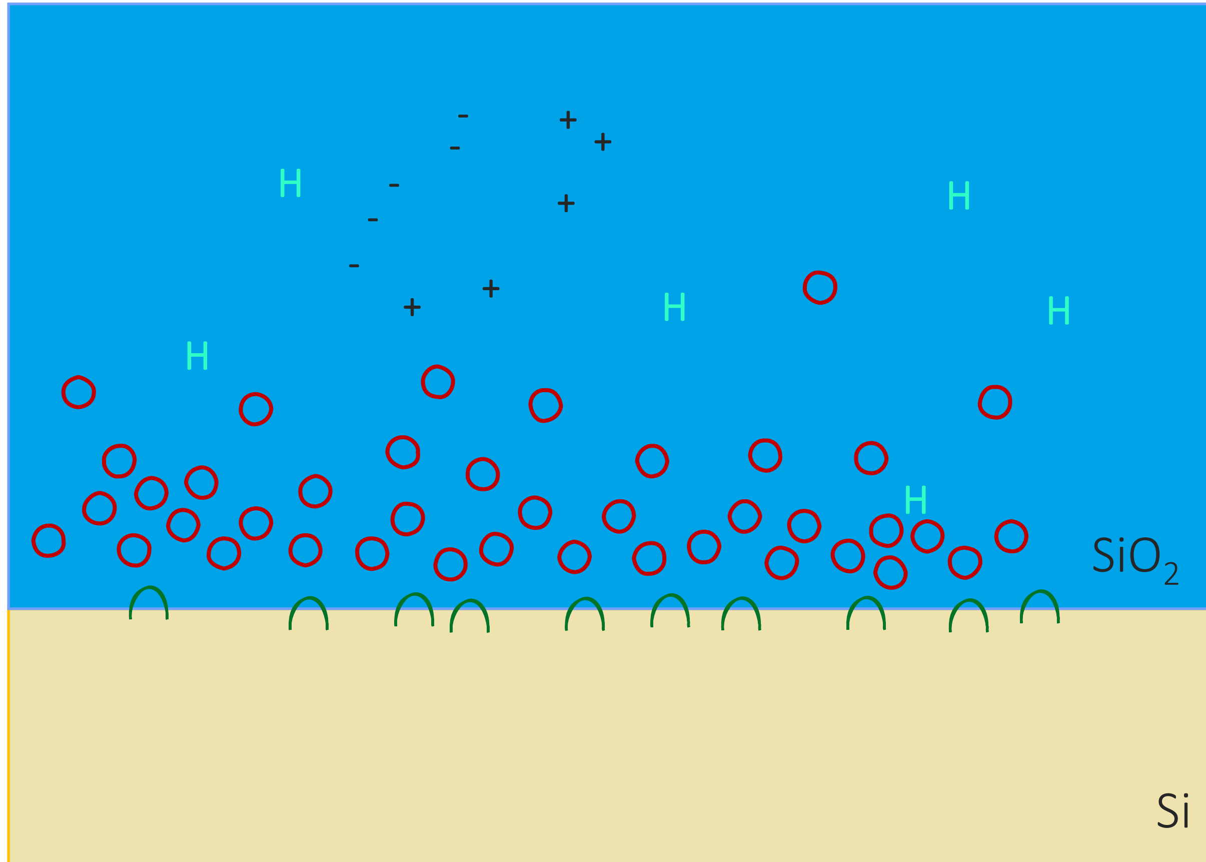


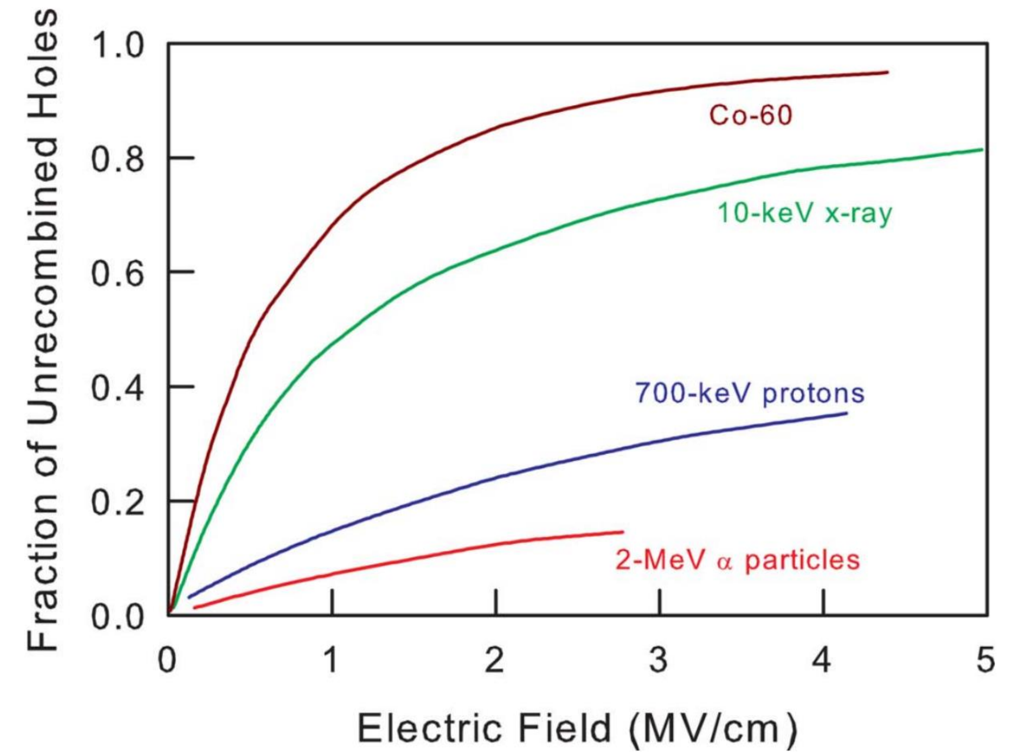
example: photons



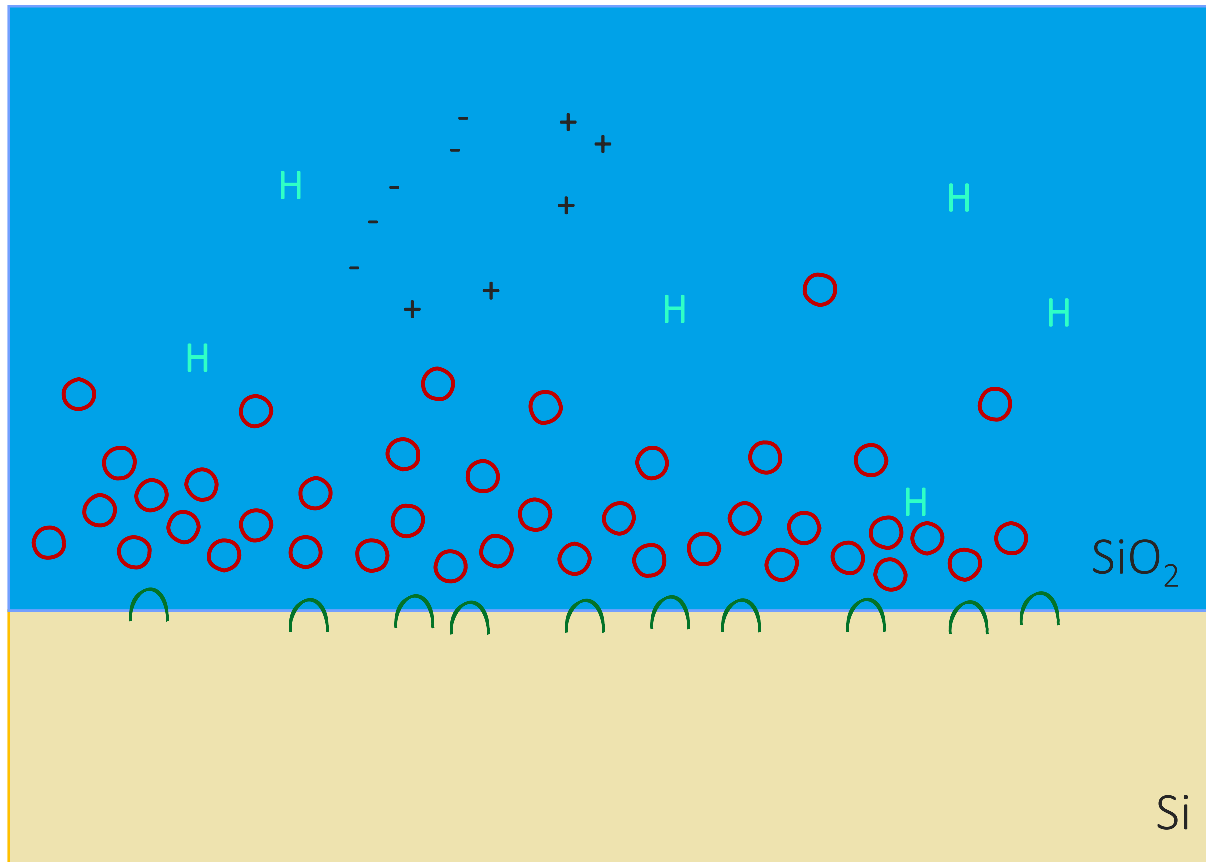
some of the e-h pairs **recombine** immediately after generation!

recombination efficiency depends on the electric field!





Schwank, James R., et al. "Radiation effects in MOS oxides." *IEEE Transactions on Nuclear Science* 55.4 (2008): 1833-1853.



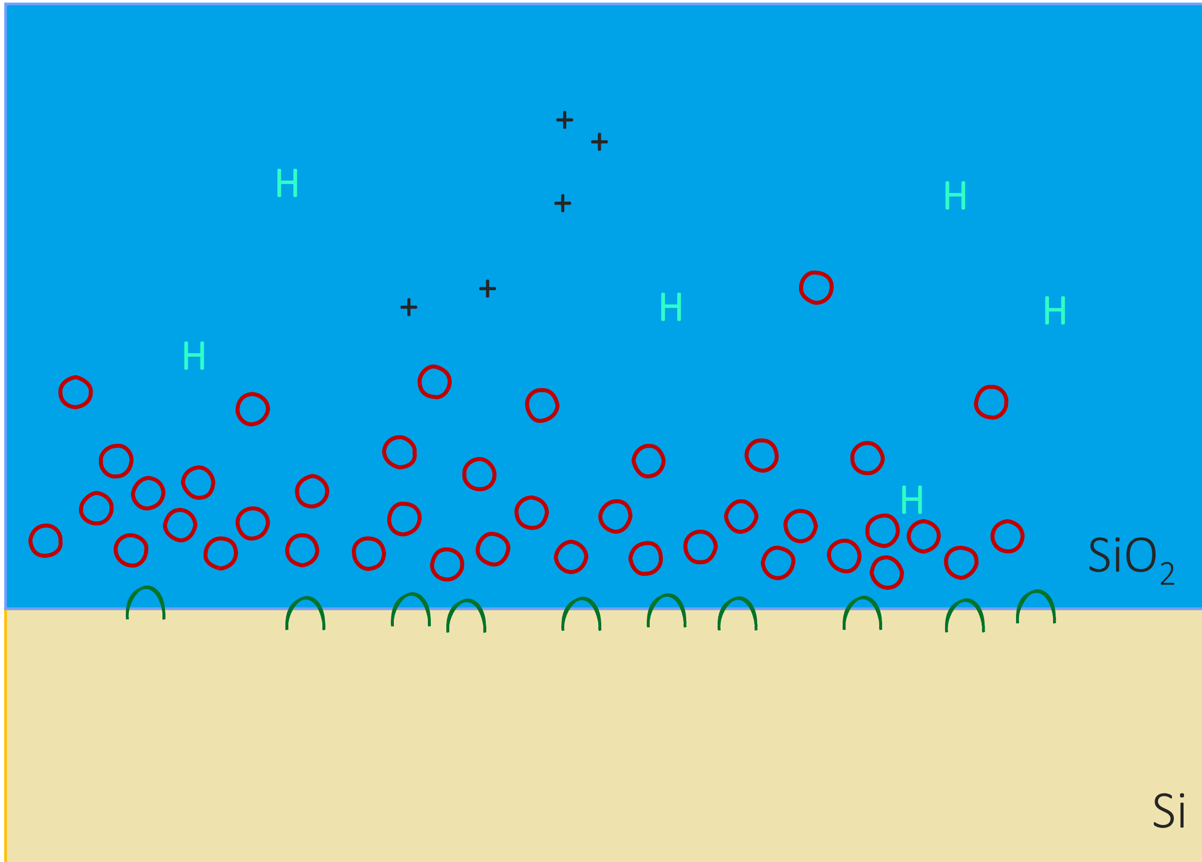
recombination must take place in the first instants after generation, because electrons move quickly and leave the oxide in a short time

example: t_{ox} = 100 nm, V = 5 V, T = 25 °C

e^- mobility (μ) in SiO_2 at room $T \approx 20\ cm^2V^{-1}s^{-1}$

time needed to cross $t_{ox} \approx$ 1 ps

electrons are very fast!

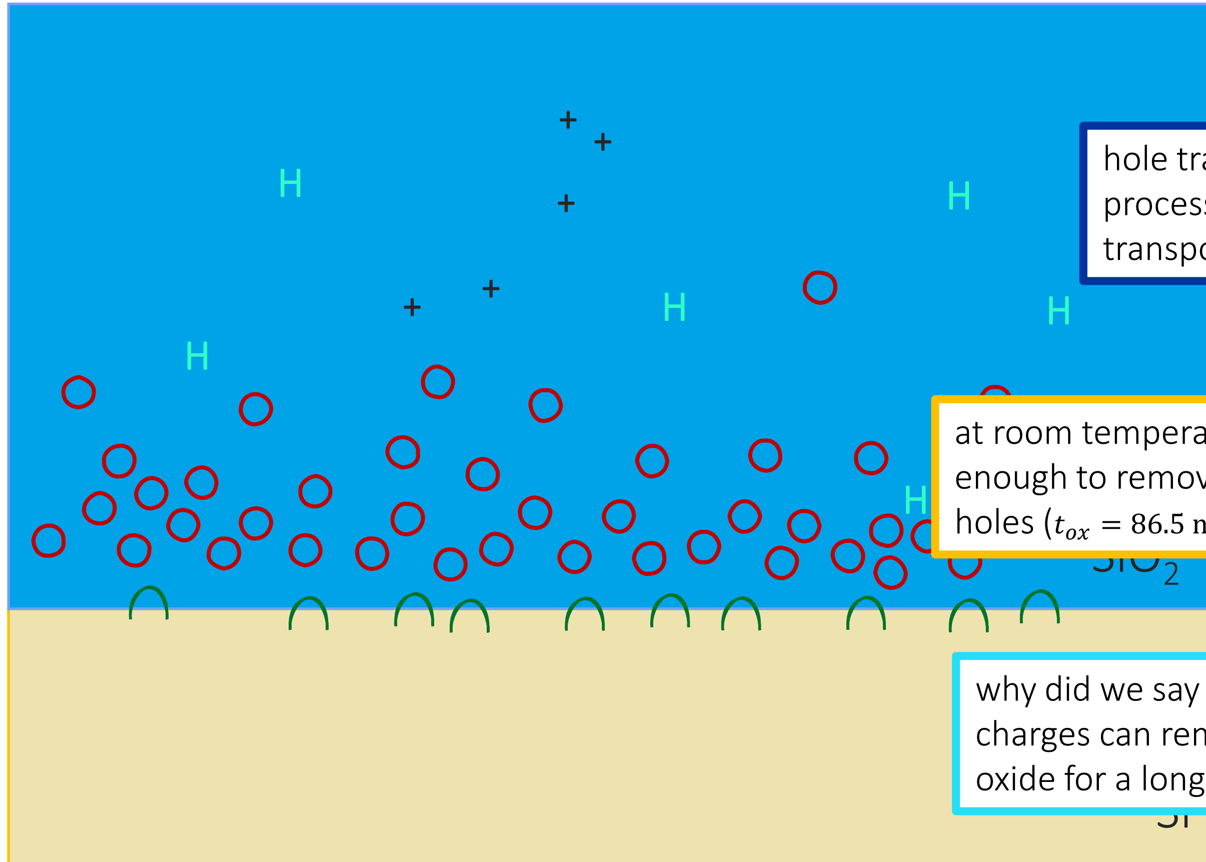


we started with a neutral oxide and now it is positively charged!

what happens to the holes?

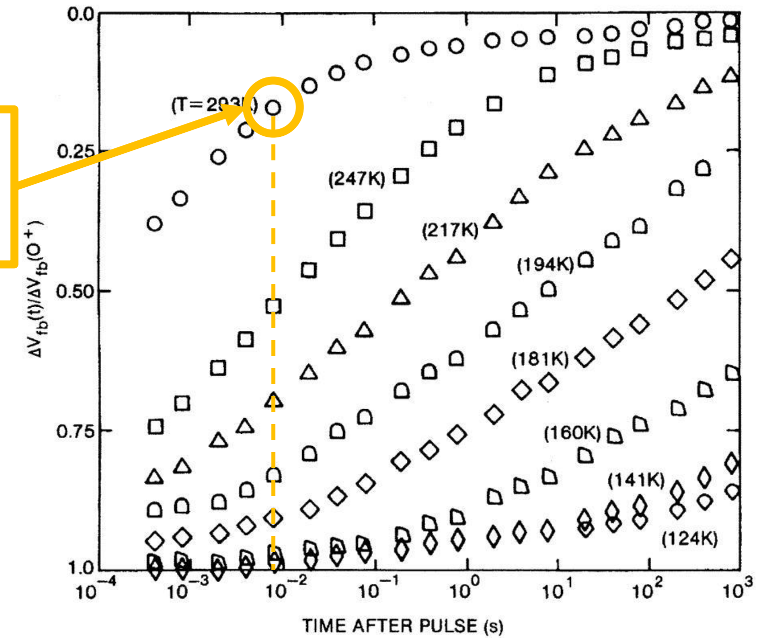
- some holes just leave the oxide
  (i.e., they recombine with an electron coming from outside)

hole transport it is a quite complex process, much slower than electron transport but still relatively fast



at room temperature ~10 ms are enough to remove a large fraction of holes ($t_{ox} = 86.5\ \text{nm}, \vec{E} = 1\ \text{MV/cm}$)

why did we say that the charges can remain in the oxide for a long time?



TRAPS!

H. E. Boesch, J. M. McGarrity, and F. B. McLean. "Temperature- and Field-Dependent Charge Relaxation in SiO2 Gate Insulators." In: IEEE Transactions on Nuclear Science 25.3 (June 1978), pp. 1012–1016.

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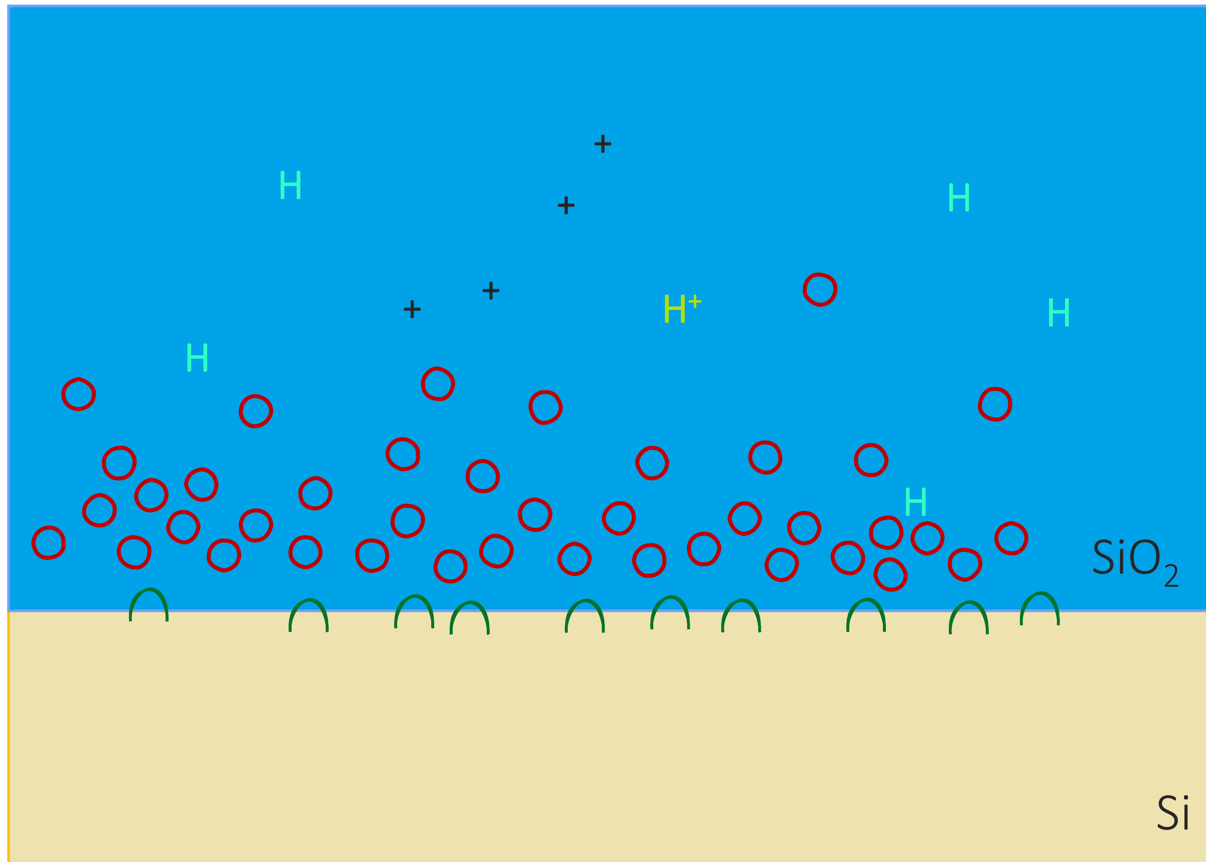
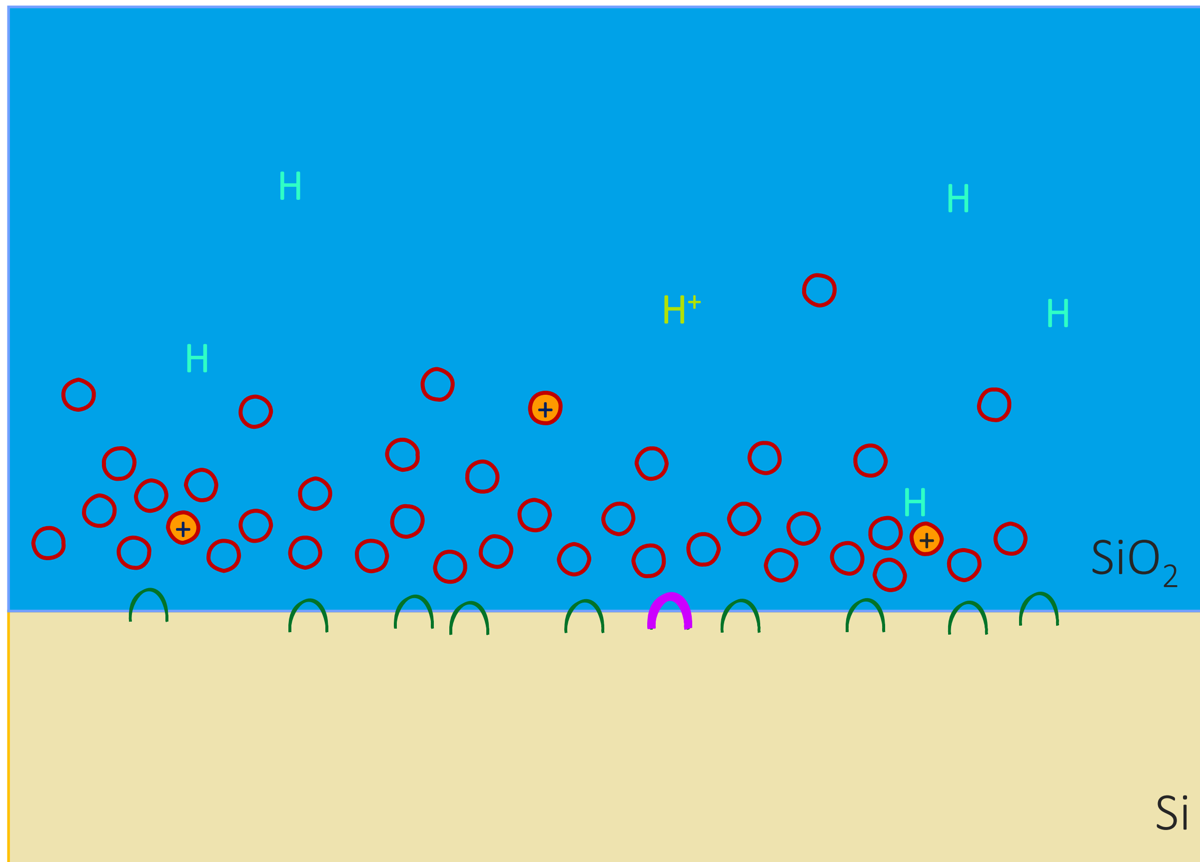
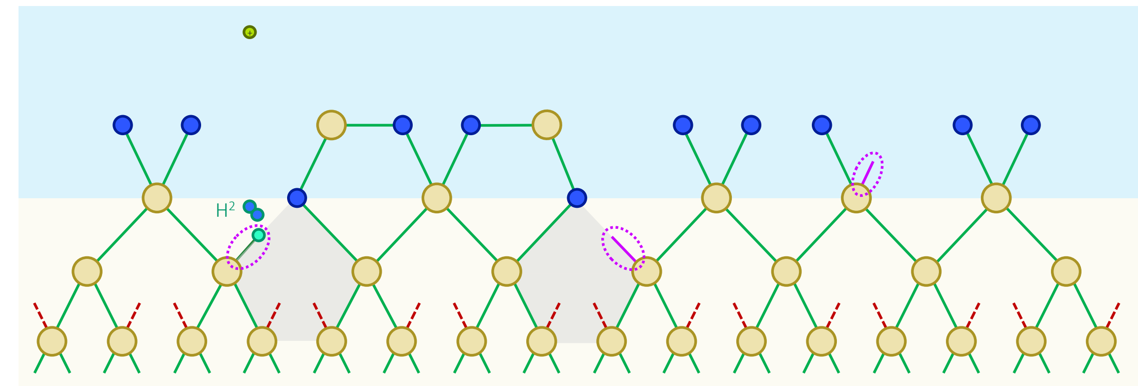


- some holes just leave the oxide
  (i.e., they recombine with an electron coming from outside)
- some holes get trapped in the oxide-traps
- some holes react with H forming hydrogen ions H^+

what happens to the H^+?

they can move through the oxide and if they reach the interface, they can de-passivate the interface traps





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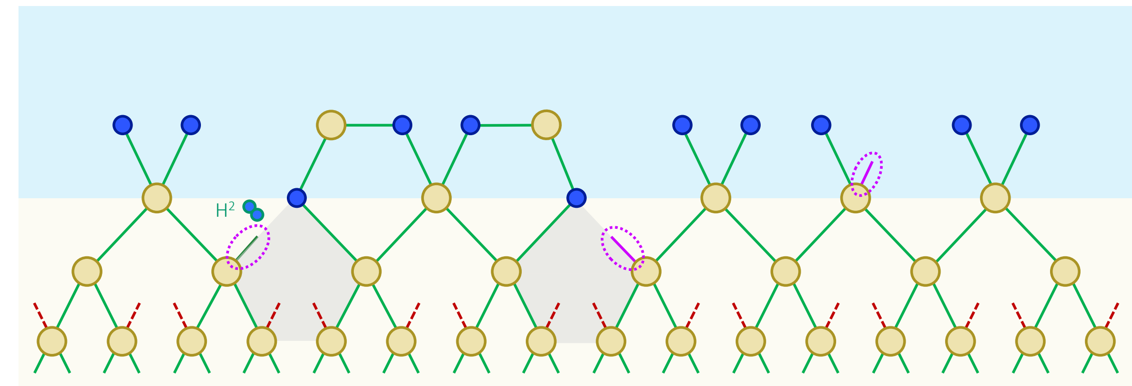

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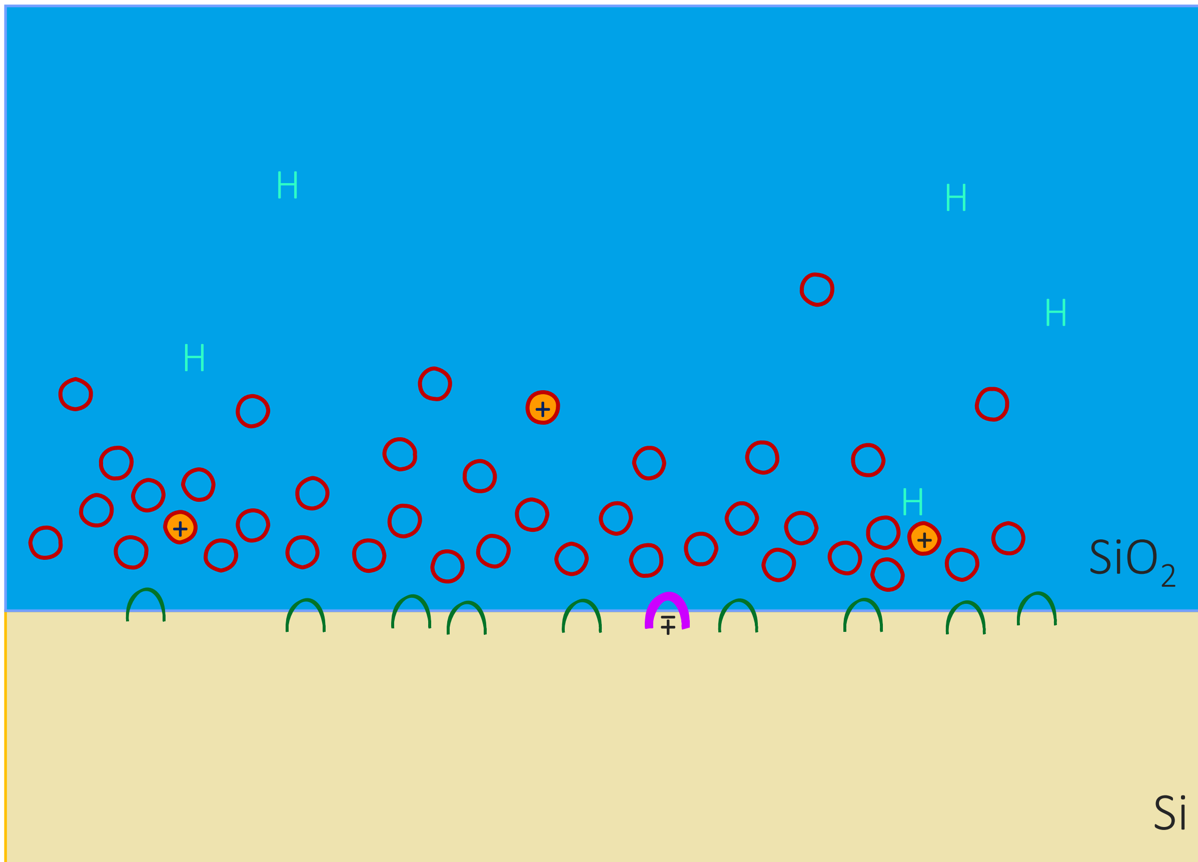

they can move through the oxide and if they reach the interface, they can de-passivate the interface traps

the sign of the charge trapped at the interface depends on the relative energy of the traps with respect to the Fermi level.

In practice:

- nMOS: negative charge
- pMOS: positive charge

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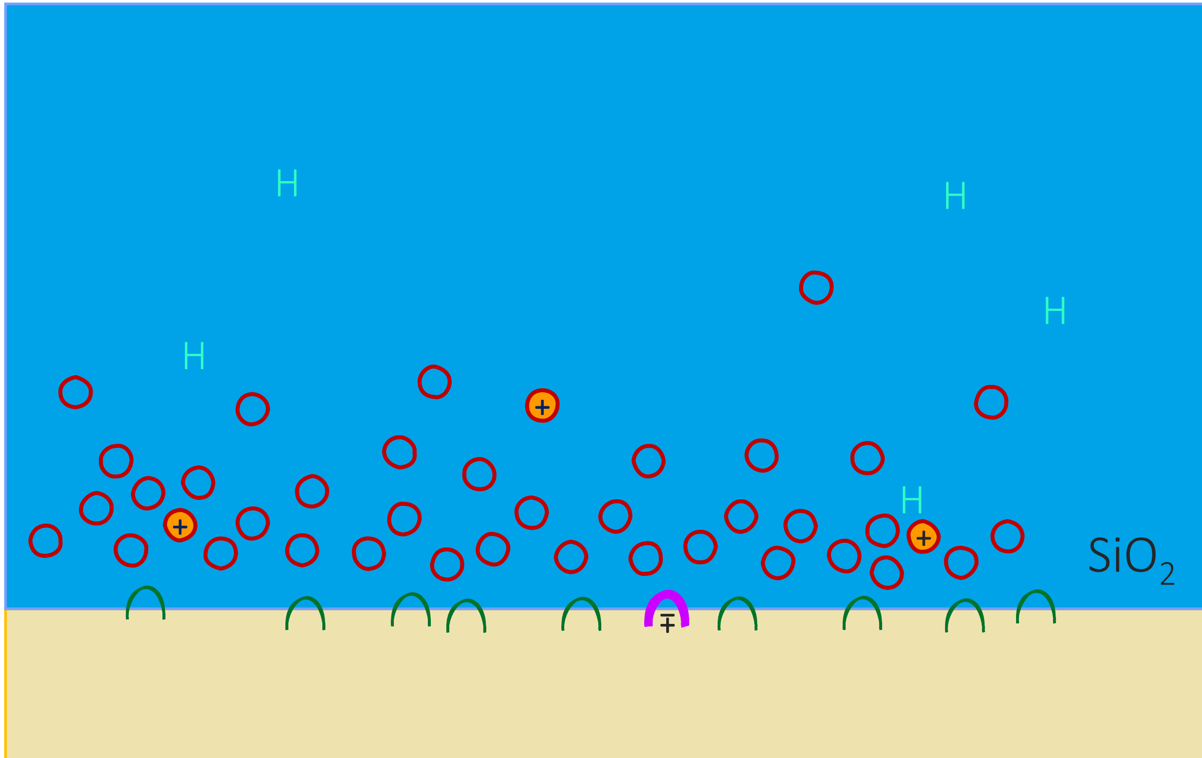

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In practice:

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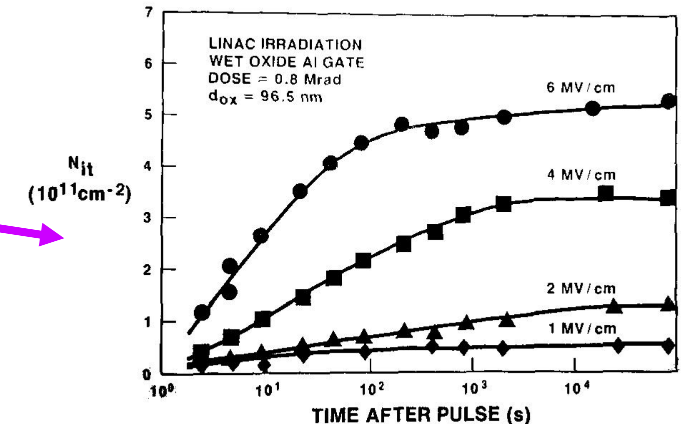
the transport of H^+ and interface traps (N_{it}) formation is significantly slower than that of hole



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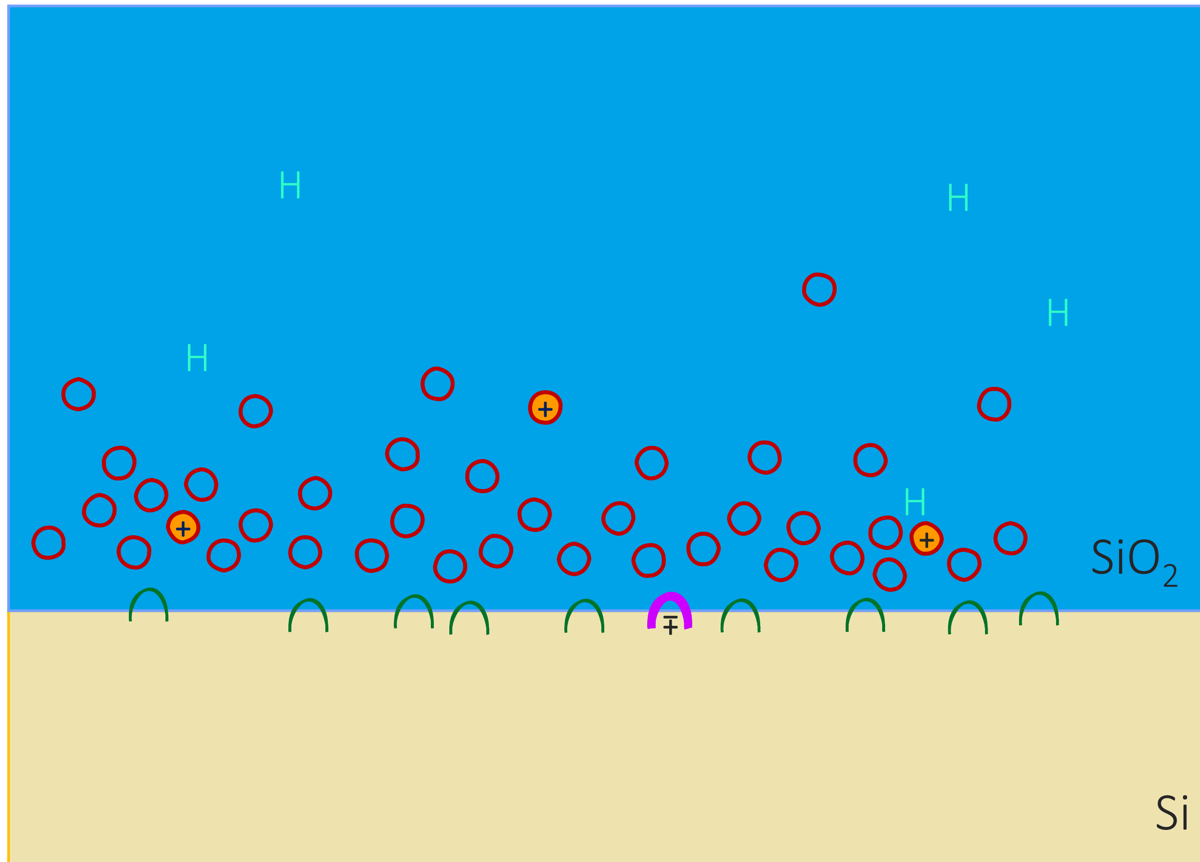
RECAP

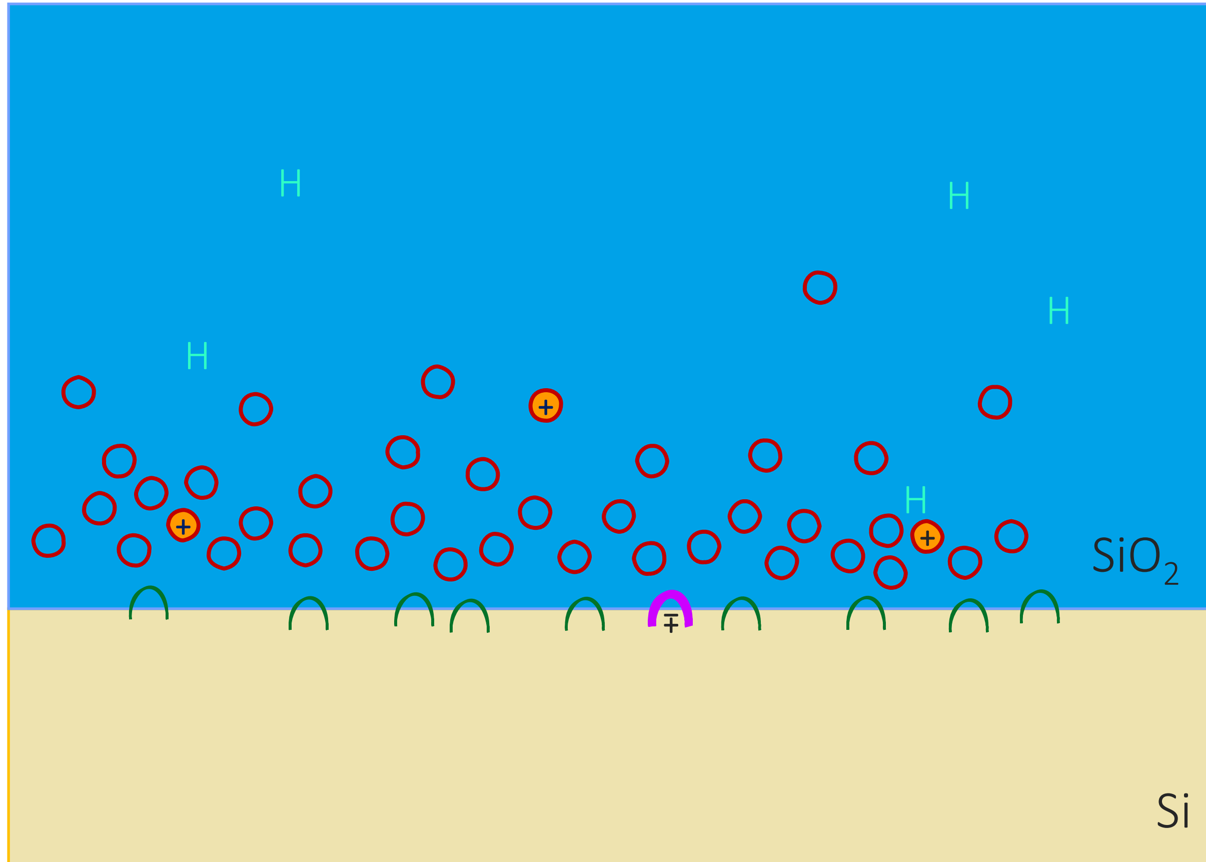


- oxide traps retain POSITIVE charge (always)
- interface traps retain
  - nMOS: negative charge
  - pMOS: positive charge
- the build-up of charge at the interface is slower than the build-up of charge in the oxide

do charges remain trapped forever?

no: reversible and permanent annealing

(in this context, “annealing” refers to the removal of charges*)



*the meaning of the term annealing changes according to context. Sometimes annealing is understood as charge removal, others as a high-temperature post-irradiation heating process, and still others as a simple monitoring of charge evolution after irradiation.

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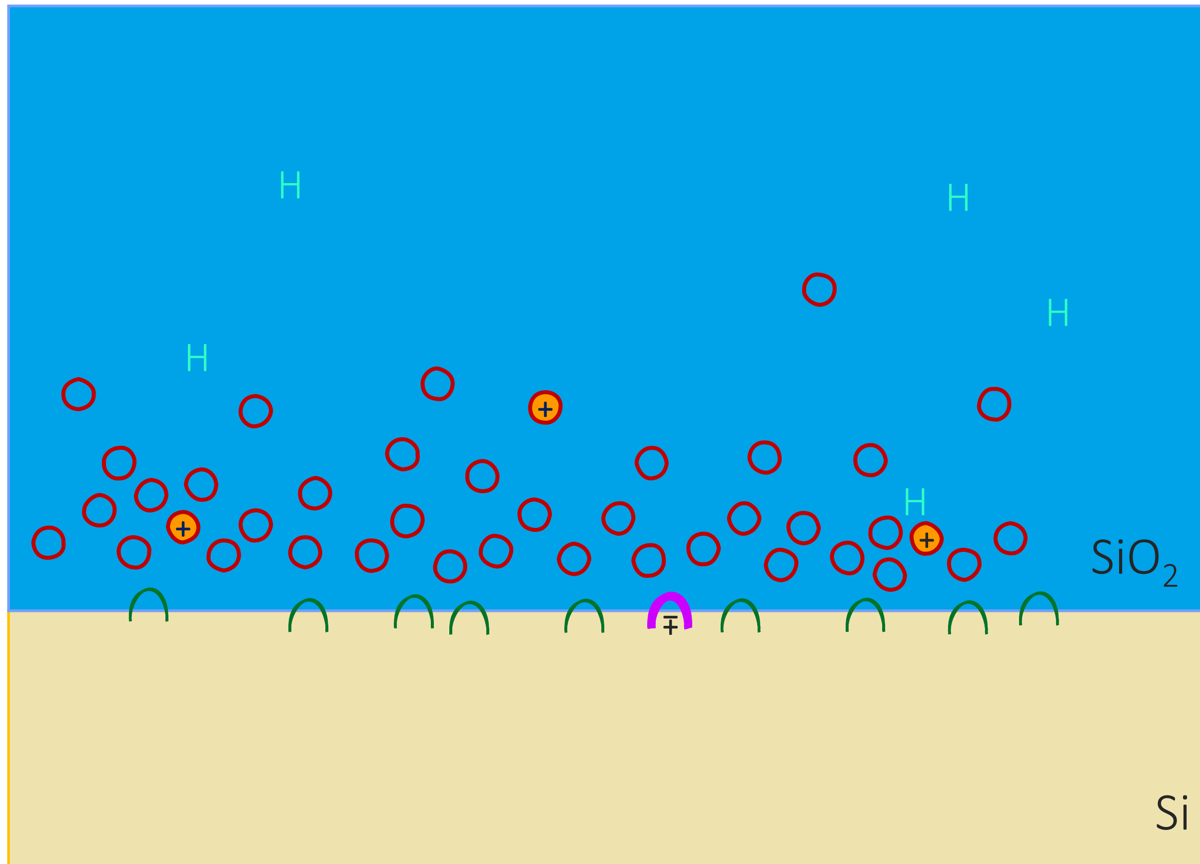

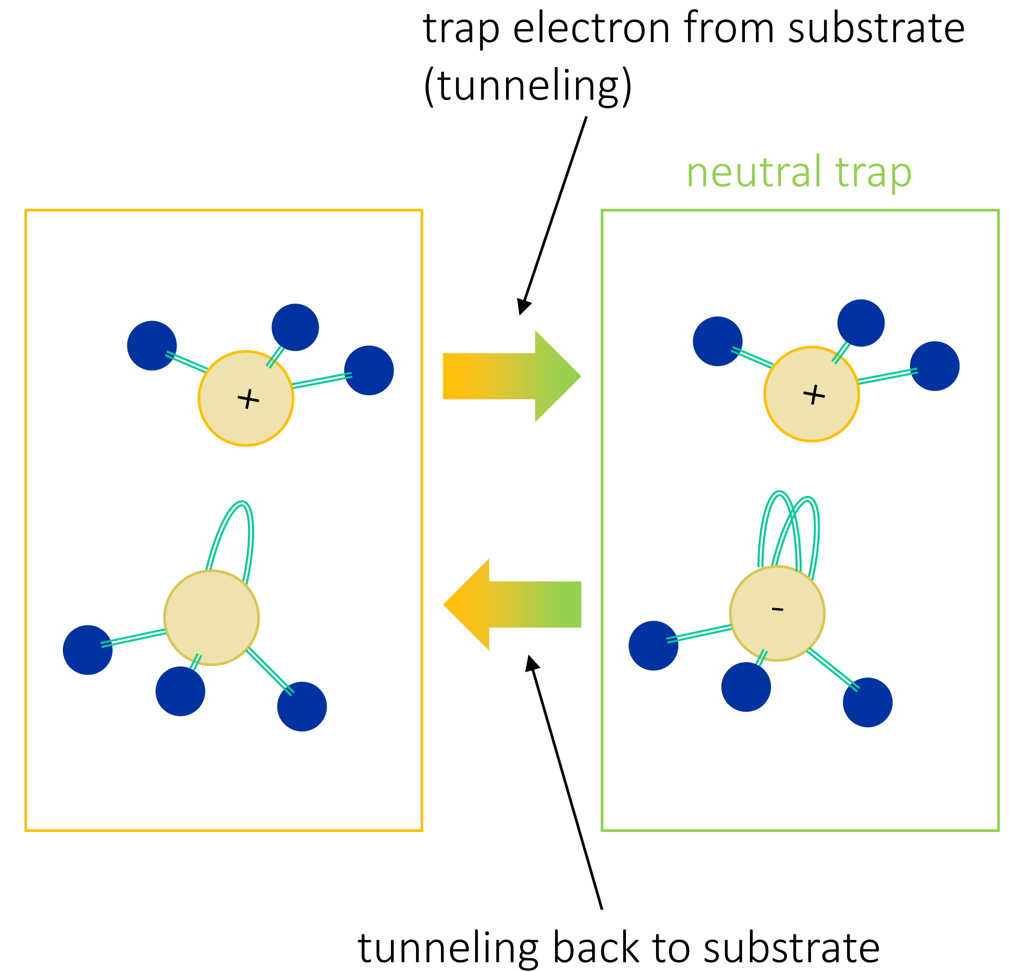

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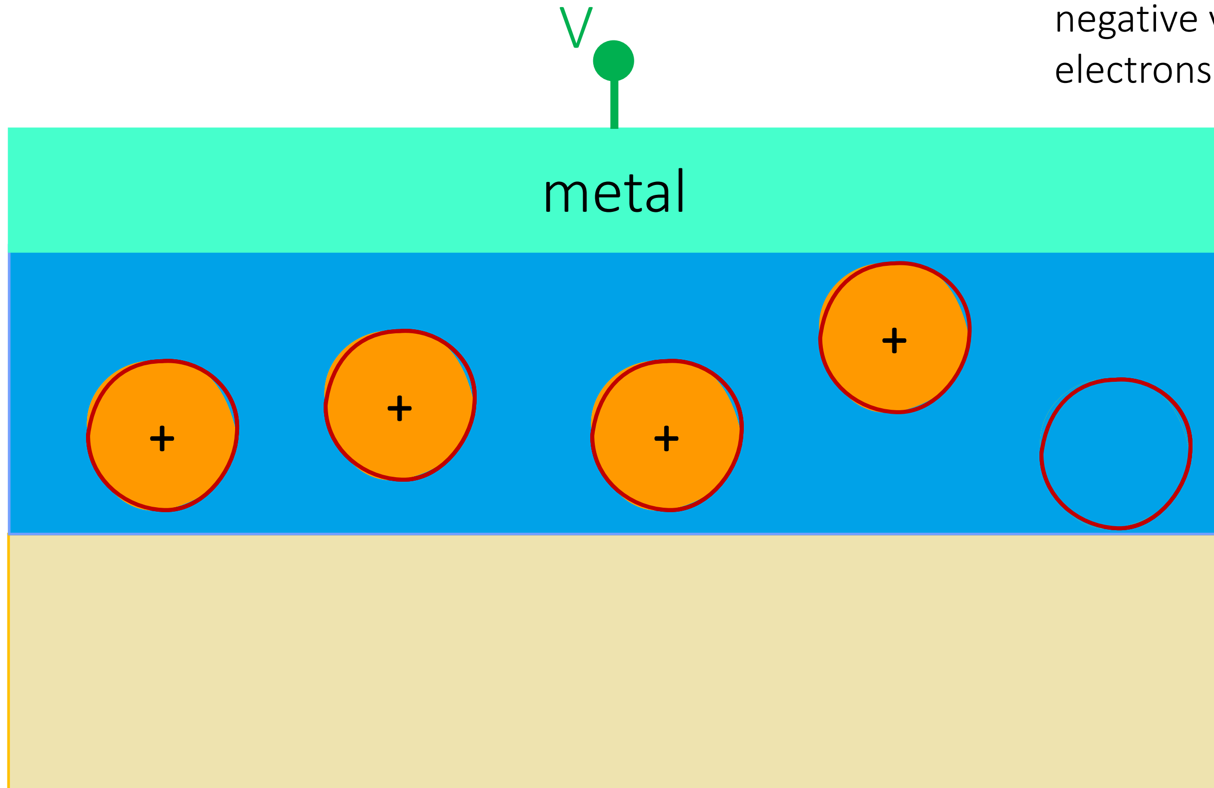

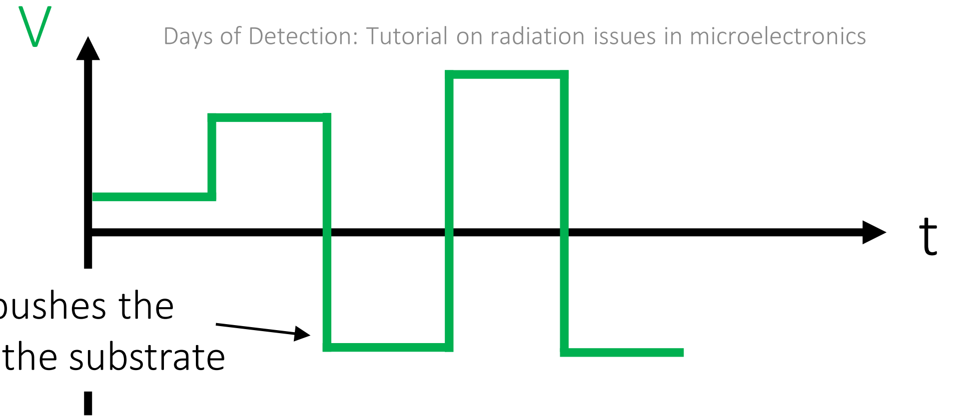

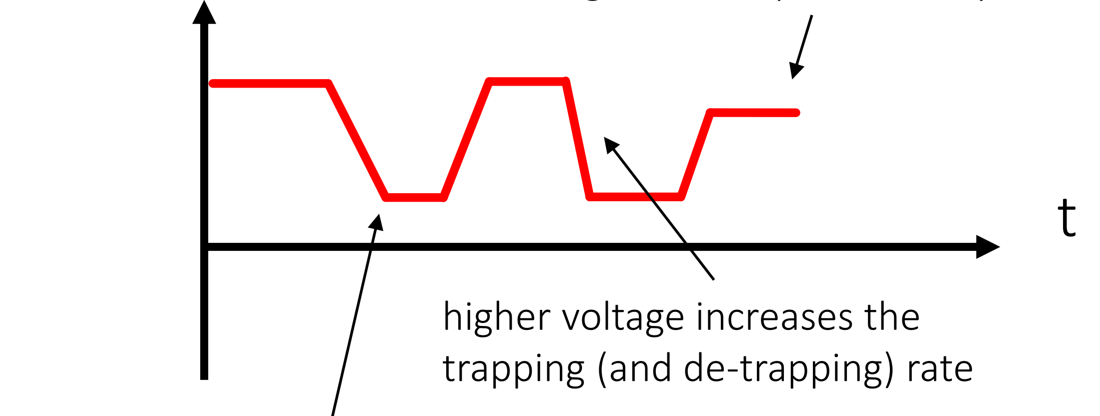

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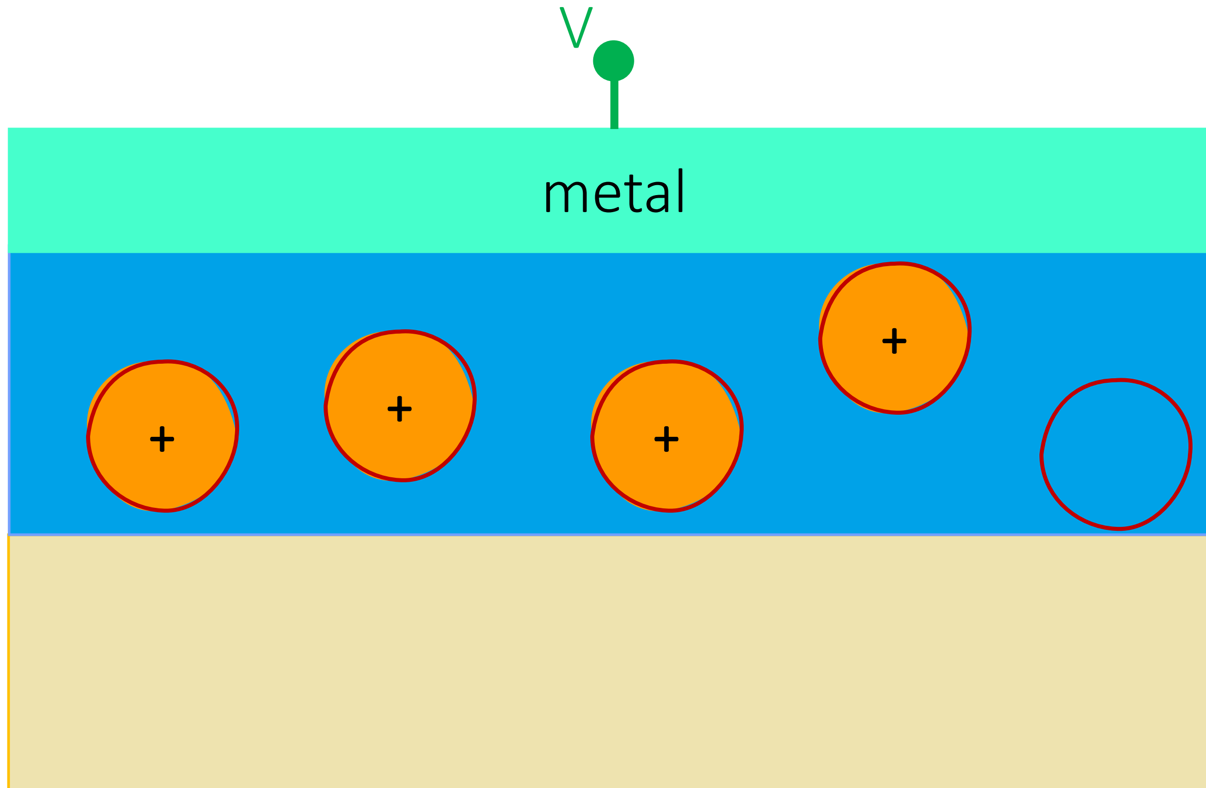

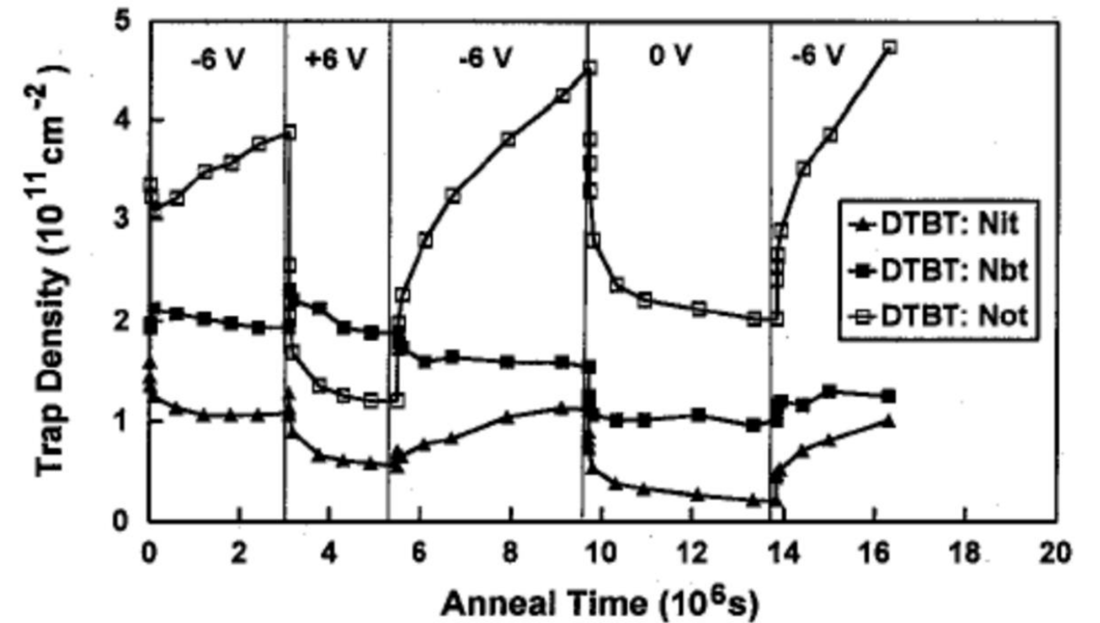

D. M. Fleetwood, W. L. Warren, J. R. Schwank, P. S. Winokur, M. R. Shaneyfelt and L. C. Riewe, "Effects of interface traps and border traps on MOS postirradiation annealing response," in *IEEE Transactions on Nuclear Science*, vol. 42, no. 6, pp. 1698-1707, Dec. 1995, doi: 10.1109/23.488768.

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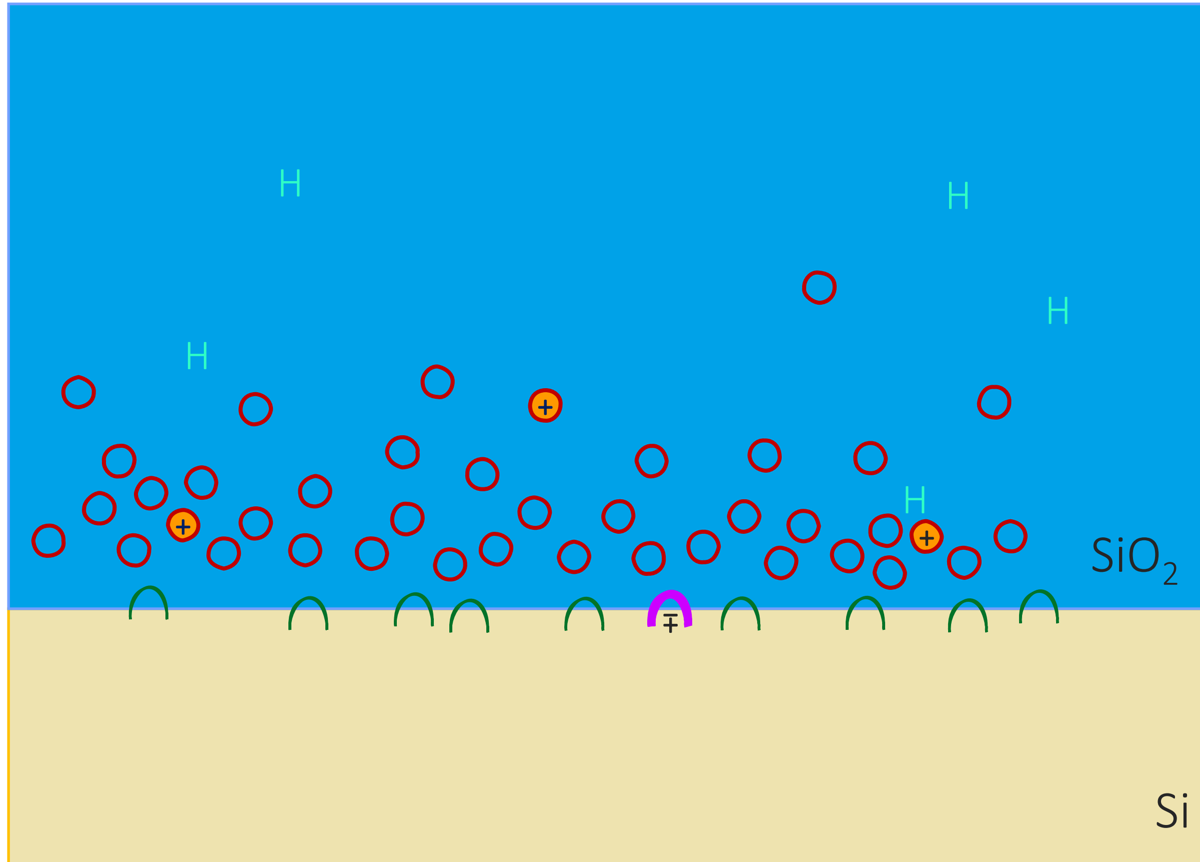

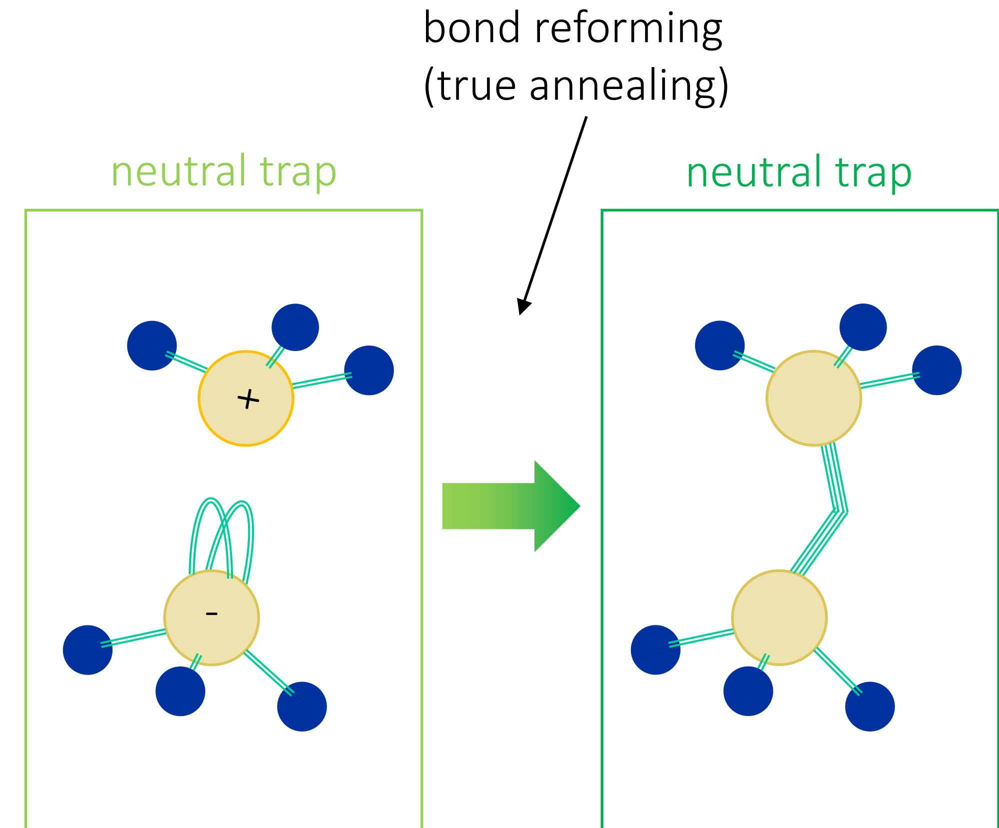

you need to irradiate the device again to trap charge in the permanently annealed traps!

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how do we measure TID?

Unit of measure:

rad (radiation absorbed dose)

1 rad = 100 Gy = 1 J/Kg

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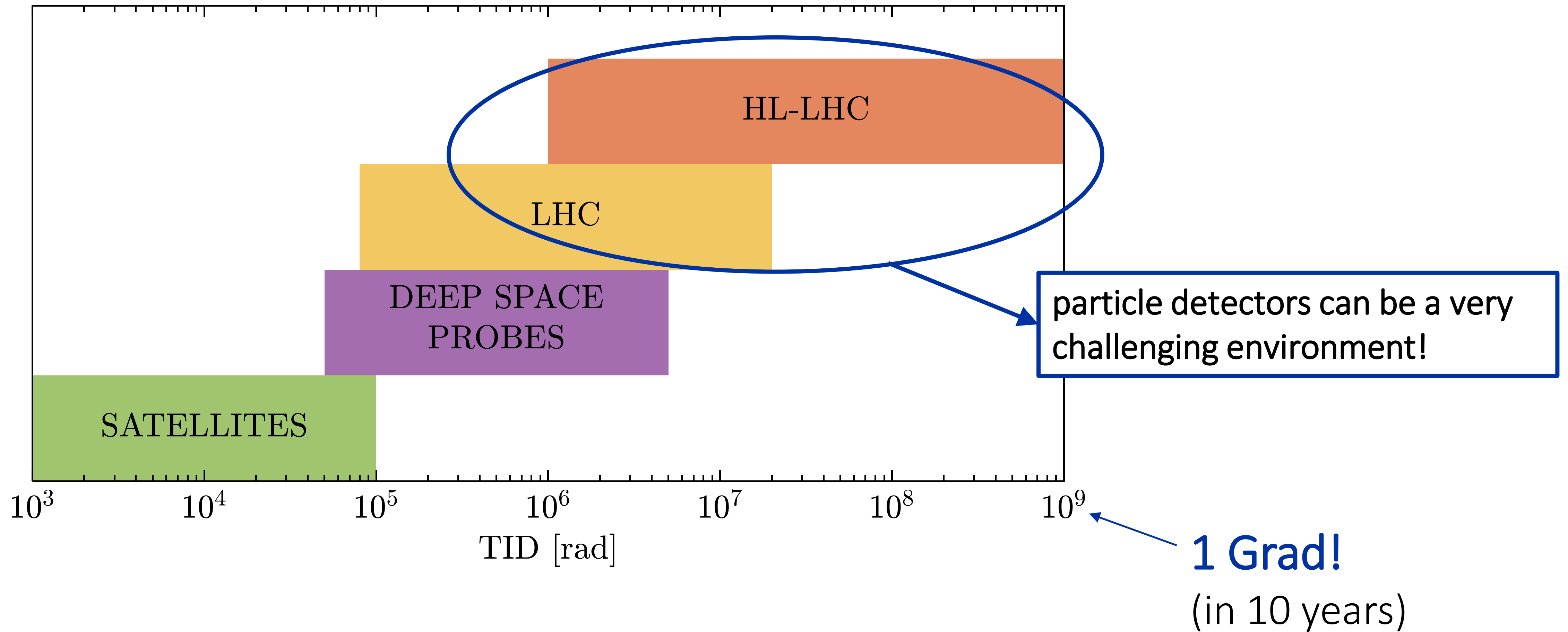
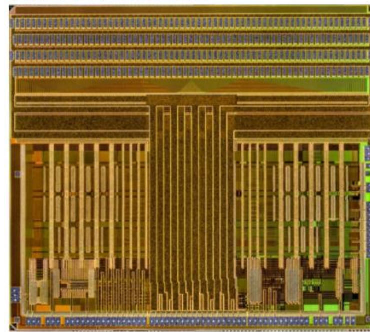

HL-LHC
LHC
DEEP SPACE PROBES
SATELLITES
10^3
10^4
10^5
10^6
10^7
10^8
10^9
TID [rad]
particle detectors can be a very challenging environment!
1 Grad!
(in 10 years)

ASIC: Application Specific Integrated Circuit

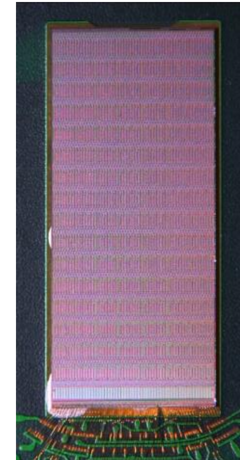
in our case, circuits specifically designed for LHC and HL-LHC

ALICE ITS

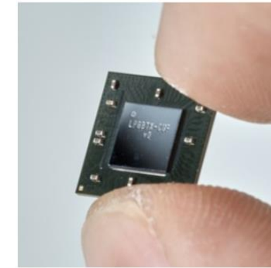
ATLAS ABCStar

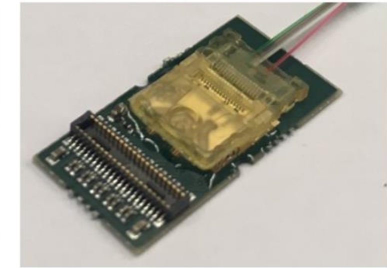


MPA



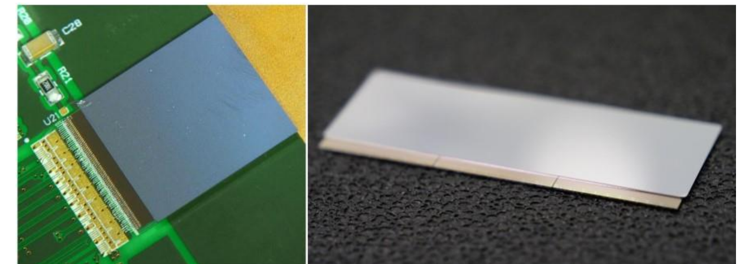
readout ASIC





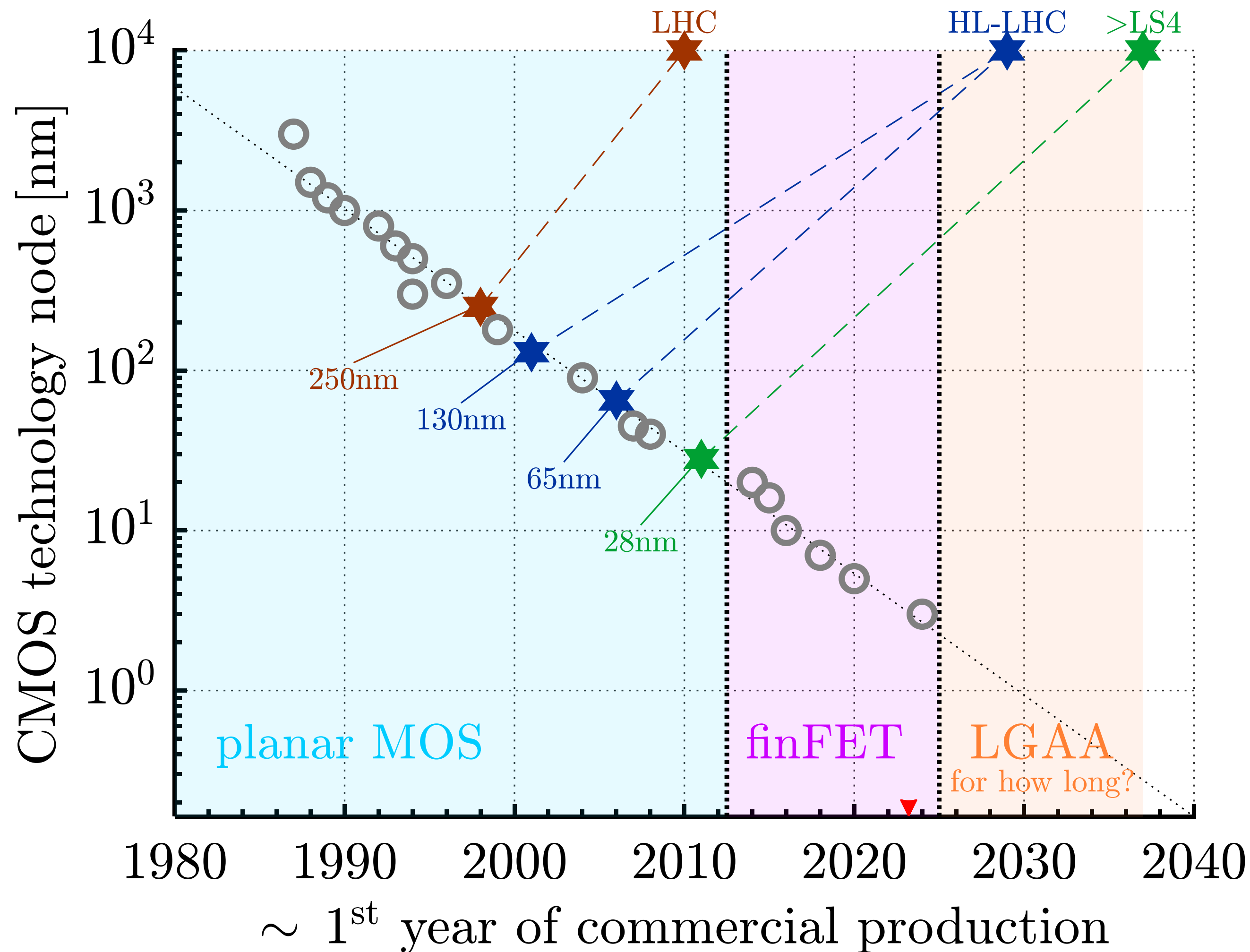
Radiation and magnetic tolerant DC-DC converters

LHCb Vertex Locator (VELOPIX)

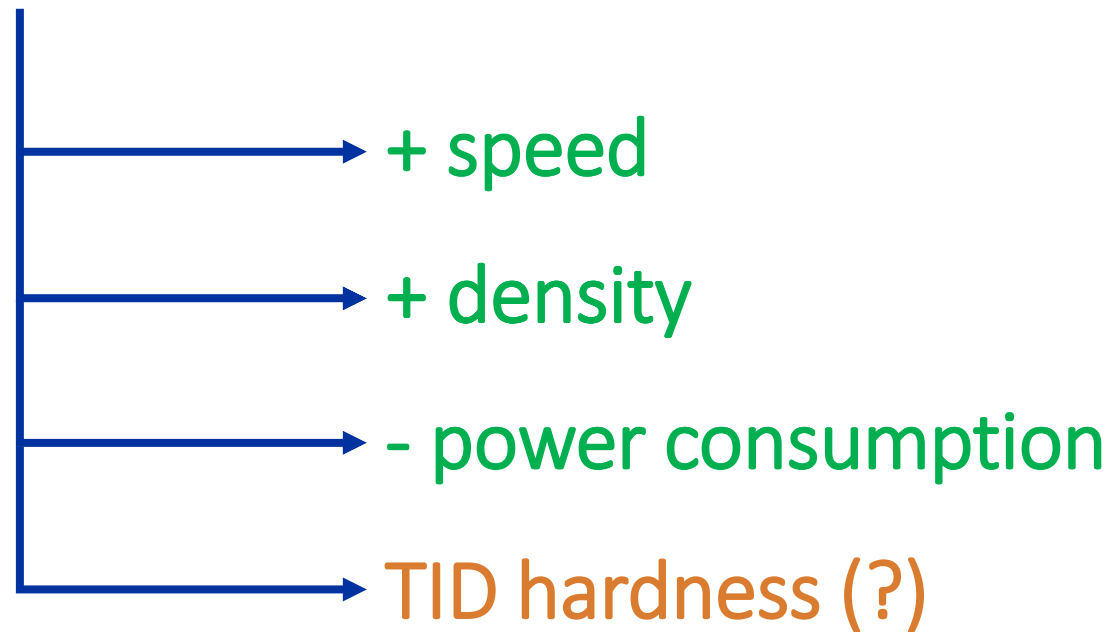


visit https://ep-ese.web.cern.ch/structure/section-ese-me for the full list of chips and projects

CERN & CMOS technology



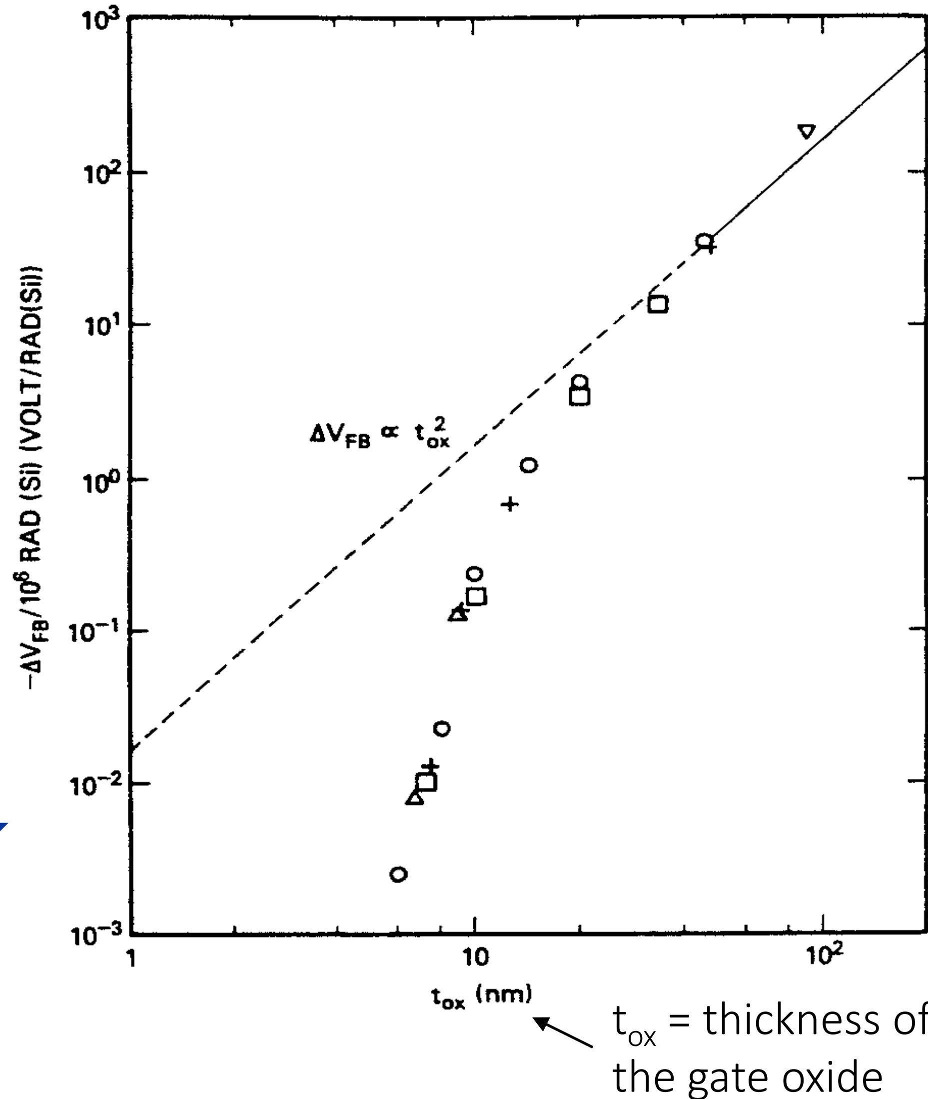
data from:
https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm
https://irds.ieee.org/editions/2022/more-moore


technology scaling
+ speed
+ density
- power consumption
TID hardness (?)

thin oxides are more rad-hard!!

Saks, N. S., et al. IEEE Trans. on Nucl. Sci. 31.6 (1984): 1249-1255.

increasing radiation hardness



t_{ox} = thickness of the gate oxide

threshold voltage

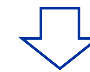
flatband voltage (sensitive to TID)

$$V_{TH} = V_{FB} + \ldots$$

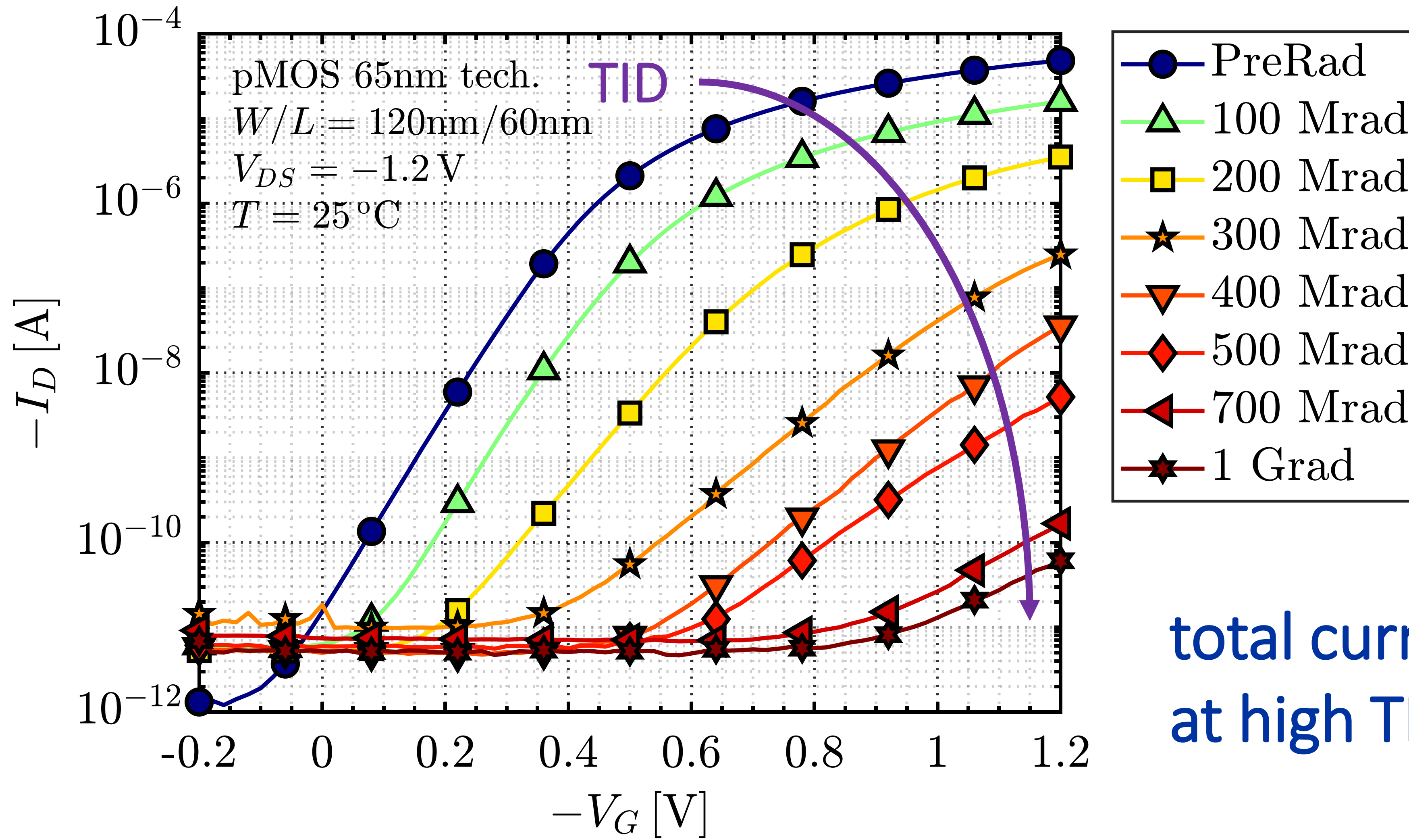
average charge density in t_{ox}

$$\Delta V_{TH}(TID) = \Delta V_{FB}(TID) = -\frac{\bar{\rho}_{OX}(TID)}{\epsilon_{OX}} t_{OX}^2$$

t_{ox} in 65nm node ≈ 2 nm

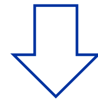


MOSFETs in 65nm CMOS technology should be extremely rad hard!



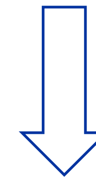
total current collapse at high TID!

why such a large degradation?



several oxides present in CMOS technology (not only the gate oxide)

much **thicker** than the gate oxide

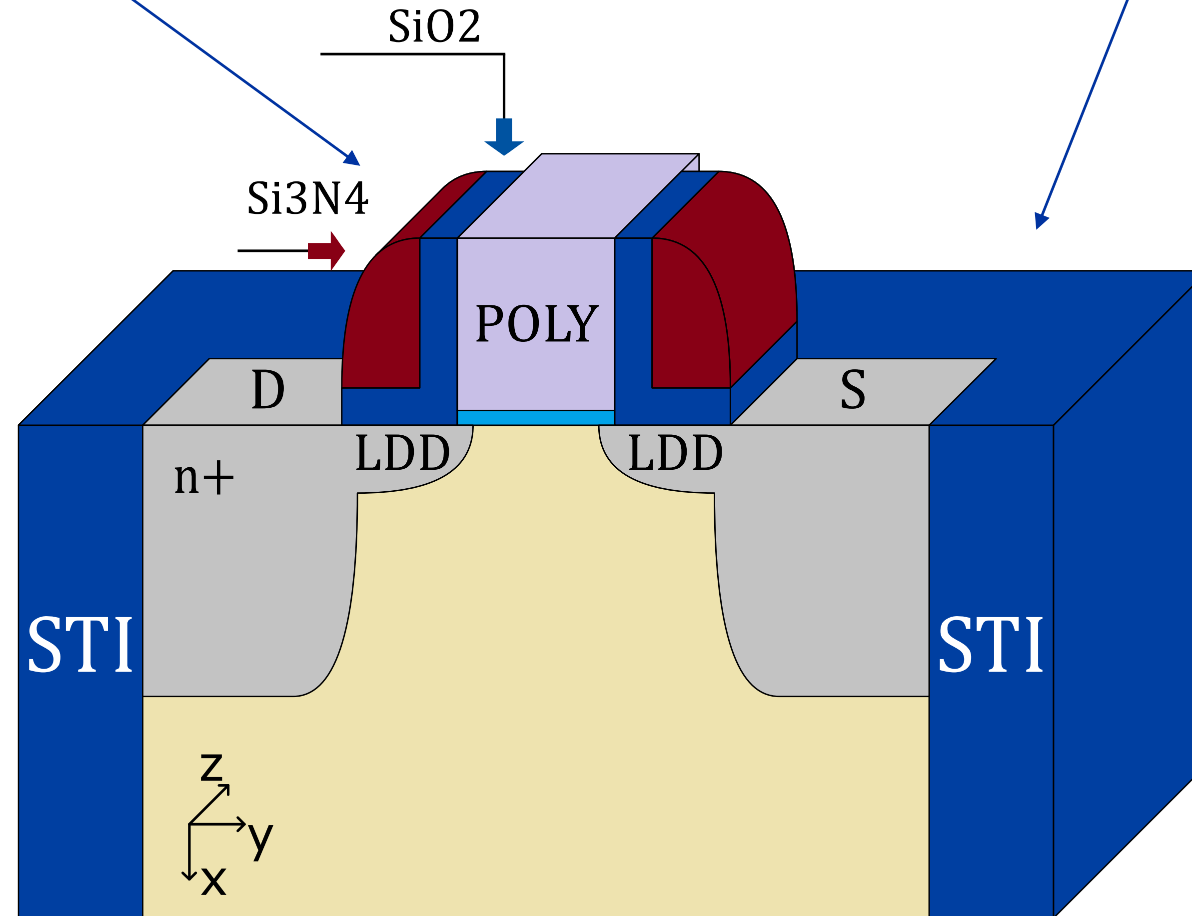


lower quality with respect to gate oxide ⇒ **rich in defects**

giulio.borghello@cern.ch | CERN EP-ESE-ME

Spacers: needed to create the Lightly Doped Source/Drain (LDD) extensions

Shallow Trench Isolation (STI): useful to isolate adjacent devices



DISCLAIMER

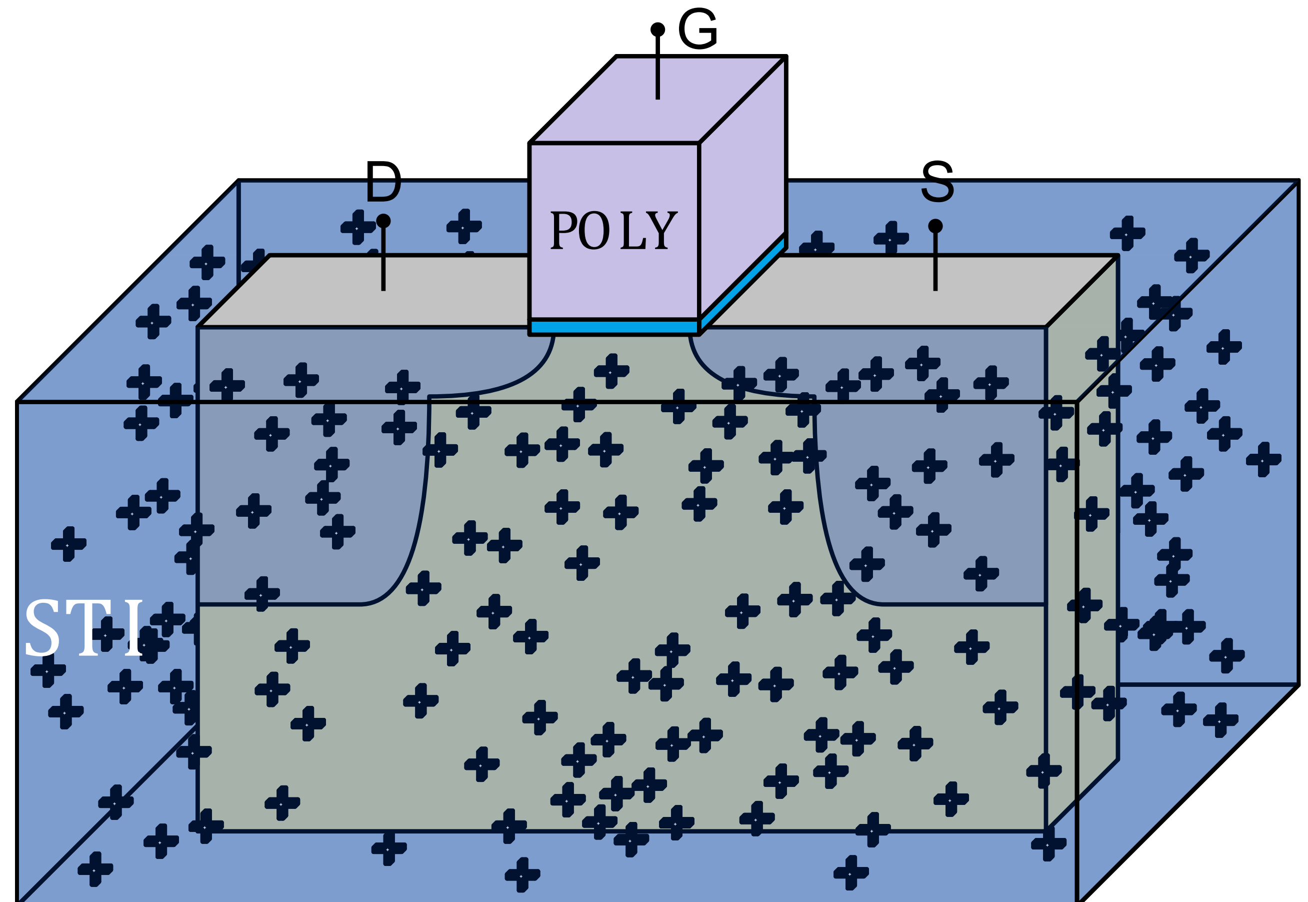
TID effects are affected by:

- technology-to-technology variability
- manufacturer-to-manufacturer variability
- fab-to-fab variability
- chip-to-chip variability
- lot-to-lot variability
- transistor-to-transistor variability

next slides will show what may happen to CMOS technology!

Shallow Trench Isolation (STI) oxide

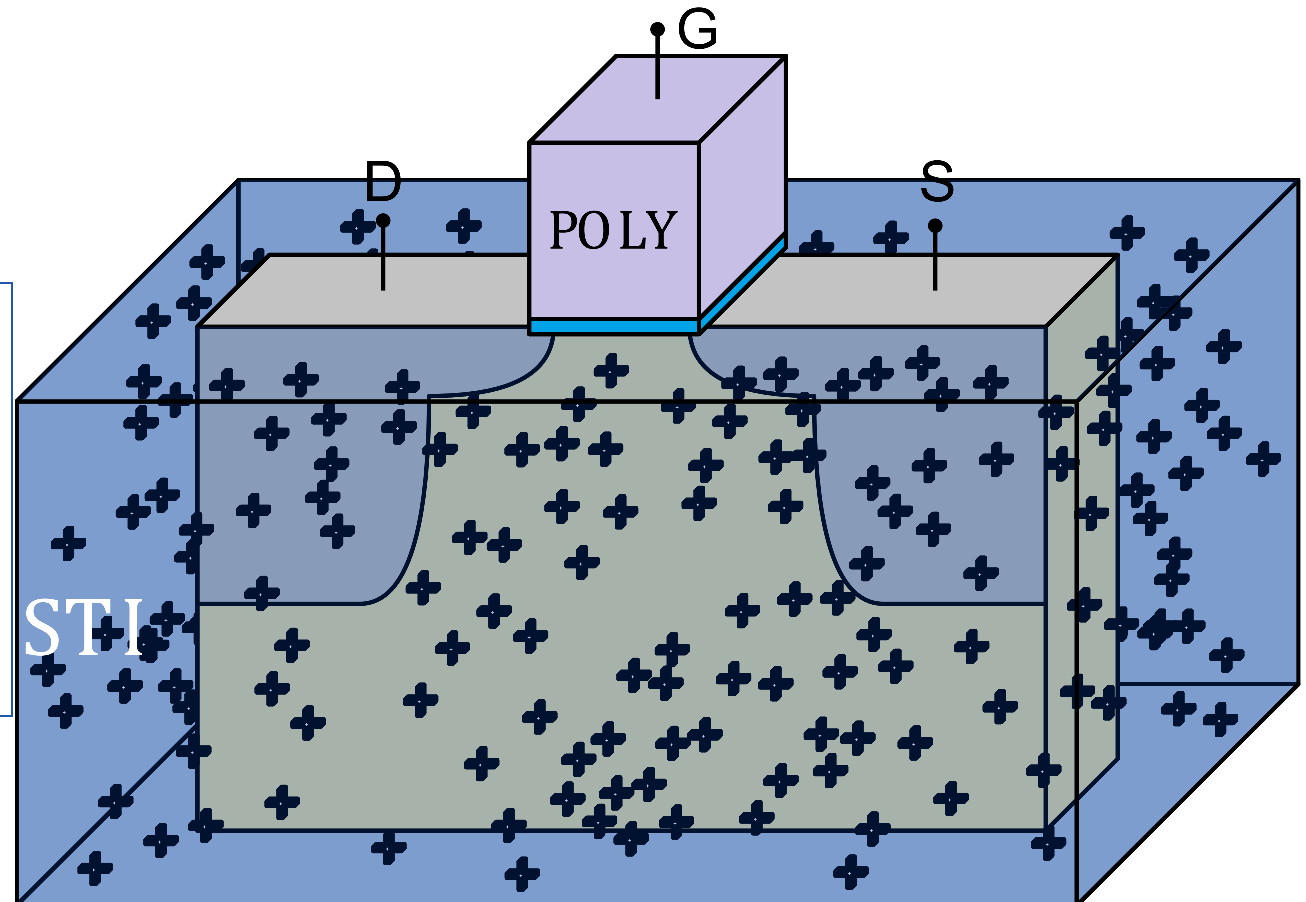
1. radiation-induced drain-to-source parasitic current
2. radiation-induced narrow channel effect (RINCE)
3. halo-enhanced robustness in short channels



Shallow Trench Isolation (STI) oxide

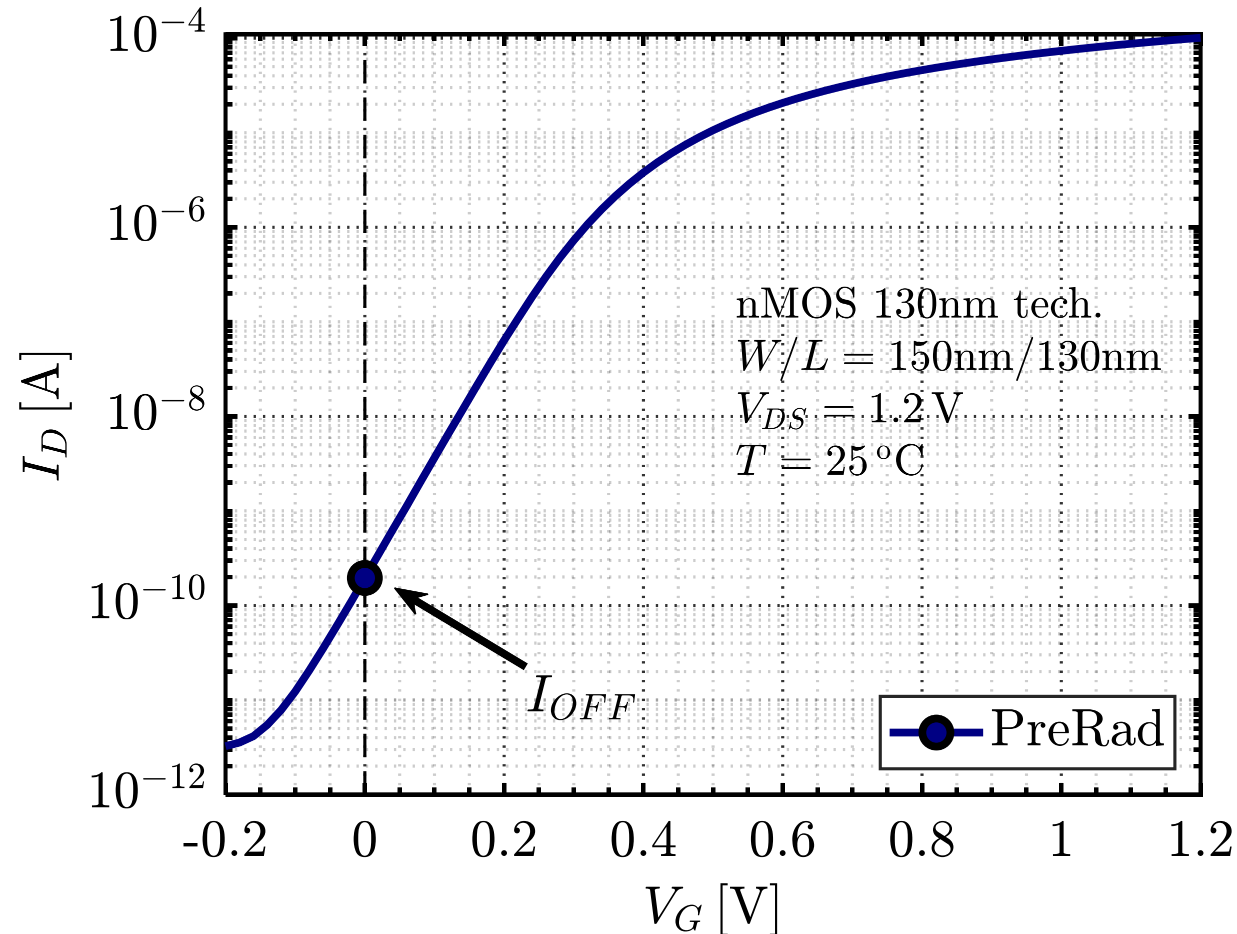
1. radiation-induced drain-to-source parasitic current

1. T. R. Oldham, et. al., "Post-Irradiation Effects in Field-Oxide Isolation Structures," in *TNS*, vol. 34, no. 6, pp. 1184-1189, Dec. 1987.
2. M. R. Shaneyfelt et. al, "Challenges in hardening technologies using shallow-trench isolation," in *TNS*, vol. 45, no. 6, pp. 2584-2592, Dec. 1998.
3. G. Niu et al., "Total dose effects on the shallow-trench isolation leakage current characteristics in a 0.35 um SiGe BiCMOS technology, in *TNS*, vol. 46, no. 6, pp. 1841-1847, Dec. 1999.
4. M. Turowski, et. al, "Nonuniform total-dose-induced charge distribution in shallow-trench isolation oxides," in *TNS*, vol. 51, no. 6, pp. 3166-3171, Dec. 2004.
5. I. S. Esqueda, et. al, "Two-dimensional methodology for modeling radiation-induced off-state leakage in CMOS technologies," in *TNS*, vol. 52, no. 6, pp. 2259-2264, Dec. 2005.
6. A. H. Johnston, et. al, "Total Dose Effects in CMOS Trench Isolation Regions," in *TNS*, vol. 56, no. 4, pp. 1941-1949, Aug. 2009.
7. Nadia Rezzak, et. al, “The sensitivity of radiation-induced leakage to STI topology and sidewall doping”, *Micr. Rel.*, Volume 51, Issue 5, 2011, Pages 889-894.
8. C. -M. Zhang et al., "Characterization and Modeling of Gigarad-TID-Induced Drain Leakage Current of 28-nm Bulk MOSFETs," in *TNS*, vol. 66, no. 1, pp. 38-47, Jan. 2019



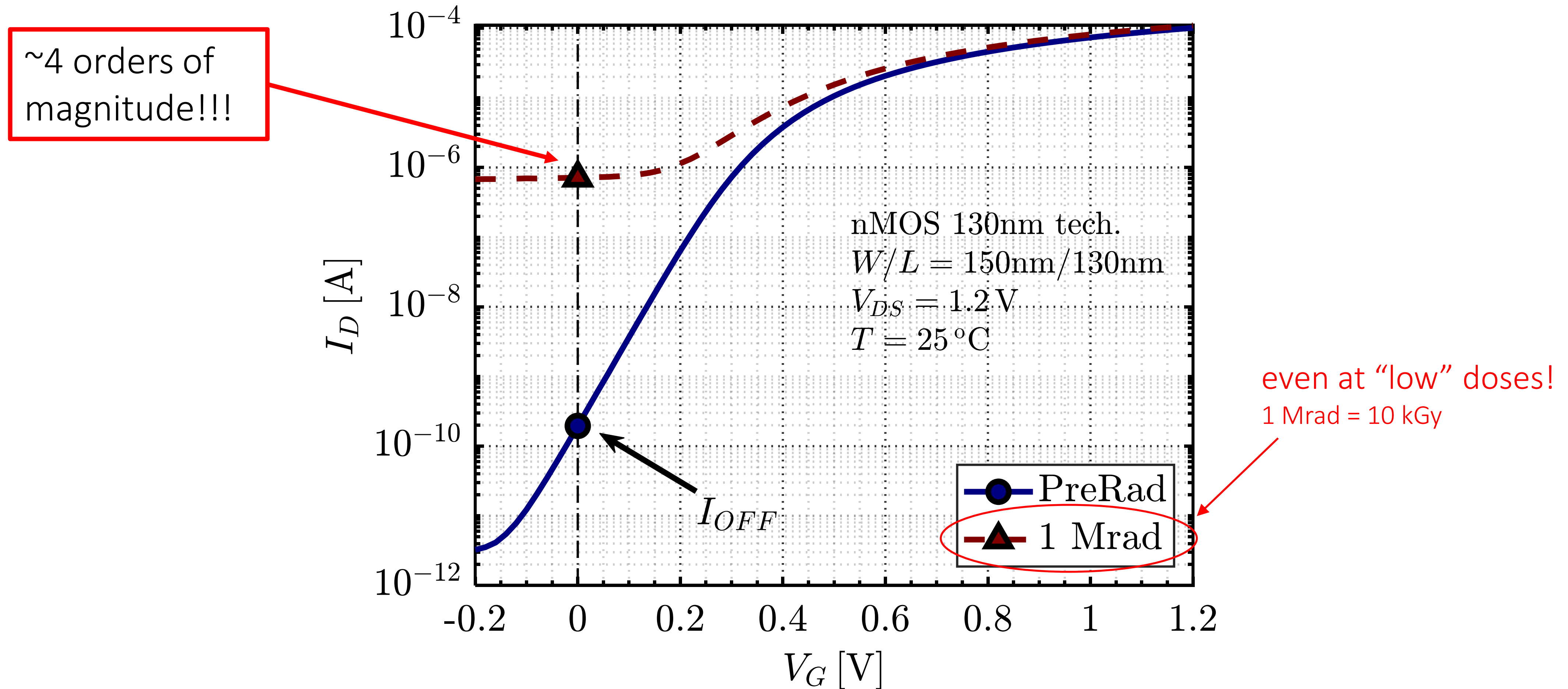
leakage current: $I_{OFF} = I_{DS}(V_{GS} = 0\ V, V_{DS} = V_{DD})$

(e.g., static power consumption of a CMOS inverter: $P_S = V_{DD} \times I_{OFF}$)

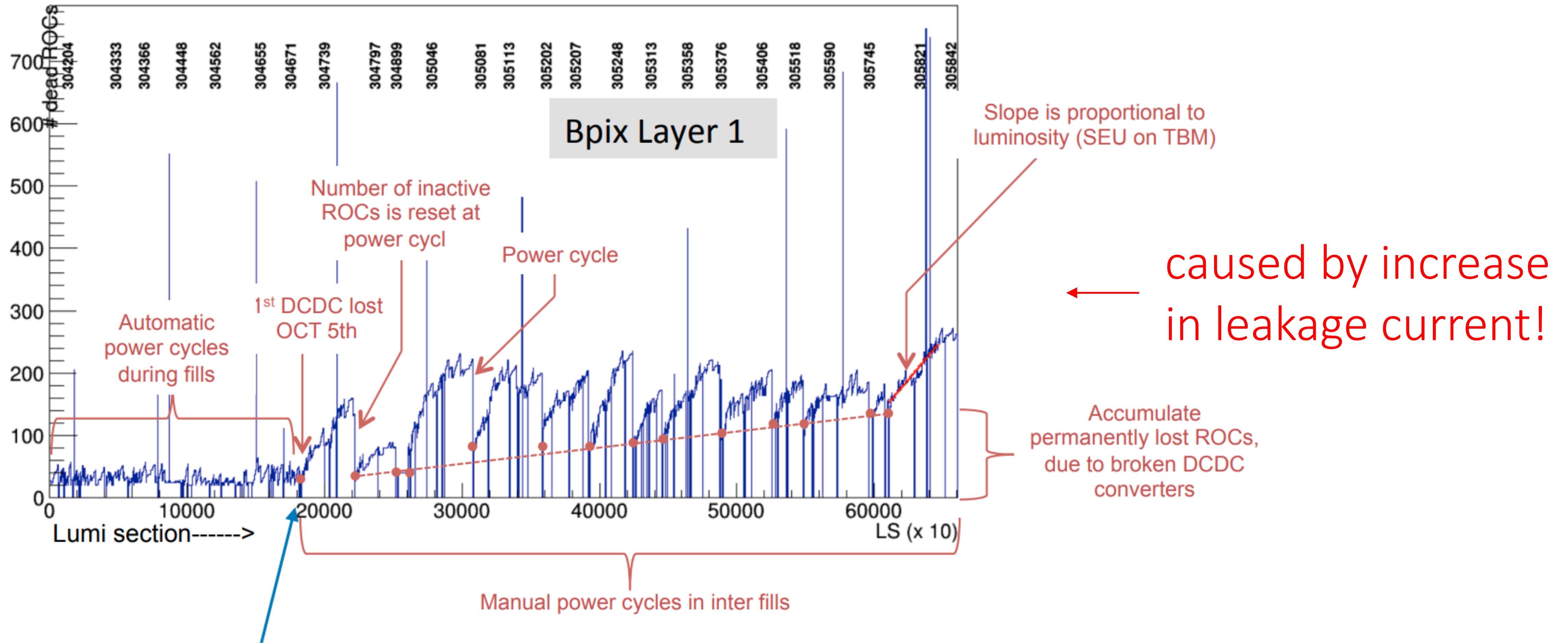


leakage current: $I_{OFF} = I_{DS}(V_{GS} = 0\ V, V_{DS} = V_{DD})$

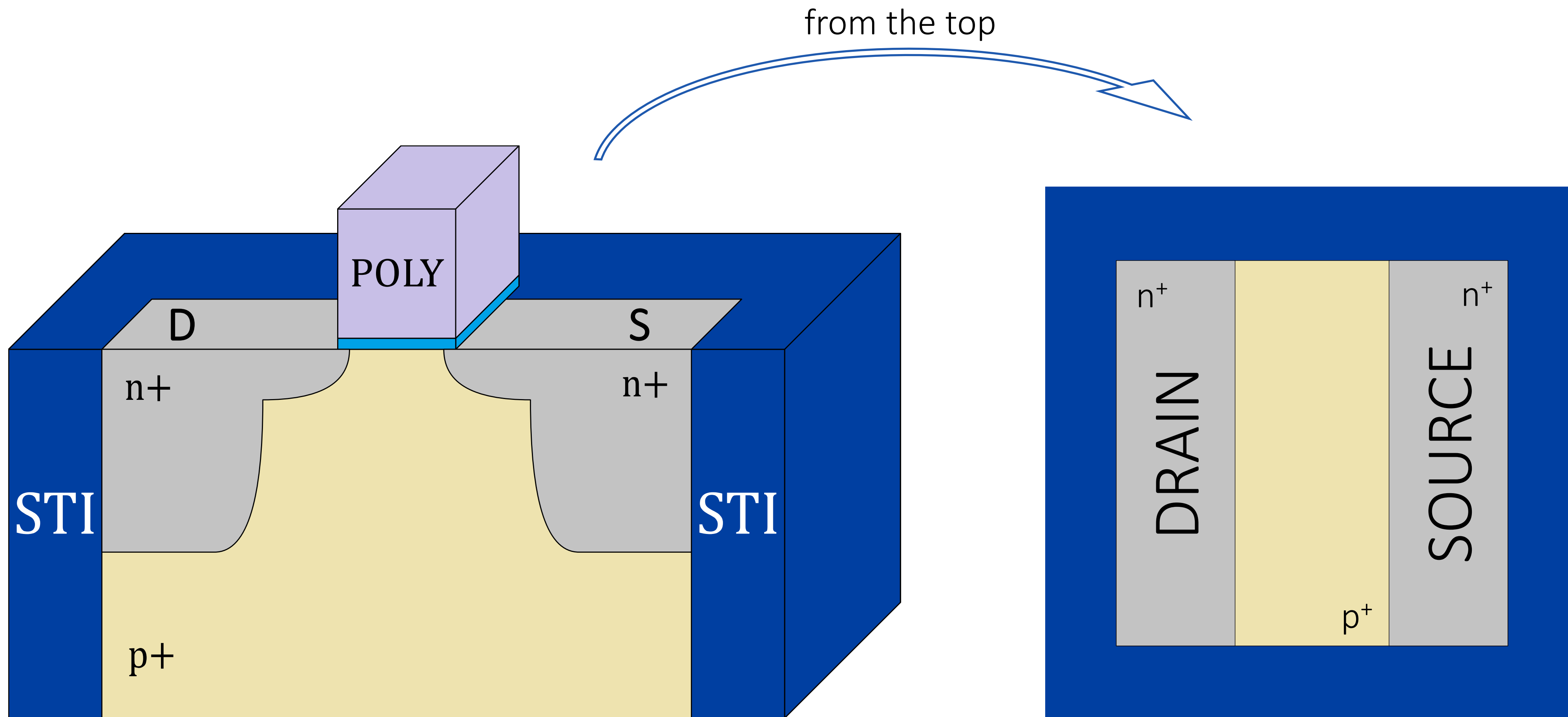
(e.g., static power consumption of a CMOS inverter: $P_S = V_{DD} \times I_{OFF}$)



failure of DCDC converters in the CMS pixel system during the 2017 run!



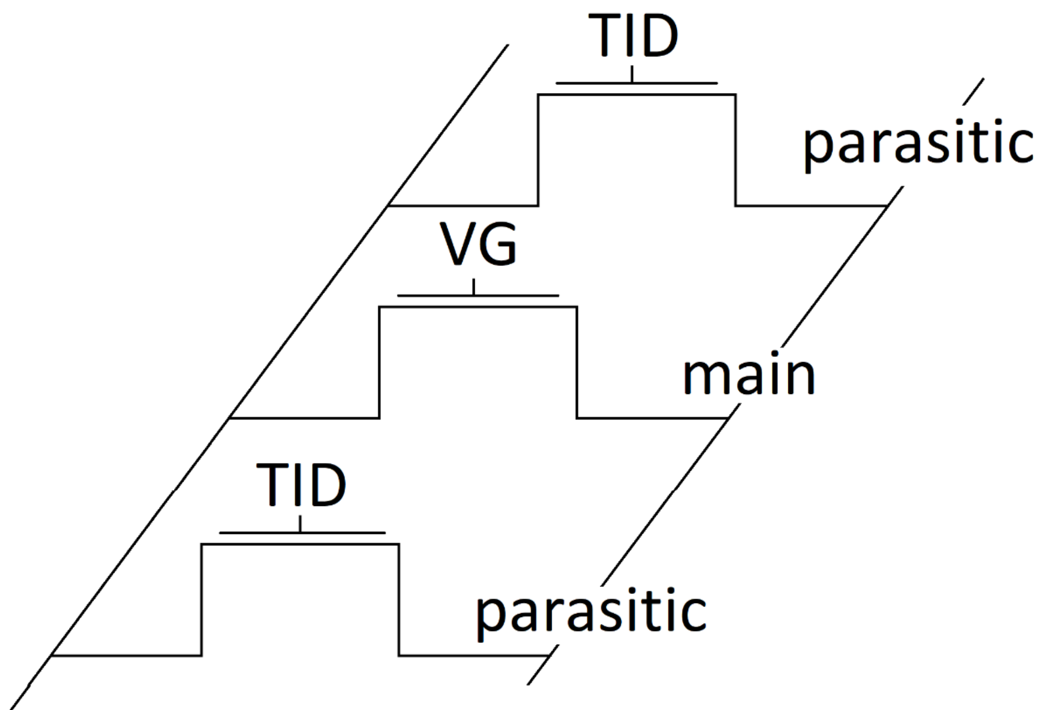
https://indico.desy.de/event/21211/contributions/42055/attachments/26775/33802/KatjaKlein_12thDetectorWorkshop_14032019.pdf
https://espace.cern.ch/project-DCDC-new/Shared%20Documents/SummaryMeasurements18.pdf
https://espace.cern.ch/project-DCDC-new/Shared%20Documents/Report_IRRAD_tests.pdf
https://indico.cern.ch/event/788031/attachments/1794169/2923948/ESE_seminar_Feb19_talk.pdf

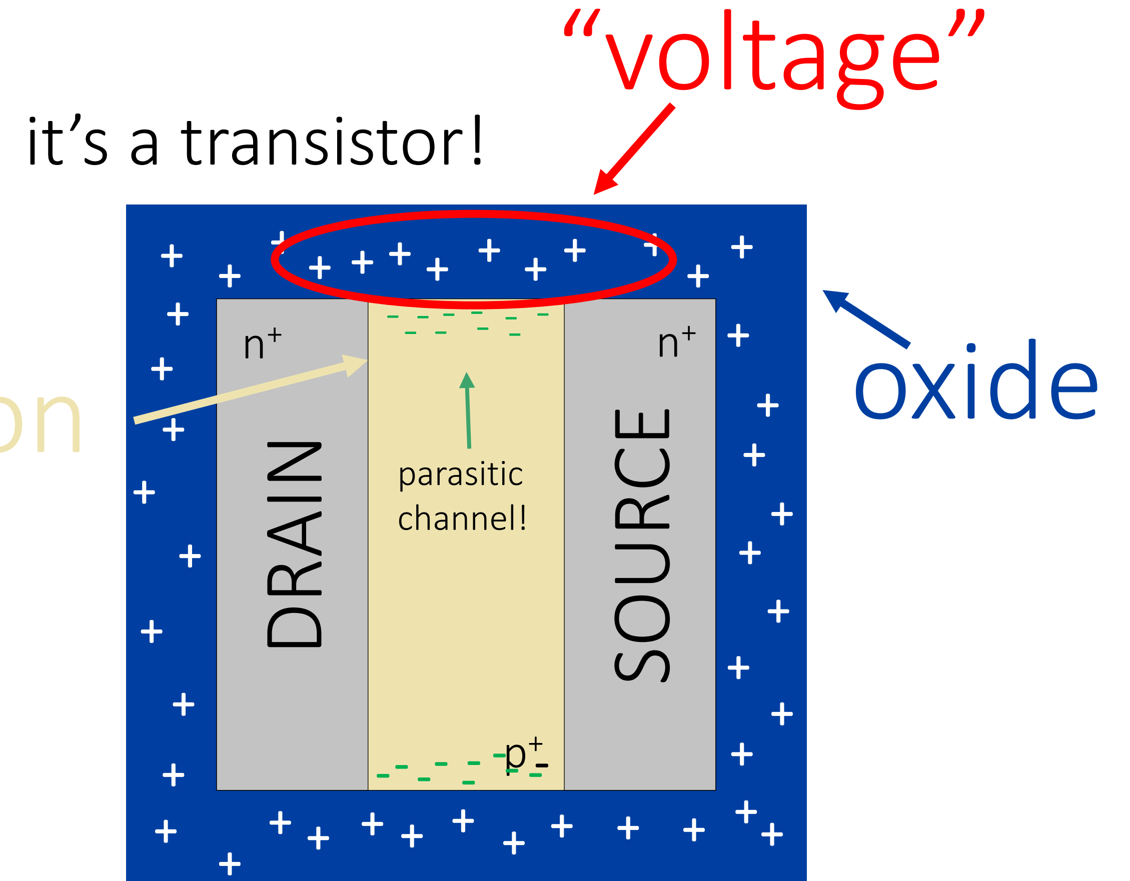

from the top
POLY
D
S
n+
n+
STI
STI
p+
n+
n+
DRAIN
SOURCE
p+

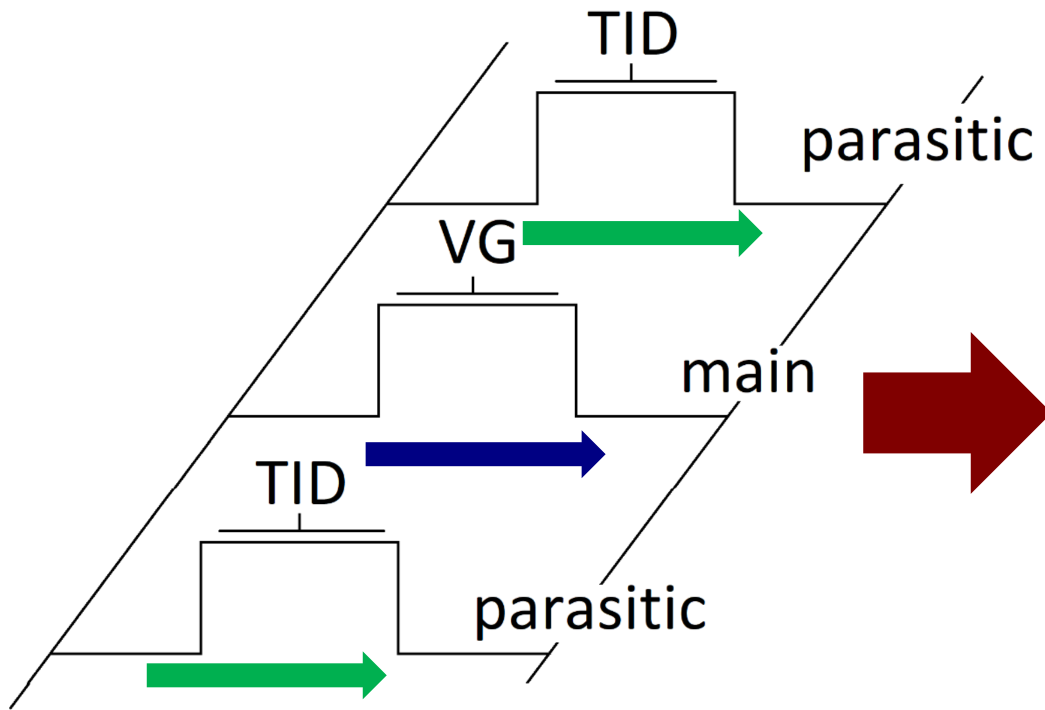
TID-induced positive charge in the oxide

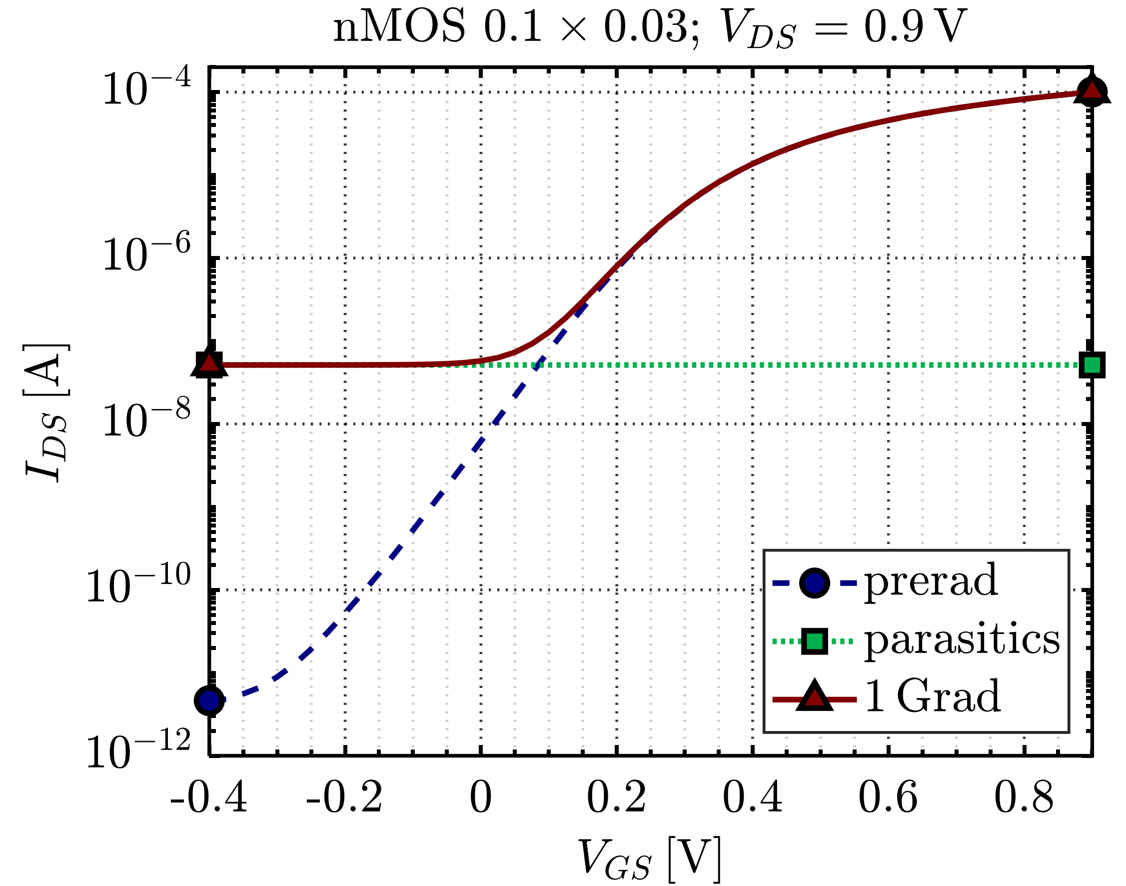
we are only interested in the charge that faces the channel

positive charge attracts electrons -> **problem only in nMOS**!

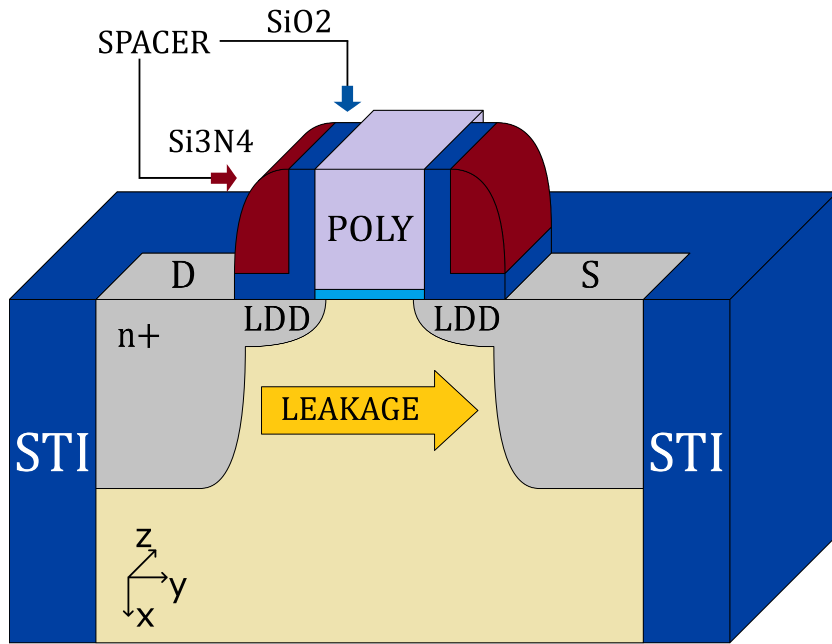




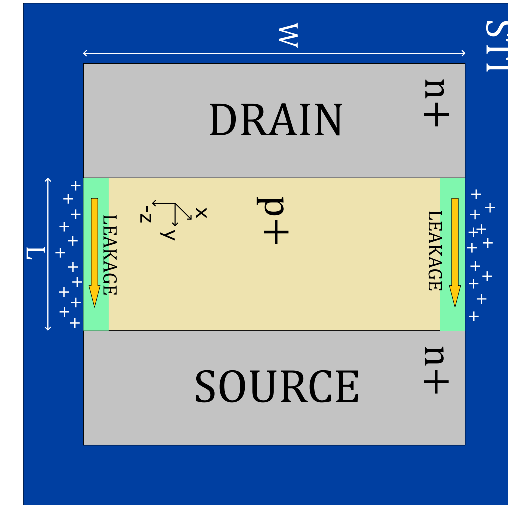

TID
parasitic
VG
main
TID
parasitic


nMOS 0.1 × 0.03; V_{DS} = 0.9 V
I_{DS} [A]
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
-0.4
-0.2
0
0.2
0.4
0.6
0.8
V_{GS} [V]
prerad
parasitics
1 Grad

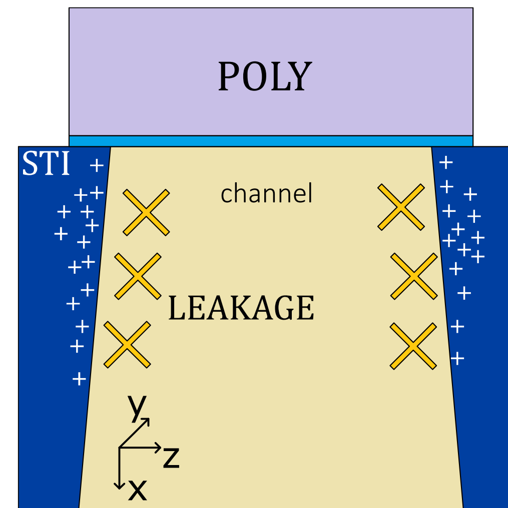
The charge is trapped all along the STI!

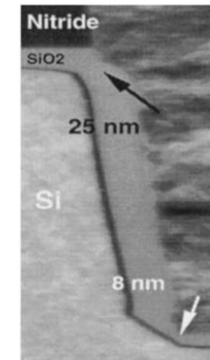


top view

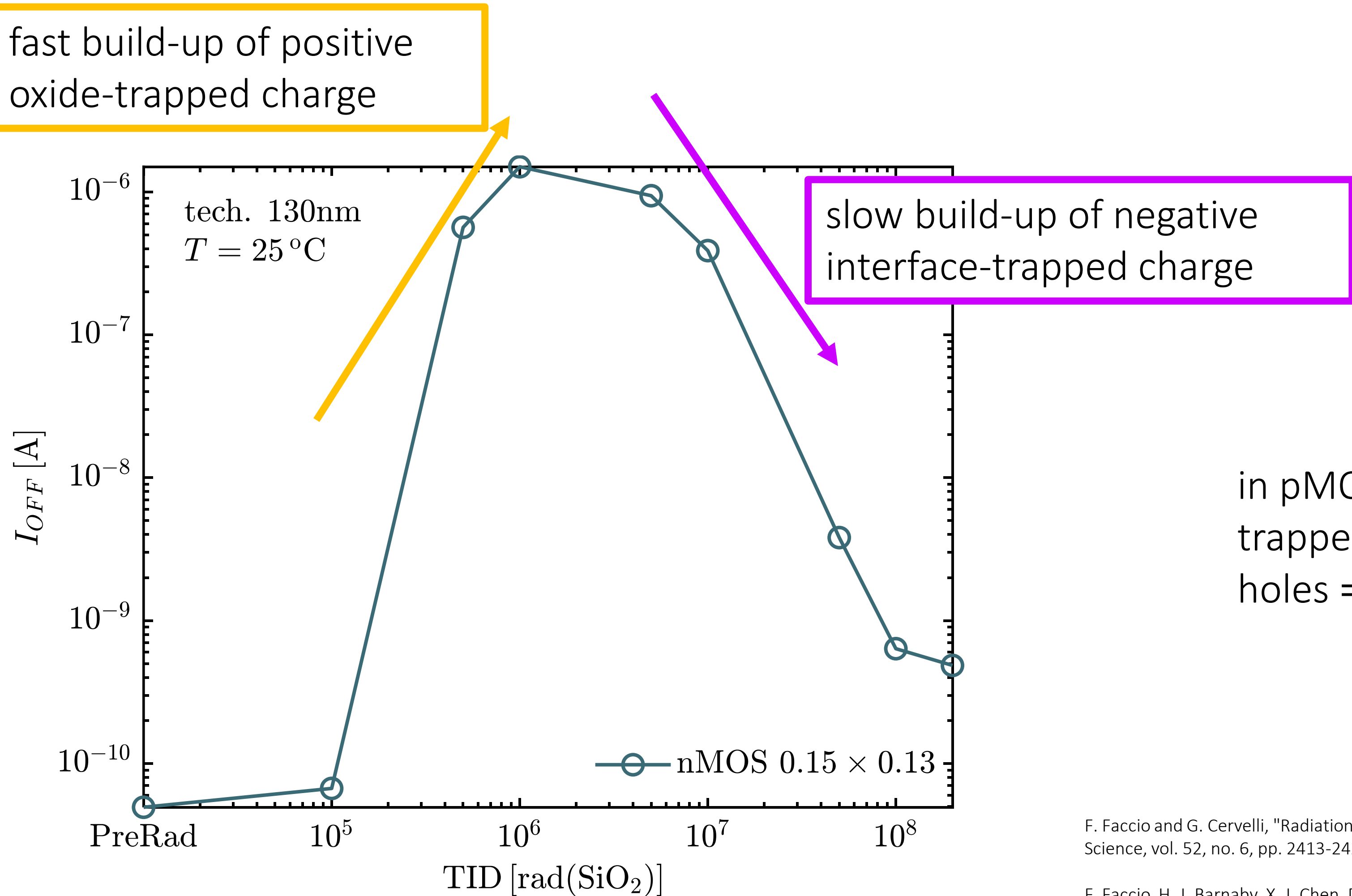


in the channel





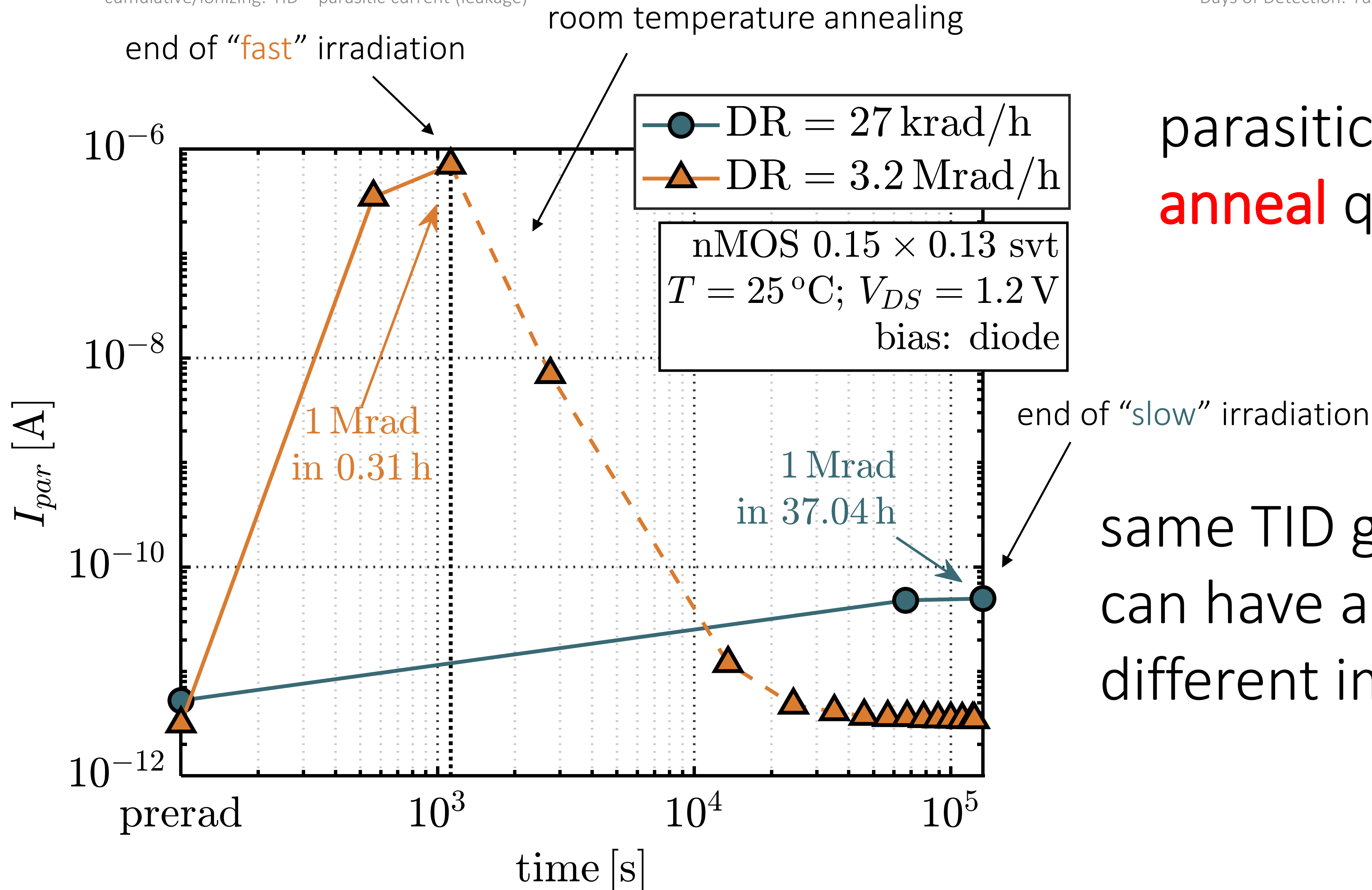
Sallagoity, P., et al. "STI process steps for sub-quarter micron CMOS." *Microelectronics Reliability* 38.2 (1998): 271-276.



in pMOS both oxide- and interface-trapped charge are positive and repel holes ⇒ no parasitic paths

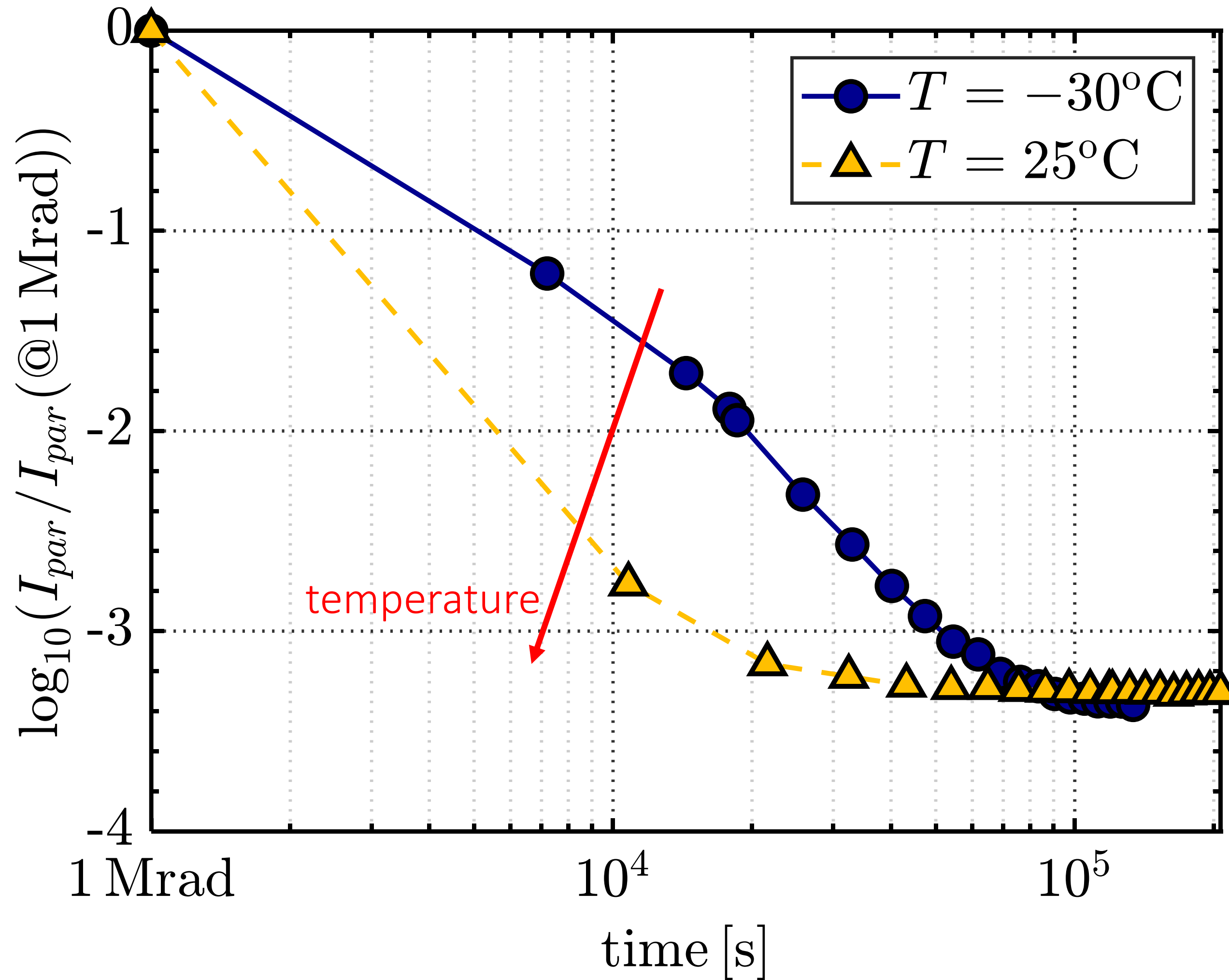
F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," in IEEE Transactions on Nuclear Science, vol. 52, no. 6, pp. 2413-2420, Dec. 2005

F. Faccio, H. J. Barnaby, X. J. Chen, D. M. Fleetwood, L. Gonella, M. McLain, and R. D. Schrimpf. "Total ionizing dose effects in shallow trench isolation oxides." In: Microelectronics Reliability 48.7 (2008), pp. 1000–1007.

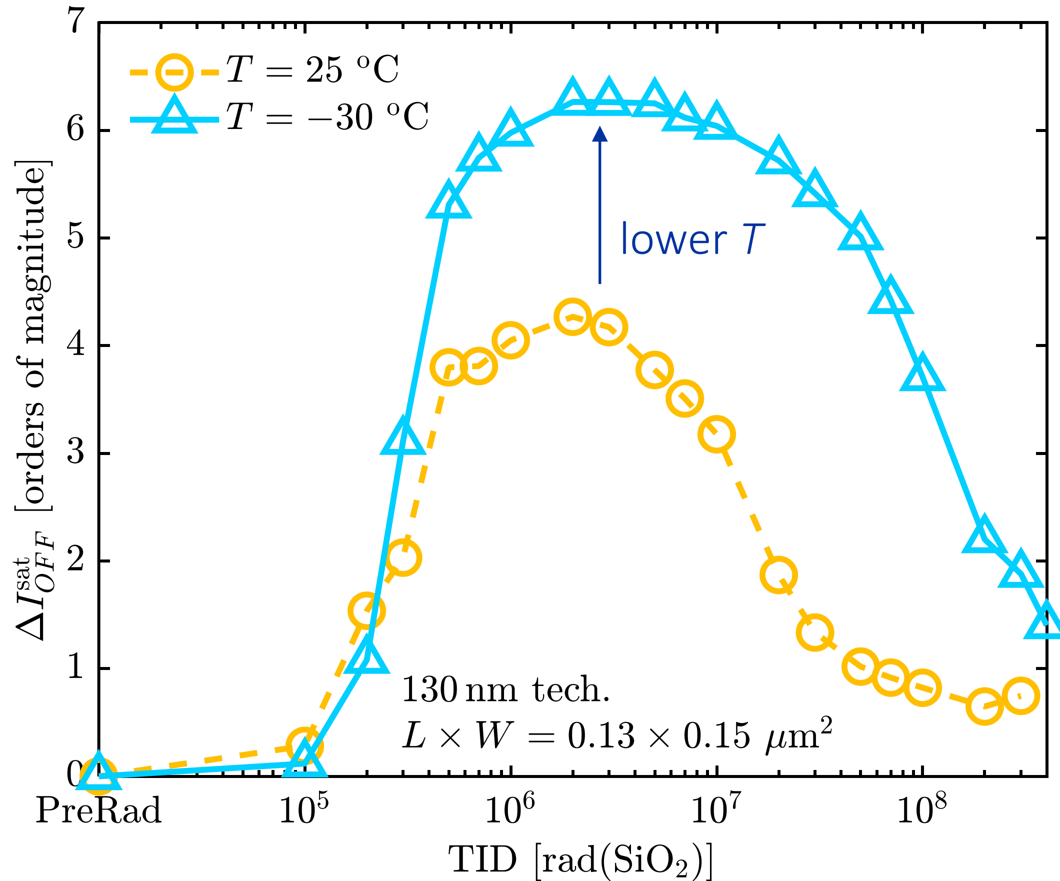


parasitic current can **anneal** quickly!

same TID given fast or slow can have a completely different impact!



high temperature accelerates annealing!



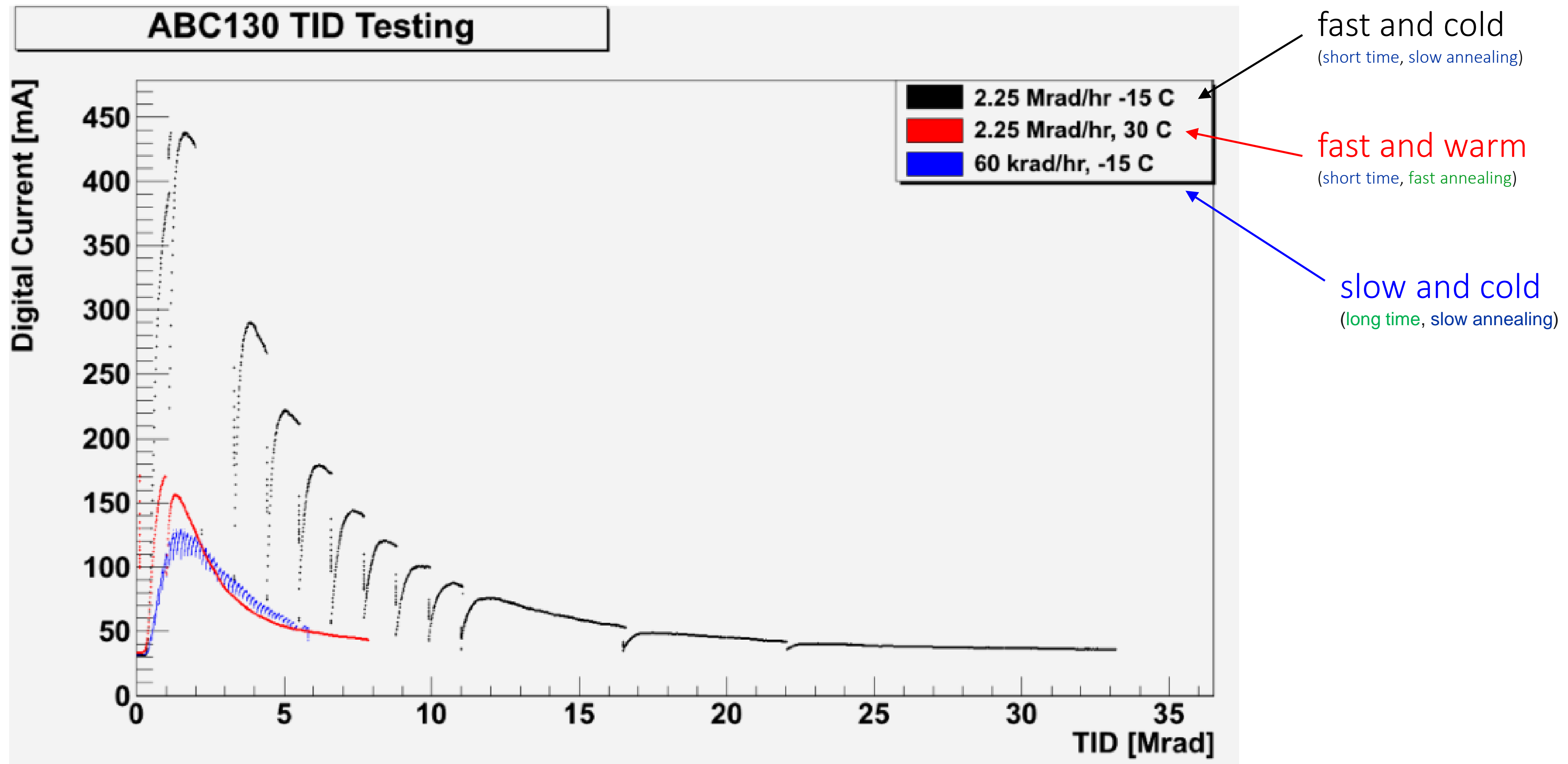
G. Borghello, Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses. Diss. Udine U., 2019

low temperature can increase the peak of leakage

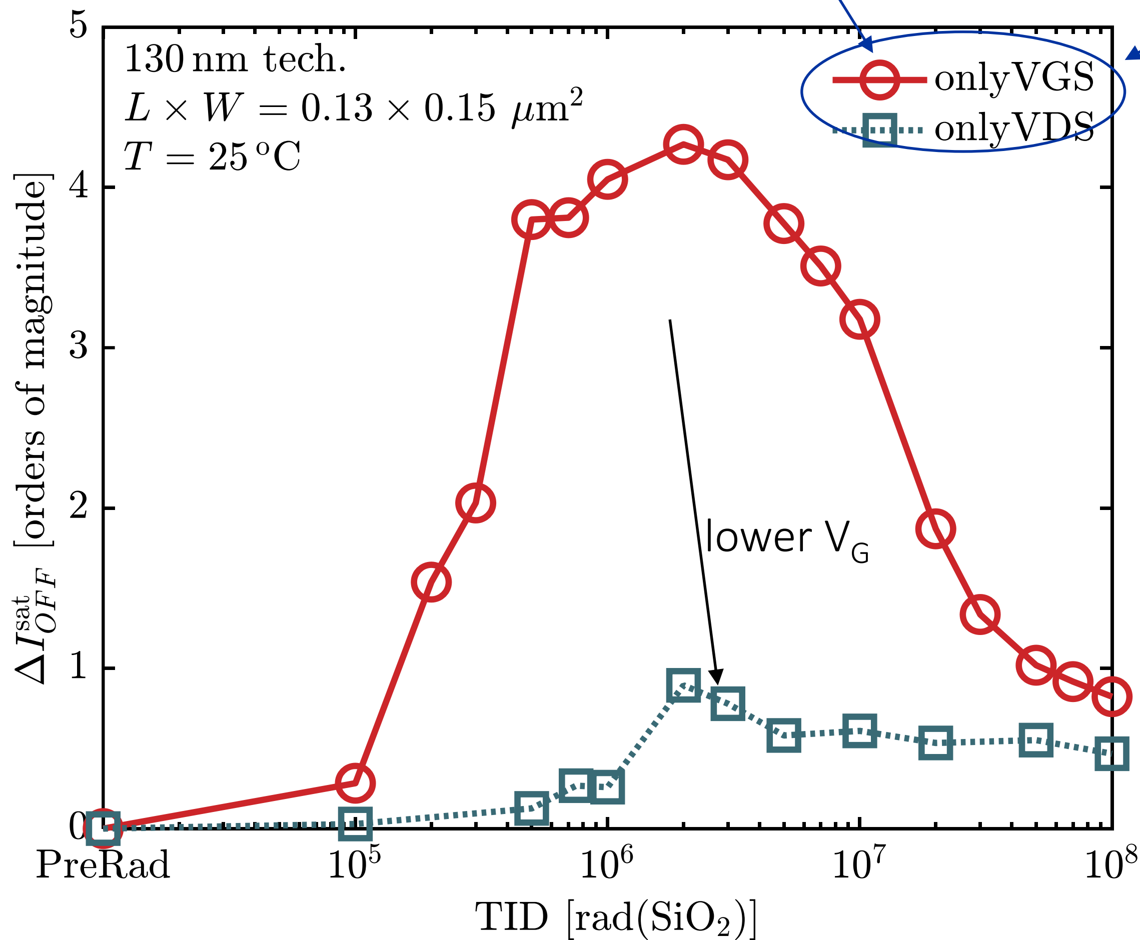
- slower annealing of positive charge in the oxide
- slower build-up of negative charge at the interface

the inner layers of particle detectors are usually kept at ~-30 °C!

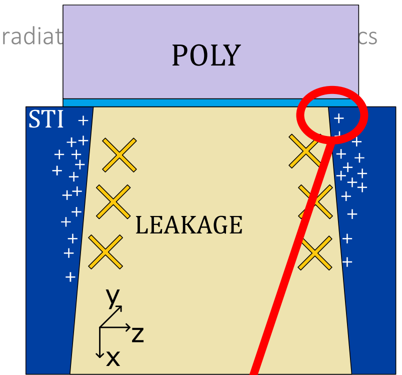
logic core current consumption of the ABC130 at different *T* and dose rates
(courtesy F. Anghinolfi and ABC130 Team)



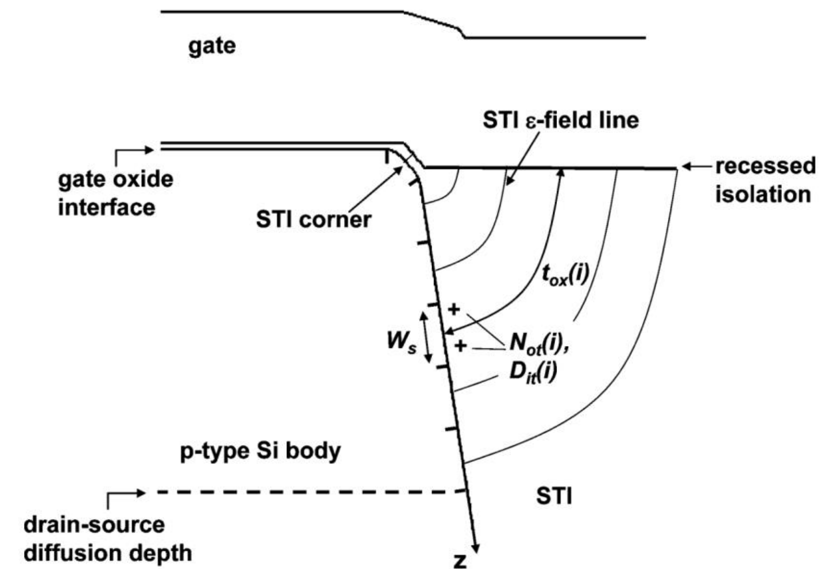
voltage applied to devices during irradiation



onlyVGS: $V_{GS} = 1.2\ V$
onlyVDS: $V_{GS} = 0\ V$



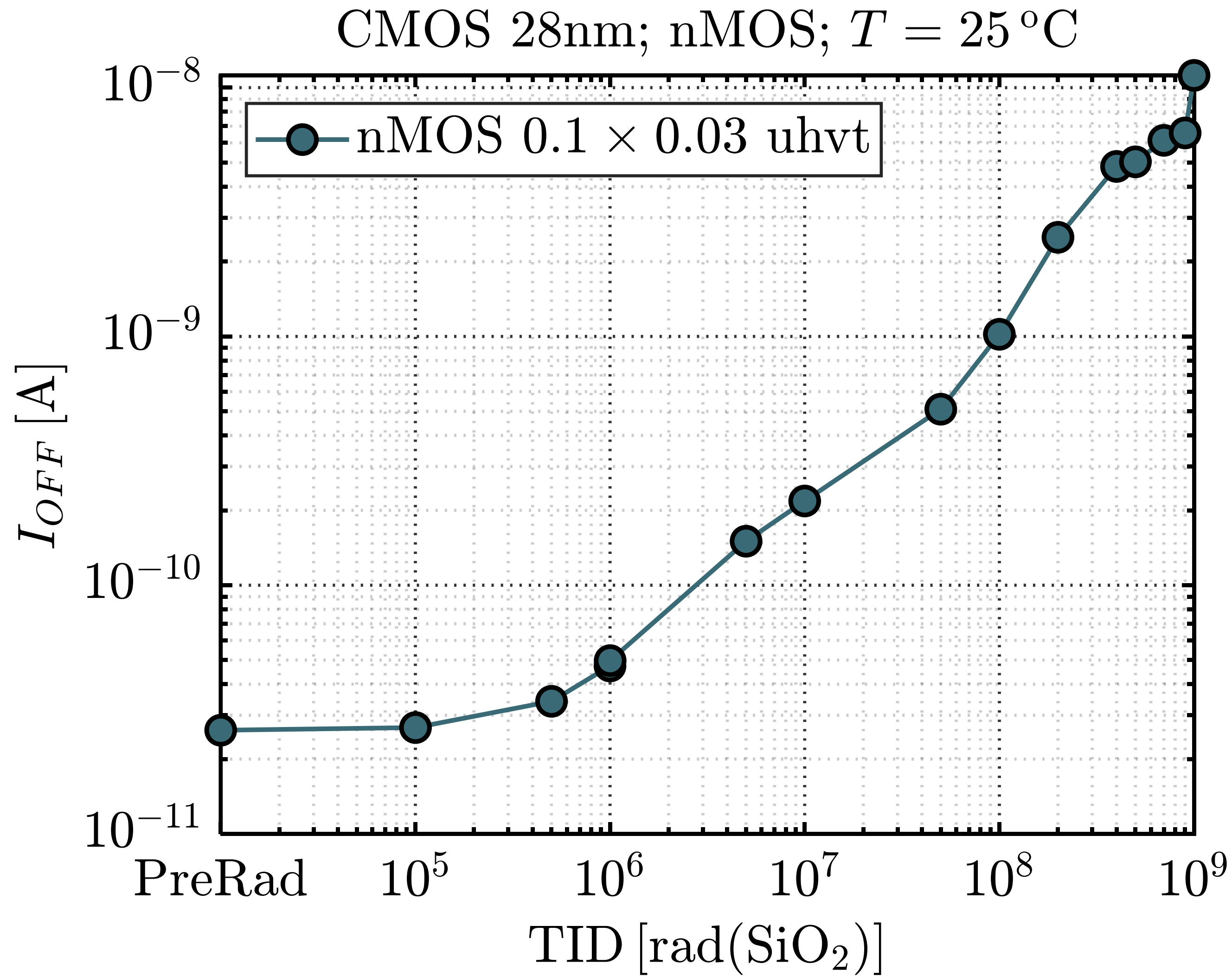
V_G changes the electric field in the corner of the STI



bias applied during exposure can significantly change the radiation response!!

H. J. Barnaby, et al., "Modeling Ionizing Radiation Effects in Solid State Materials and CMOS Devices," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 8, pp. 1870-1883, Aug. 2009

G. Borghello, Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses. Diss. Udine U., 2019

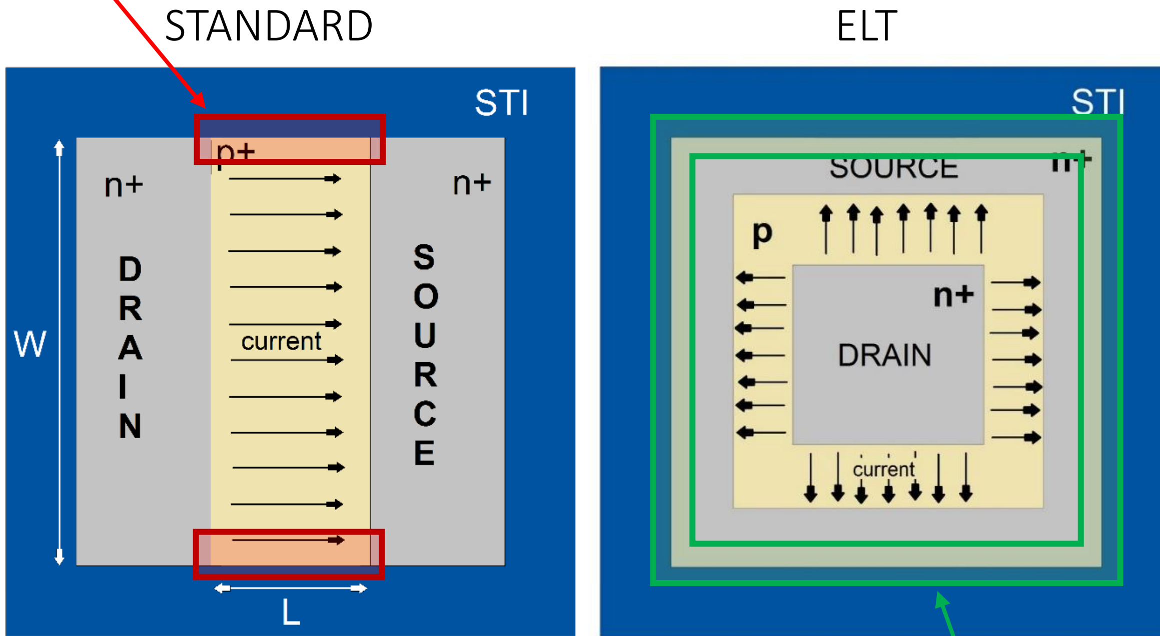


monotonic I_{OFF}(TID) increase for some technology!

Enclosed Layout Transistor (ELT)

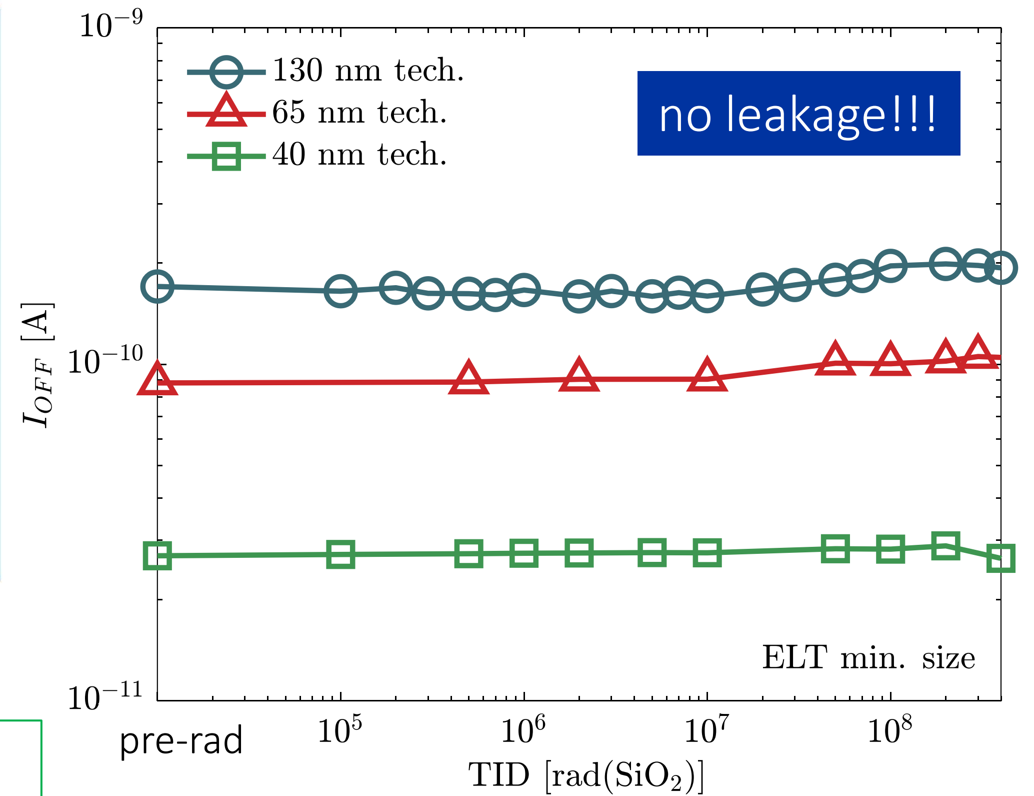
the STI faces the channel

NOT AVAILABLE IN 28nm and smaller nodes!



MOSFET TOP VIEW

the STI does not face the channel!



3 fabrication plants (Fab): A, B and C

nMOS 130 nm
0.15 × 0.13

I_{OFF}^{sat} [A]

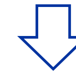
TID [rad(SiO_2)]

PreRad, 10^5, 10^6, 10^7, 10^8

10^{-5}, 10^{-6}, 10^{-7}, 10^{-8}, 10^{-9}, 10^{-10}, 10^{-11}

Fab; Date; T [°C]; Bias
- A; 2014/11; 25; diode
- A; 2016/01; 25; diode
- A; 2016/09; 25; diode
- A; 2017/02; 25; diode
- A; 2017/10; 25; diode
- A; 2017/11; 25; diode
- A; 2018/12; 25; diode
- A; 2019/08; 25; diode
- A; 2020/02; 25; diode
- B; 2016/12; 25; diode
- B; 2019/07; 25; diode
- B; 2020/03; 25; diode
- C; 2014/08; 25; EField
- C; 2018/07; 25; diode
- C; 2019/10; 25; diode

very different behaviour even for nominally identical devices produced in different fabs!!



this variability is caused by small differences in the STI fabrication process*

extremely difficult to define a “typical behaviour” of any given technology**

any new lot of any technology must be tested for leakage current!

Termo, G., et al. "Fab-to-fab and run-to-run variability in 130 nm and 65 nm CMOS technologies exposed to ultra-high TID." *Journal of Instrumentation* 18.01 (2023)

*F. T. Brady, et al. “A scalable, radiation hardened shallow trench isolation.” In: IEEE Transactions on Nuclear Science 46.6 (Dec. 1999), pp. 1836–1840.
*Z. Hu, Z. Liu, et al. “Impact of within-wafer process variability on radiation response.” In: Microelectronics Journal 42.6 (2011), pp. 883–888.

**this is true for any TID-induced effect

SUMMARY

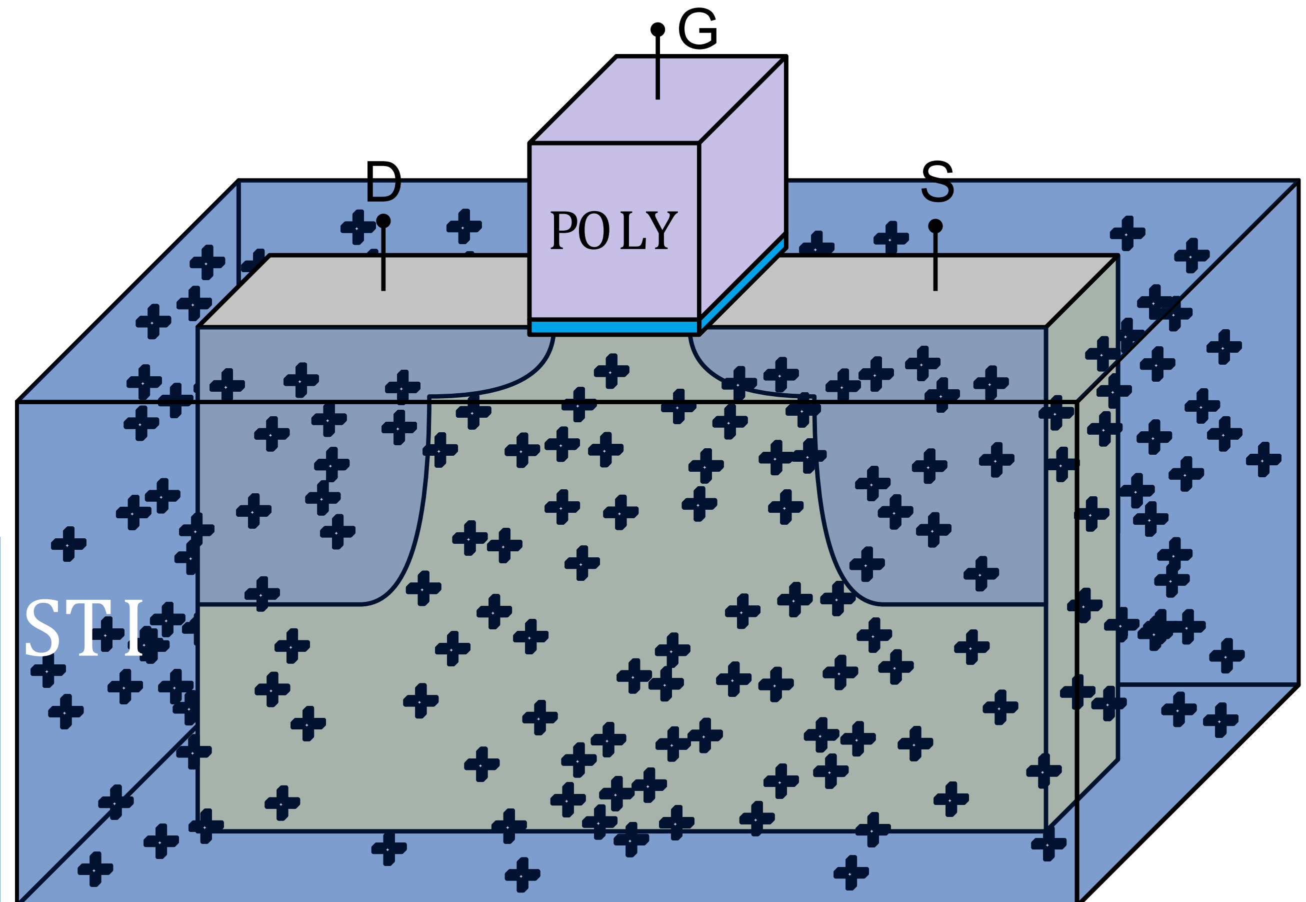
- I_{OFF} can increase of several orders of magnitude even for TID < 1 Mrad
- it is caused by positive oxide-trapped charge in the STI of nMOS
- pMOS are not affected by this problem
- bias and temperature can have a significant impact
- extremely process-dependent (huge variability!)

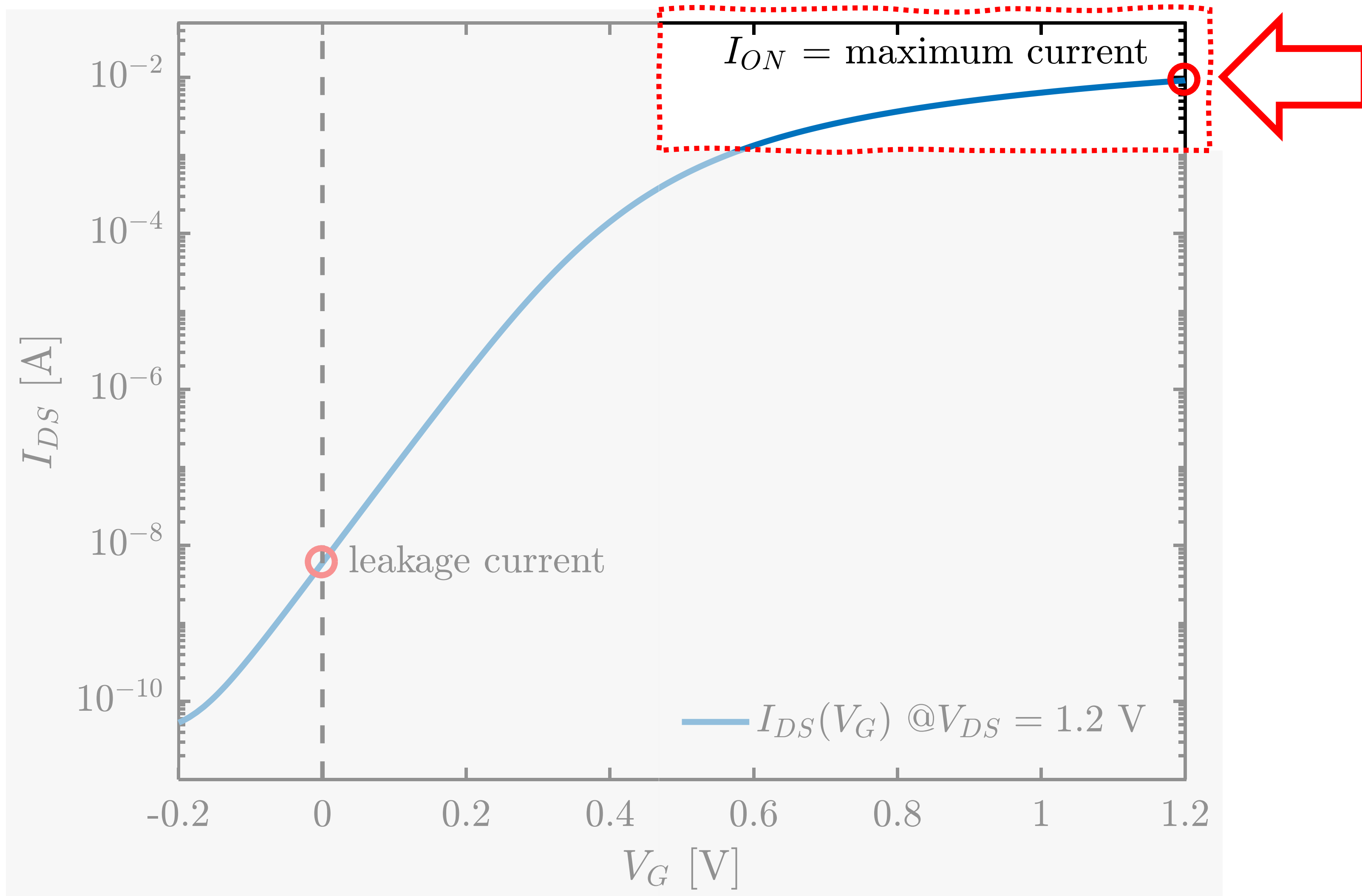
Shallow Trench Isolation (STI) oxide

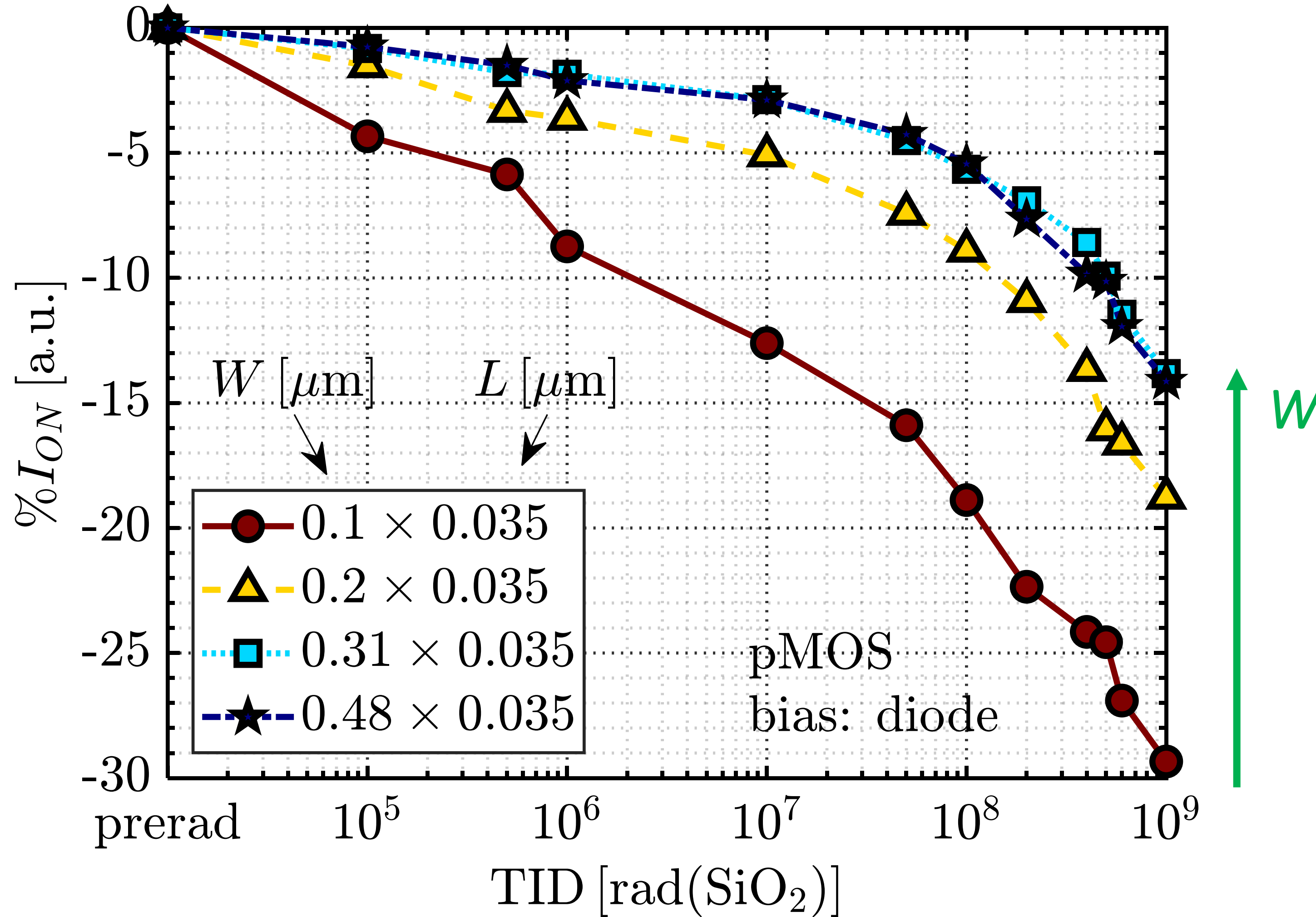
1. radiation-induced drain-to-source **parasitc** current

2. radiation-induced narrow channel effect (RINCE)

1. Faccio, Federico, and Giovanni Cervelli. "Radiation-induced edge effects in deep submicron CMOS transistors." *IEEE Transactions on Nuclear Science* 52.6 (2005): 2413-2420.
2. Gaillardin, M., et al. "Enhanced Radiation-Induced Narrow Channel Effects in Commercial ${\hbox {0.18}}~\mu $ m Bulk Technology." *IEEE Transactions on Nuclear Science* 58.6 (2011): 2807-2815.
3. Faccio, F., et al. "Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs." *IEEE Transactions on Nuclear Science* 62.6 (2015): 2933-2940.
4. Borghello, G., et al. "Ionizing radiation damage in 65 nm CMOS technology: Influence of geometry, bias and temperature at ultra-high doses." *Microelectronics Reliability* 116 (2021): 114016.




I_{ON} = maximum current
leakage current
$I_{DS}(V_G)$ @V_{DS} = 1.2 V
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
I_{DS} [A]
-0.2
0
0.2
0.4
0.6
0.8
1
1.2
V_G [V]



larger degradation in narrow channel devices!

W

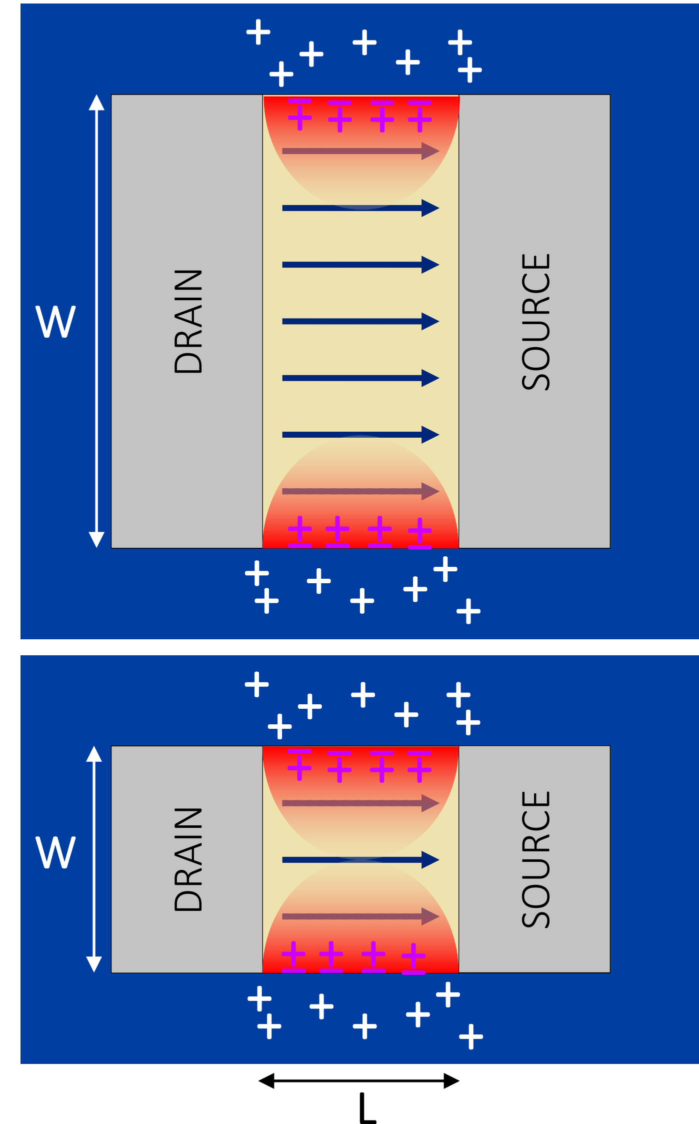
- two transistors:
  - same channel length *L*
  - different channel width *W*

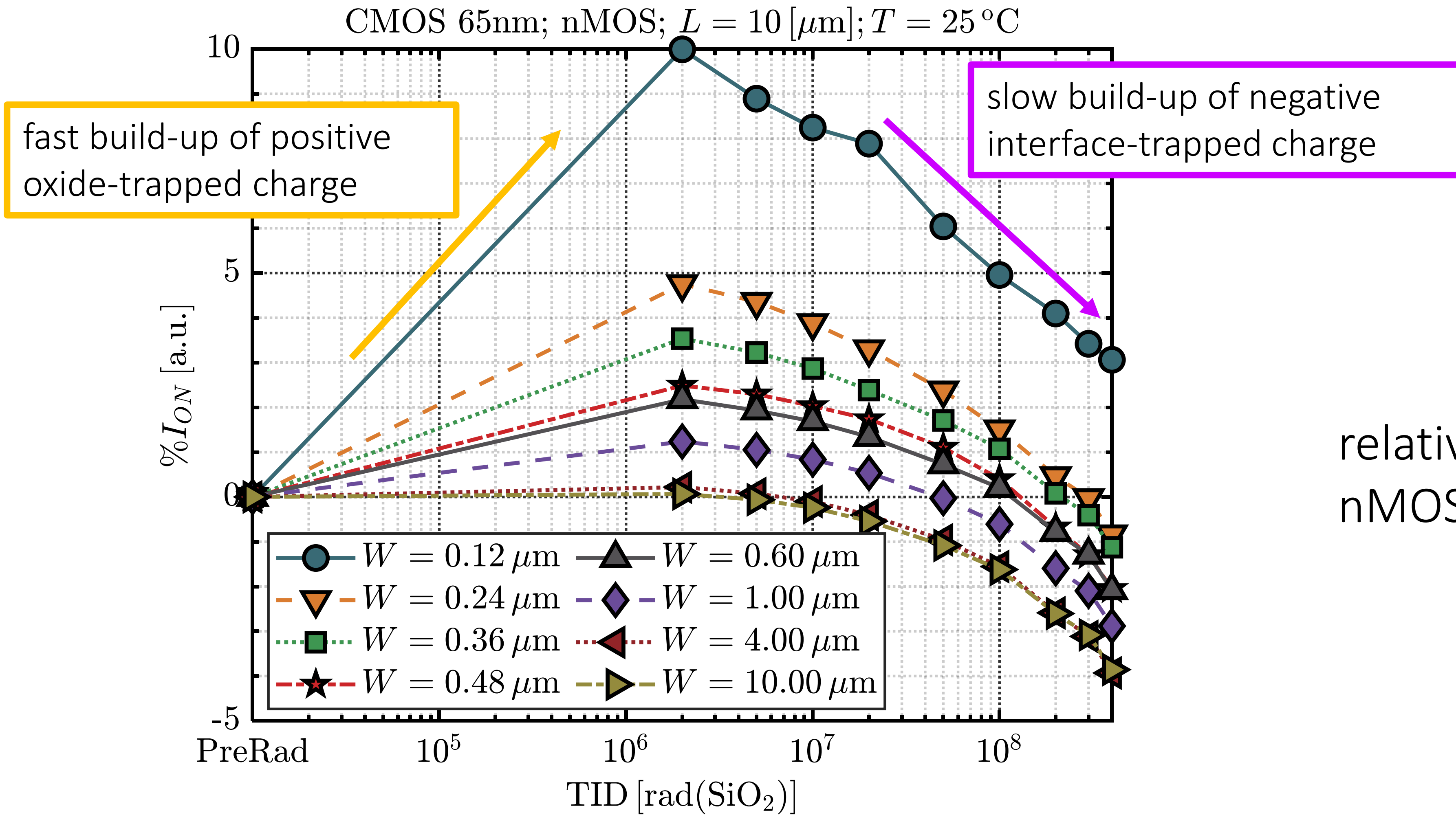
large channel
(*W* ↗↗)

- the amount of trapped charge does not depend on *W*!! (same STI)

- a larger percentage of the narrow channel is affected by the same TID-induced charge!

narrow channel
(*W* ↘↘)



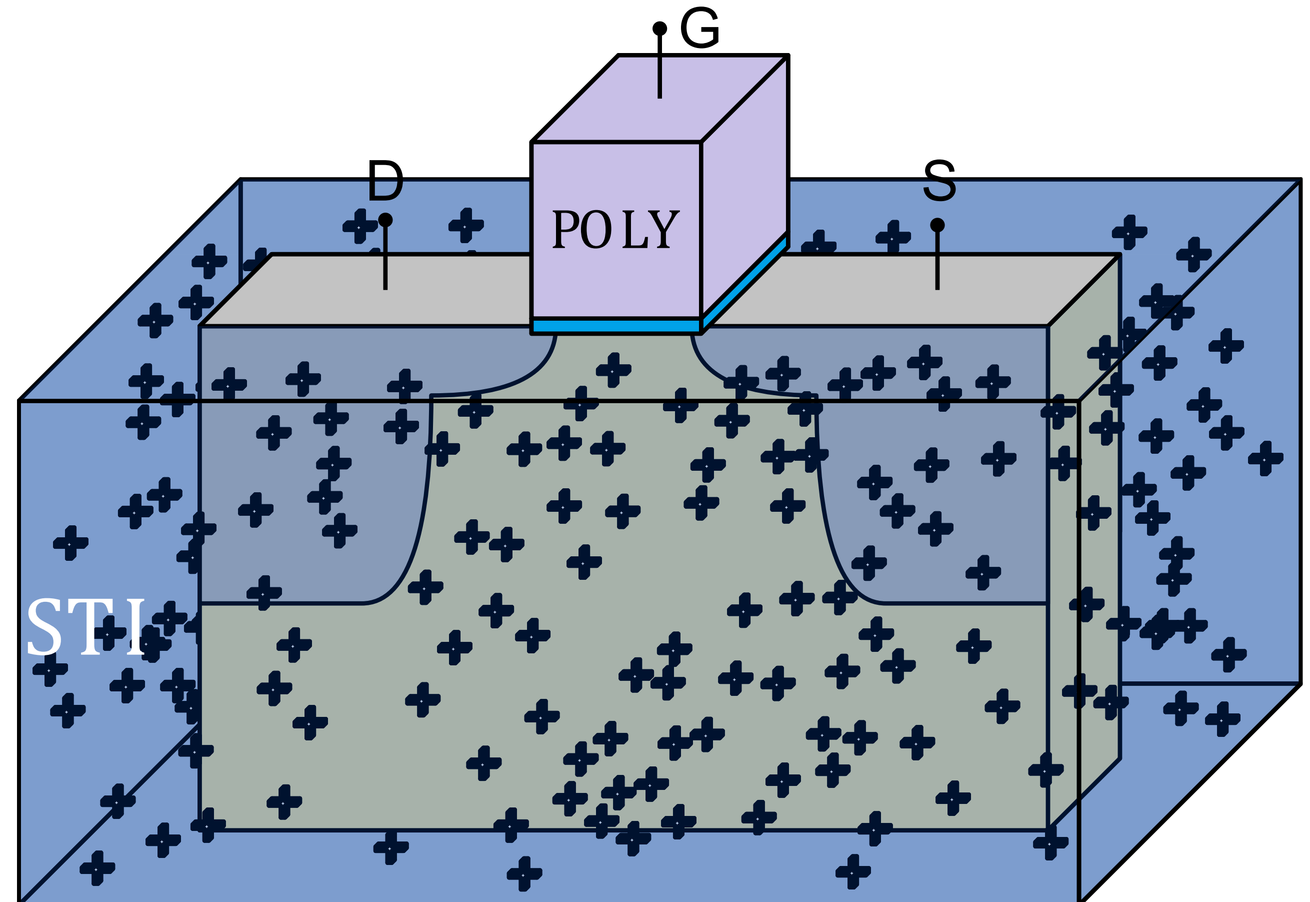


relatively small variation in nMOS caused by RINCE

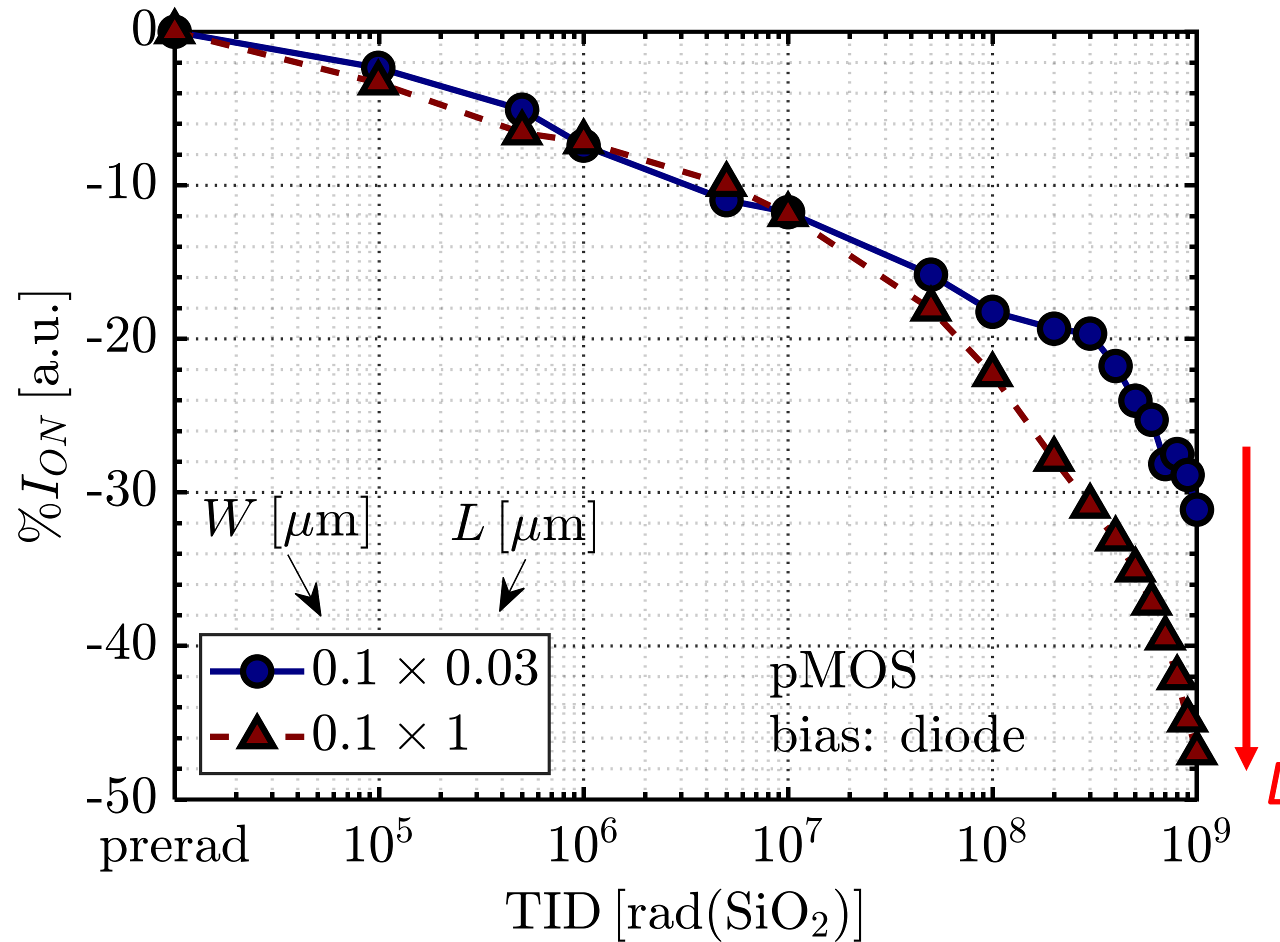
Shallow Trench Isolation (STI) oxide

1. radiation ... drain-to-source le...
2. radiation ... channel effect (RINCE)
3. halo-enhanced robustness in **short** channels

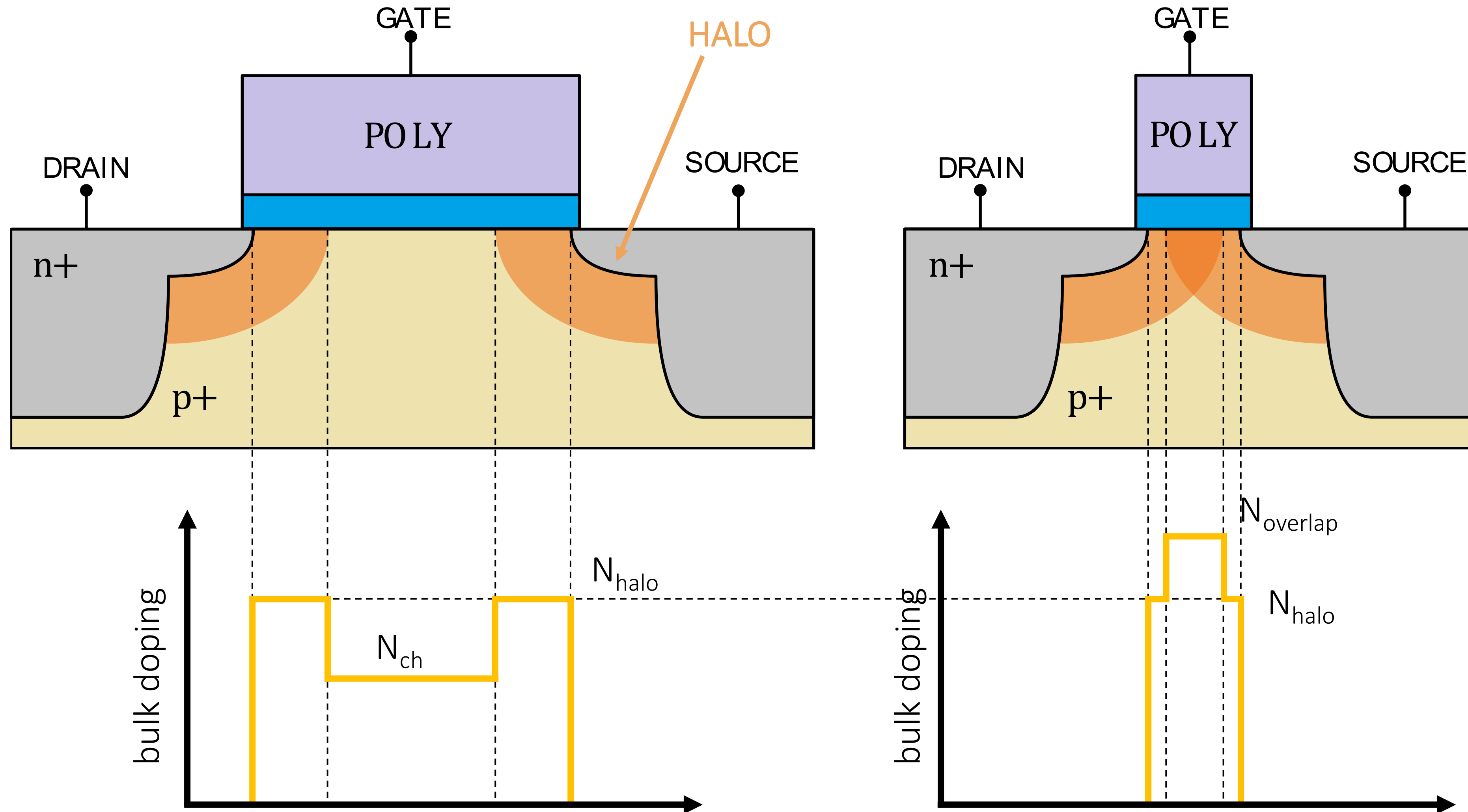
Measured in 28nm (planar) and 16nm (finFET) CMOS technology!



1. Bonaldo, S., et al. "Influence of halo implantations on the total ionizing dose response of 28-nm pMOSFETs irradiated to ultrahigh doses." *IEEE Transactions on Nuclear Science* 66.1 (2018): 82-90.
2. Bonaldo, S., et al. "Ionizing-radiation response and low-frequency noise of 28-nm MOSFETs at ultrahigh doses." *IEEE Transactions on Nuclear Science* 67.7 (2020): 1302-1311.

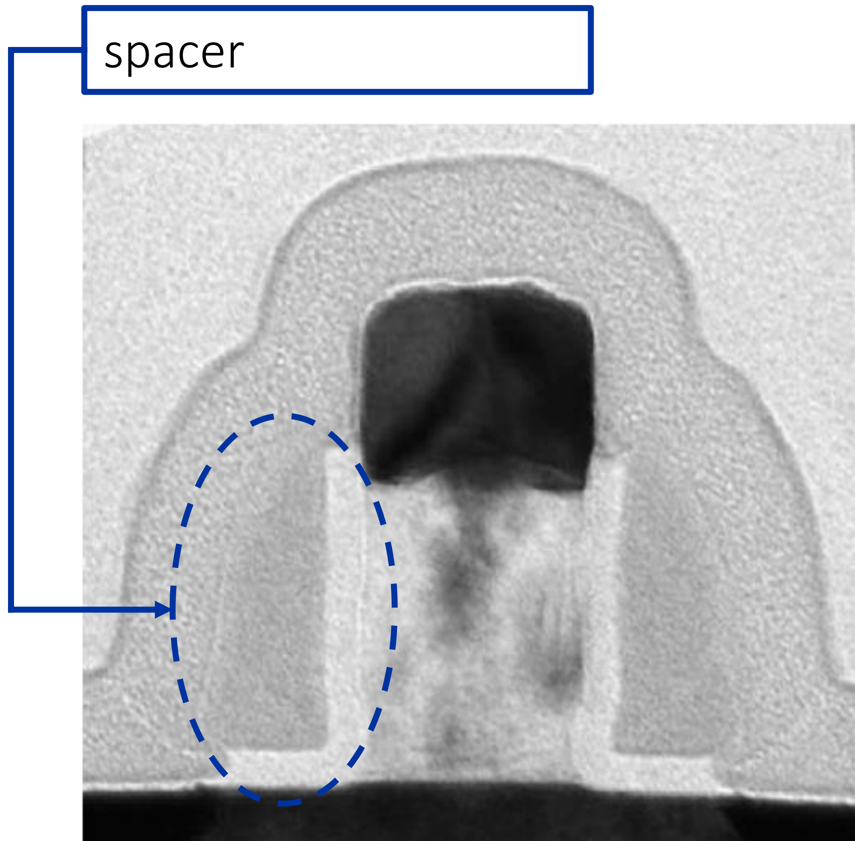


smaller degradation in short channel devices!



1. Bonaldo, S., et al. "Influence of halo implantations on the total ionizing dose response of 28-nm pMOSFETs irradiated to ultrahigh doses." *IEEE Transactions on Nuclear Science* 66.1 (2018): 82-90.
2. Bonaldo, S., et al. "Ionizing-radiation response and low-frequency noise of 28-nm MOSFETs at ultrahigh doses." *IEEE Transactions on Nuclear Science* 67.7 (2020): 1302-1311.

Spacers-related effects



radiation-induced short channel effect (RISCE)

only recently studied!

[1] F. Faccio, S. Michelis, D. Cornale, A. Paccagnella and S. Gerardin, "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2933-2940, Dec. 2015

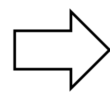
[2] F. Faccio *et al*., "Influence of LDD Spacers and H+ Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses," in *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 164-174, Jan. 2018

[3] S. Bonaldo et al., "Charge Buildup and Spatial Distribution of Interface Traps in 65-nm pMOSFETs Irradiated to Ultrahigh Doses," in IEEE Transactions on Nuclear Science, vol. 66, no. 7, pp. 1574-1583, July 2019

[4] G. Borghello, Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses. Diss. Udine U., 2019

measured in 65nm and 130nm technologies!

larger degradation in short-channel devices



TID

65nm CMOS
pMOS
$W = 20\ \mu m$

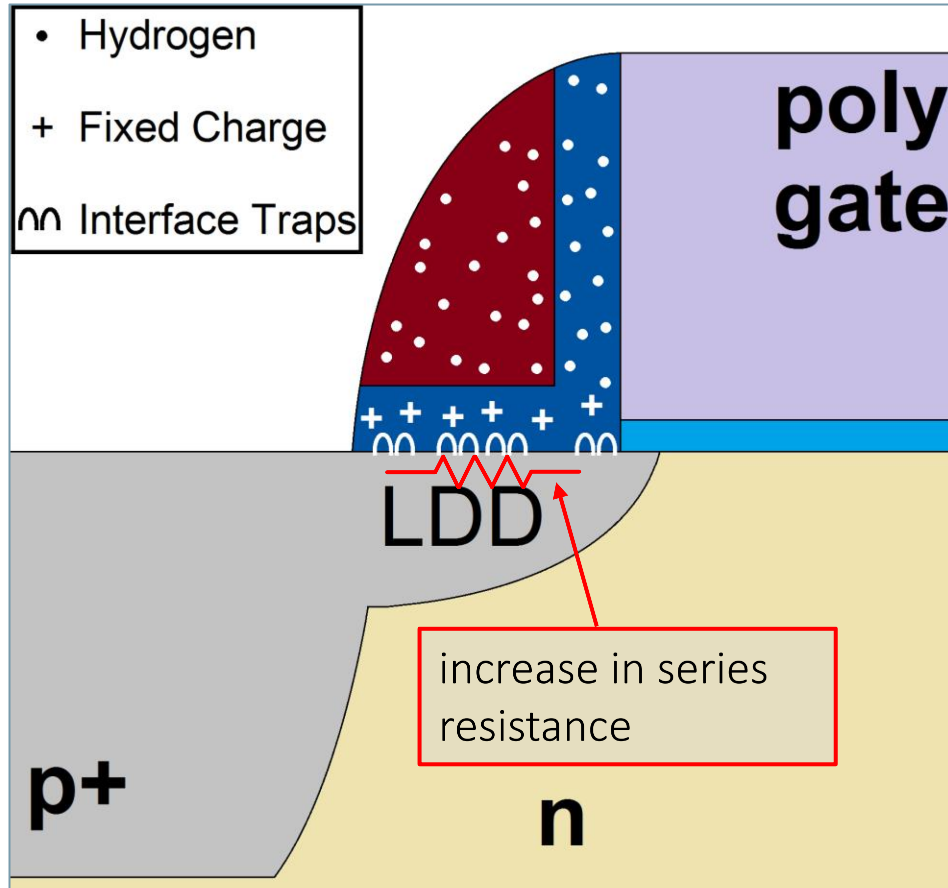
5 Mrad
100 Mrad
200 Mrad
500 Mrad

$\%I_{ON}$

0
-10
-20
-30
-40
-50

10^{-1} 10^{0} 10^{1}

$L\ [\mu m]$

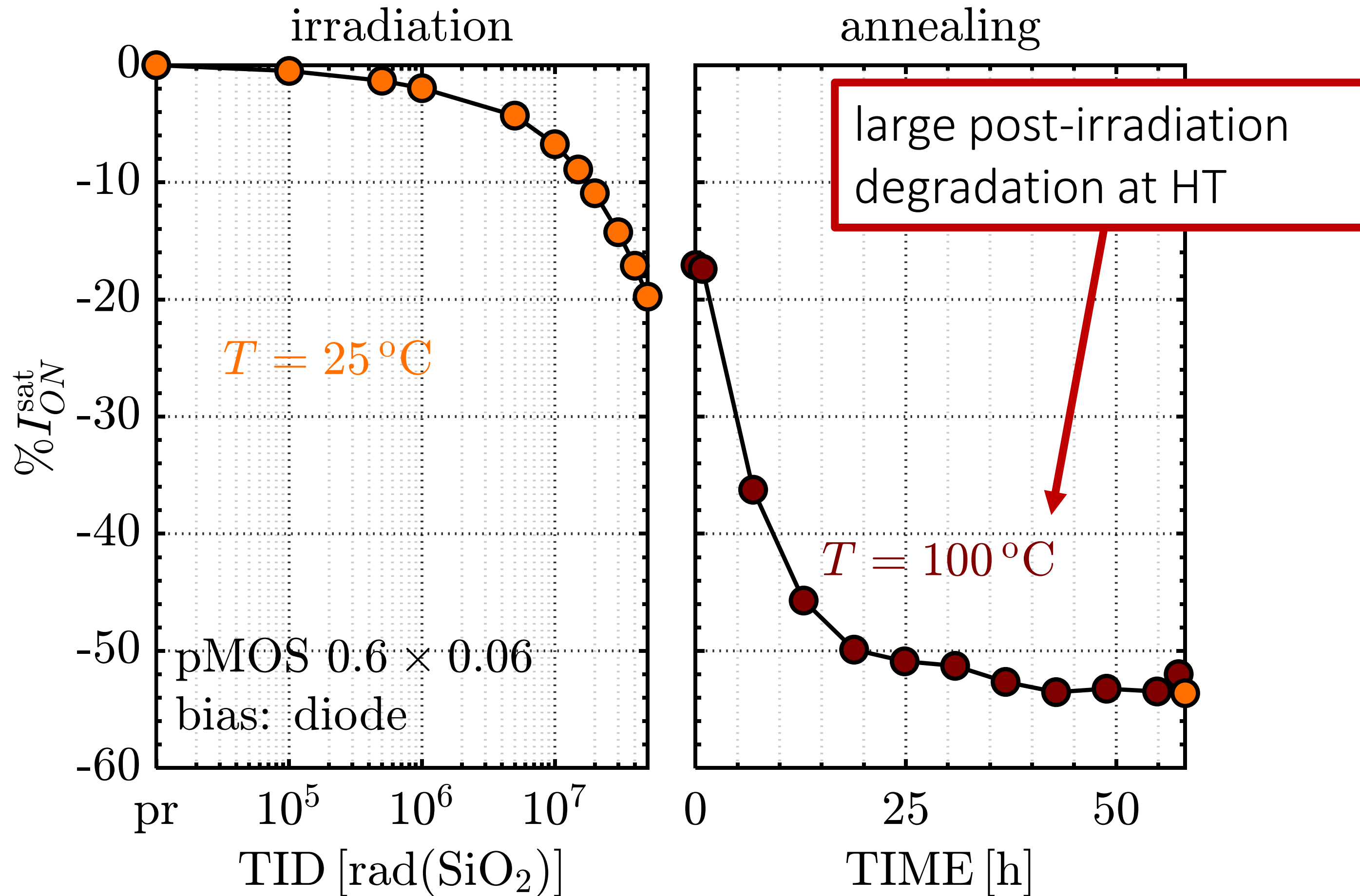


Same R_{SD} + higher current (small L)
→ Larger voltage drop

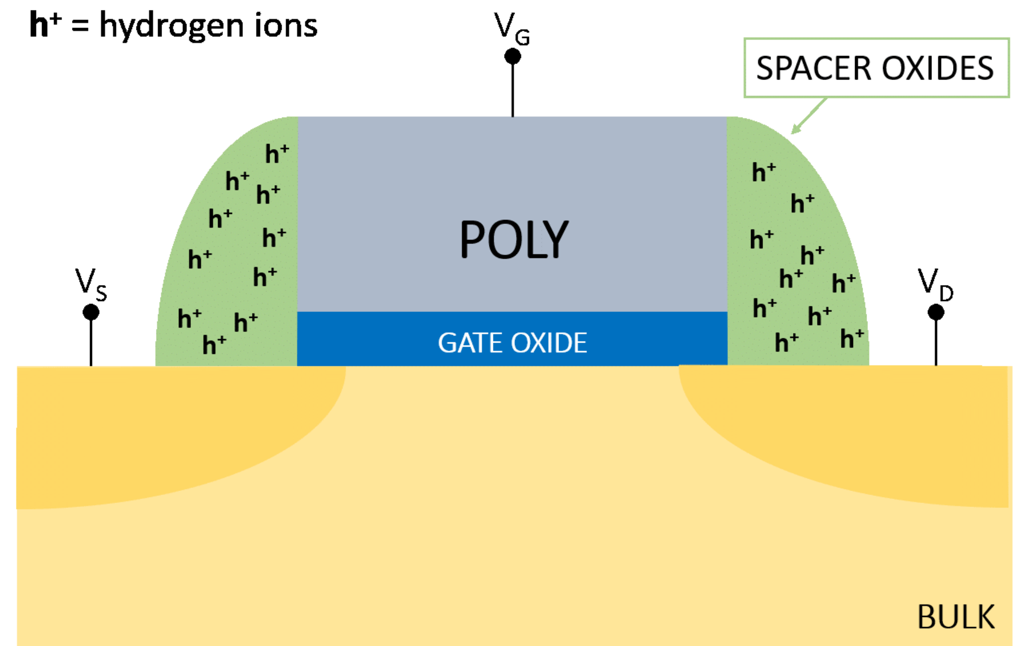
$$V_D^{\text{channel}} = V_D^{\text{terminal}} - I_D R_{SD}$$

$$\Rightarrow V_D^{\text{terminal}} - V_D^{\text{channel}} \triangleq \Delta V_D = I_D R_{SD} = R_{SD} \frac{W}{L} I_{JD}$$

F. Faccio, G. Borghello, E. Lerario, D. M. Fleetwood, R. D. Schrimpf, H. Gong, E. X. Zhang, P. Wang, S. Michelis, S. Gerardin, A. Paccagnella, and S. Bonaldo. "Influence of LDD spacers and H+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultra-high doses". In: *IEEE Transactions on Nuclear Science* 65.1 (Jan. 2018), pp. 164–174.

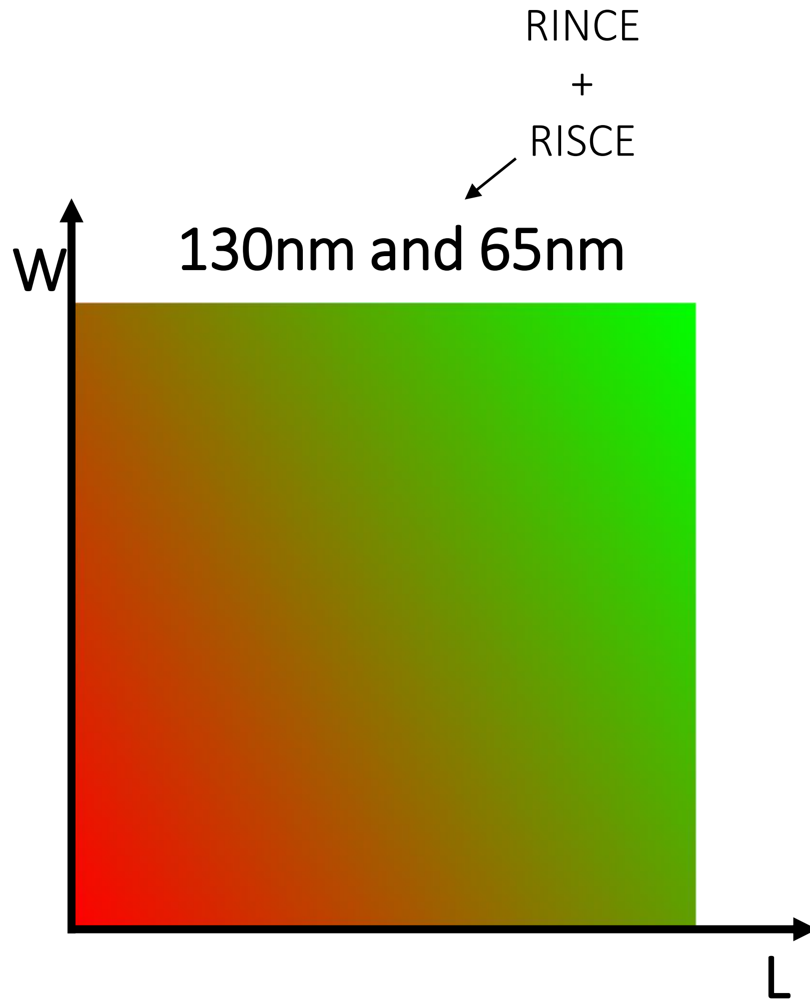


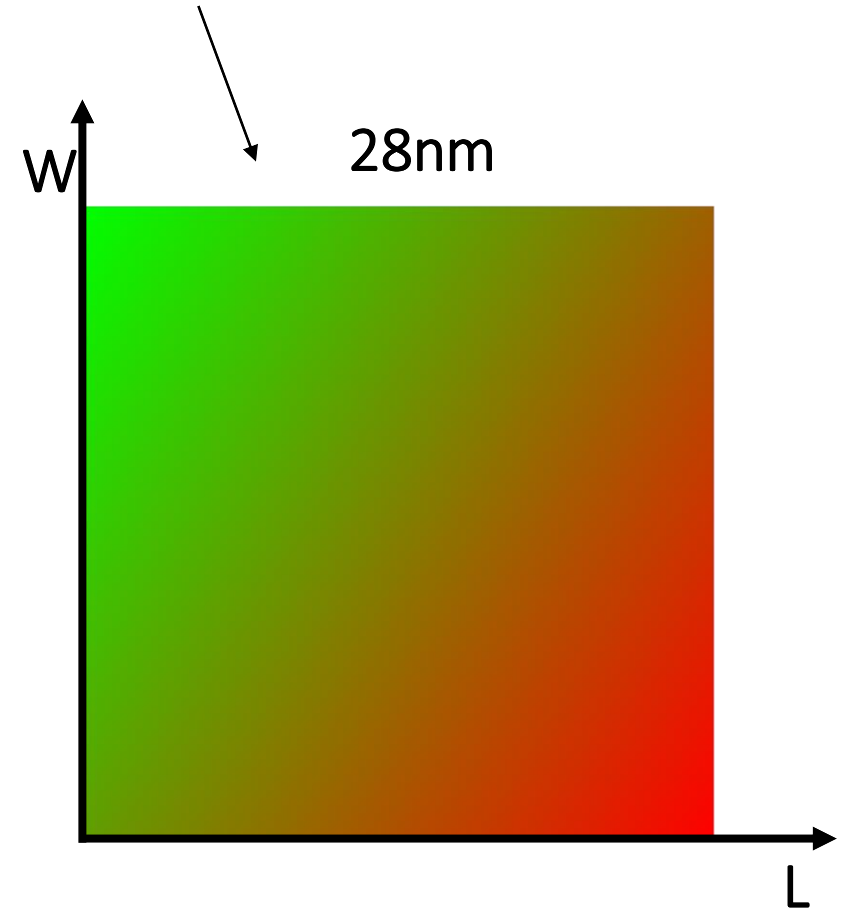
spacers-to-gate oxide transport of H^+



F. Faccio et al., "Influence of LDD Spacers and H+ Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses," in IEEE TNS, vol. 65, no. 1, pp. 164-174, Jan. 2018,

130nm VS 65nm VS 28nm

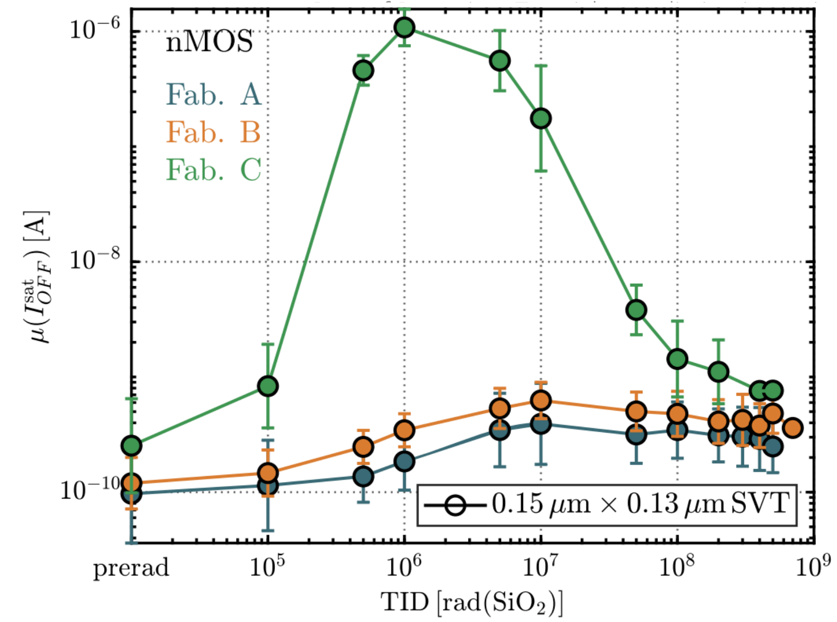


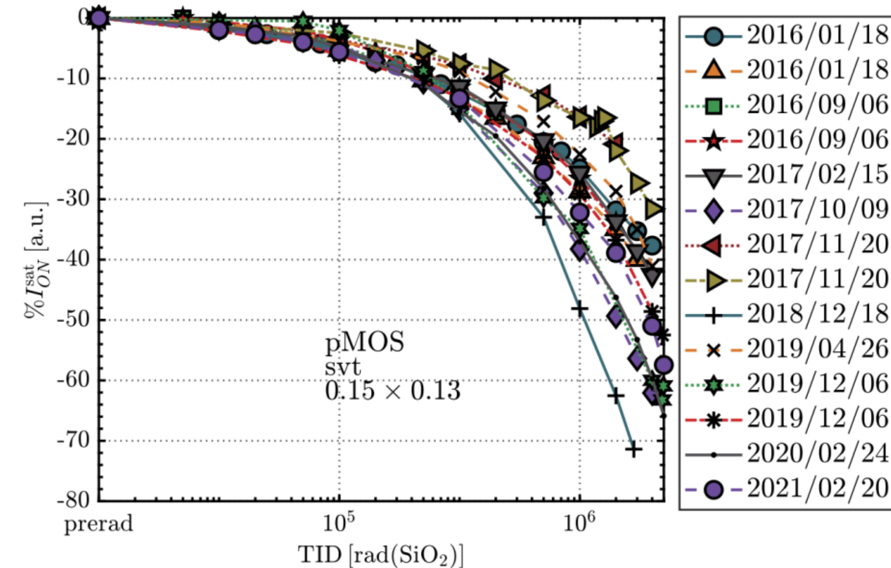


radiation-induced variability

TID effects are affected by:

- technology-to-technology variability
- manufacturer-to-manufacturer variability
- fab-to-fab variability
- chip-to-chip variability
- lot-to-lot variability
- transistor-to-transistor variability



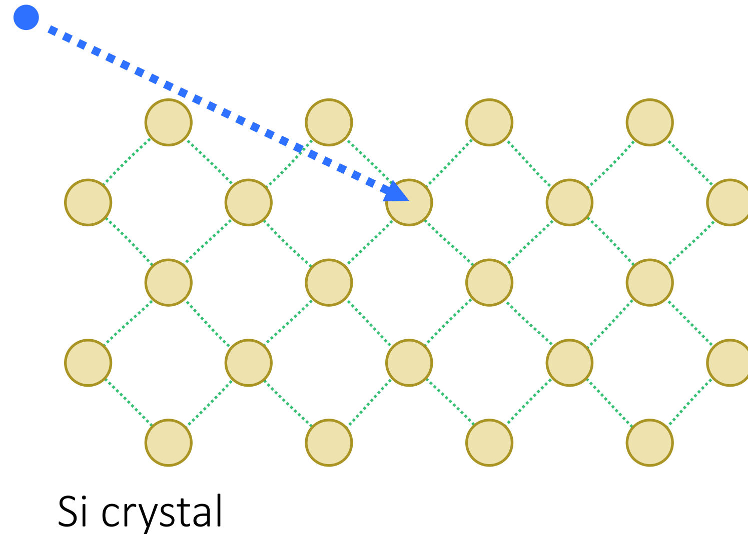


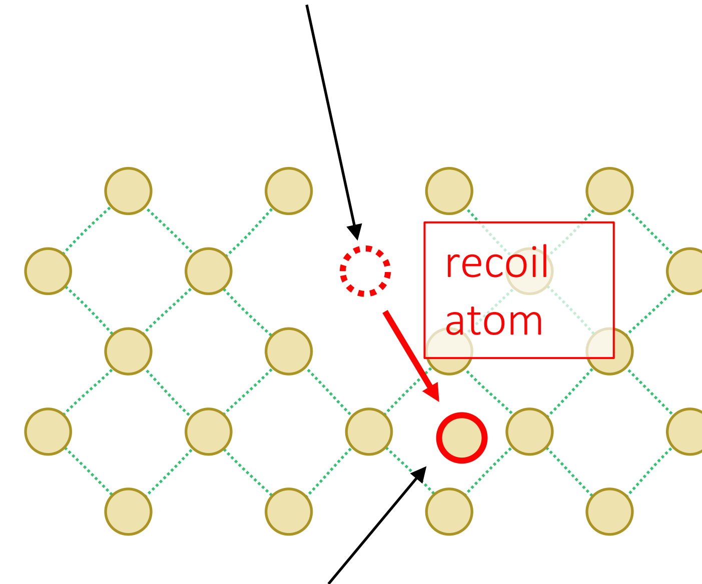
Termo, G., Borghello, G., Faccio, F., Michelis, S., Koukab, A., & Sallese, J. M. (2023). "Fab-to-fab and run-to-run variability in 130 nm and 65 nm CMOS technologies exposed to ultra-high TID". *Journal of Instrumentation*, 18(01), C01061.

OUTLINE

- introduction
- cumulative effects
  - ionizing effects (total ionizing dose [TID])
    - basic mechanisms
    - TID effects in microelectronics
  - non-ionizing effects (displacement damage [DD])
- stochastic effects
  - ionizing effects (single event effects [SEE])

physical mechanisms of DD-induced degradation

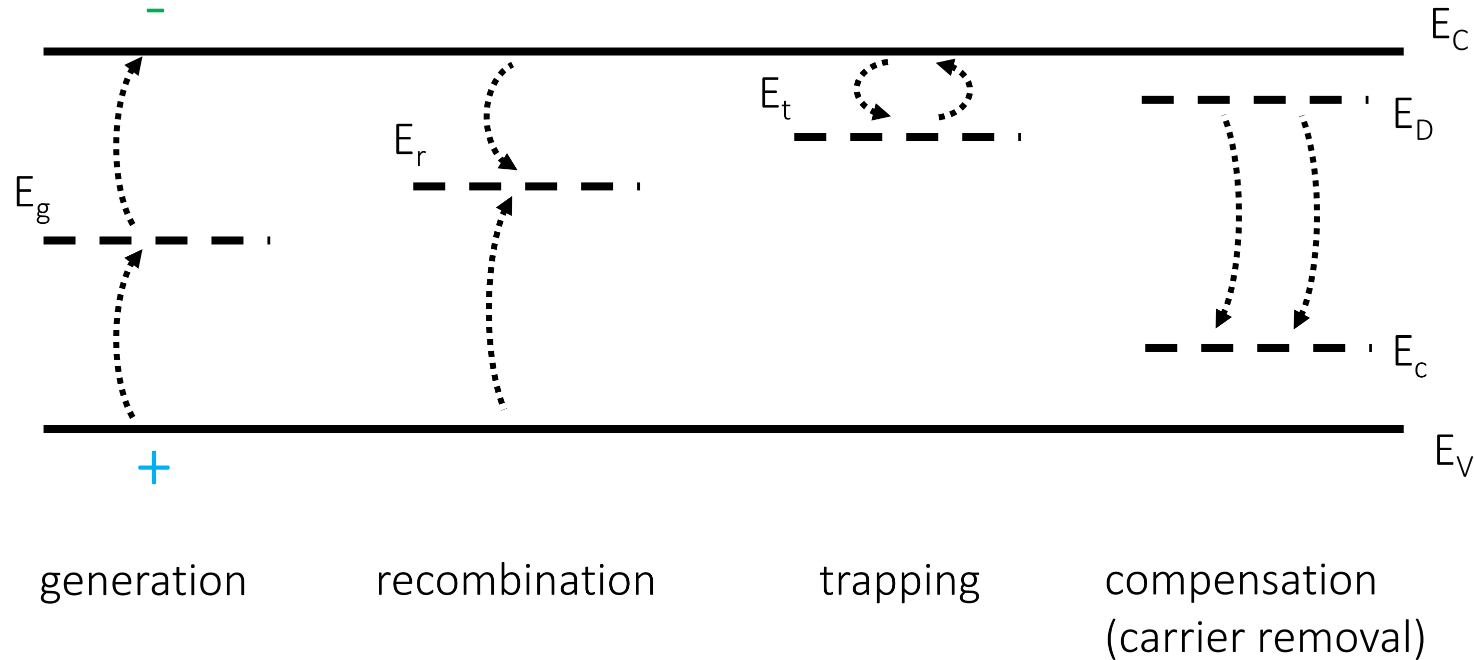




The disturbance in the crystal lattice periodicity has associated discrete energy levels in the forbidden energy band-gap. These influence generation-recombination processes in the material.

[1] J. R. Srour, C. J. Marshall and P. W. Marshall, "Review of displacement damage effects in silicon devices," in *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653-670, June 2003, doi: 10.1109/TNS.2003.813197.
[2] Oldham, Timothy R. "Basic mechanisms of TID and DDD response in MOS and bipolar microelectronics." *NSREC Short Course* (2011).
[3] J. R. Srour and J. W. Palko, "Displacement Damage Effects in Irradiated Semiconductor Devices," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1740-1766, June 2013, doi: 10.1109/TNS.2013.2261316.

physical mechanisms of DD-induced degradation



[1] J. R. Srour, C. J. Marshall and P. W. Marshall, "Review of displacement damage effects in silicon devices," in *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653-670, June 2003, doi: 10.1109/TNS.2003.813197.
[2] Oldham, Timothy R. "Basic mechanisms of TID and DDD response in MOS and bipolar microelectronics." *NSREC Short Course* (2011).
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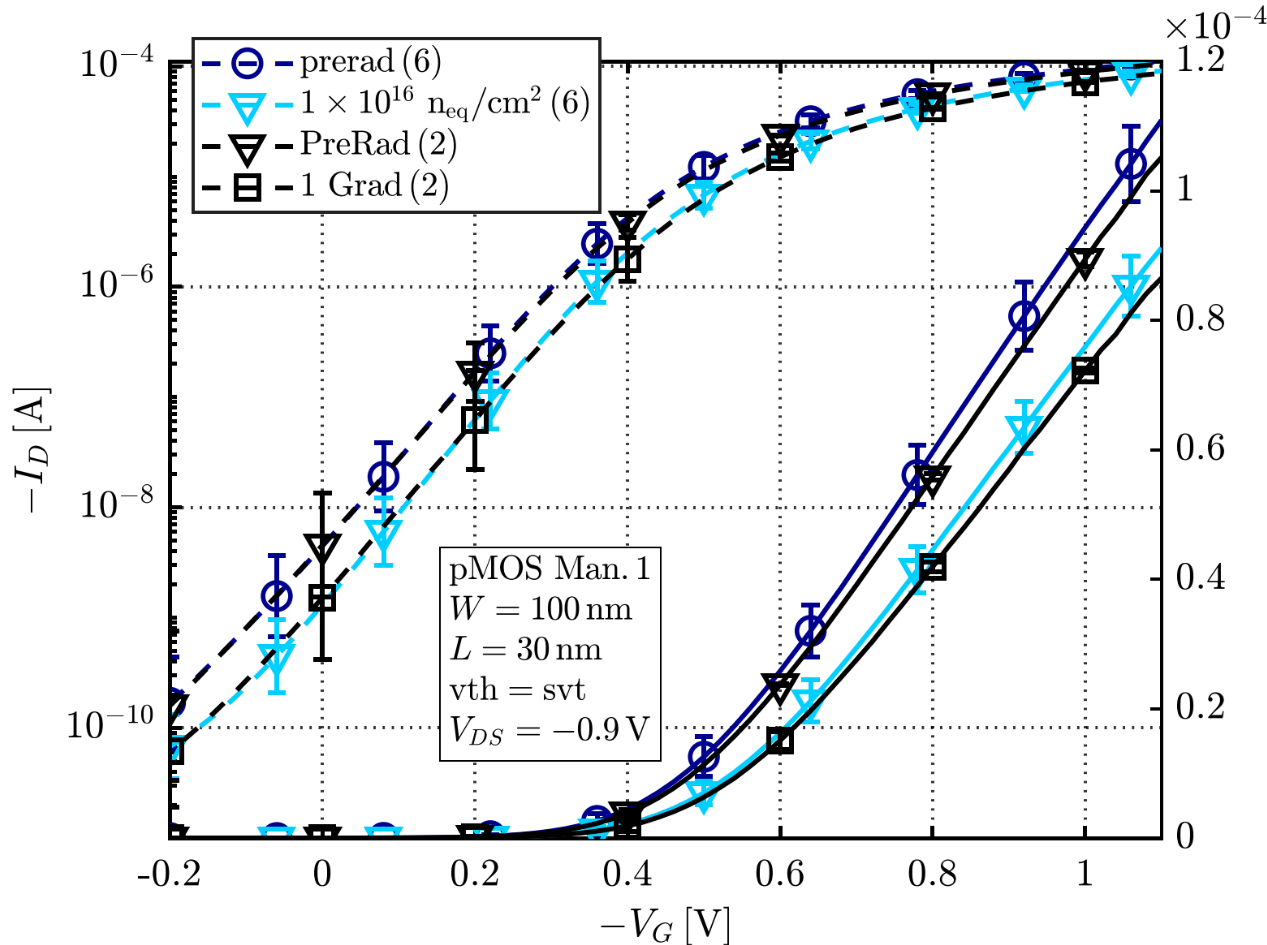
MOS transistors & displacement damage



G. Termo, et al., *"Neutron- and Proton-Induced Degradation Of MOS Transistors In 28nm CMOS Technology."* RADECS 2023

CMOS 28nm technology
colored lines -> proton irradiation
black lines -> Xray irradiation

The effect of proton irradiation is explainable by the deposited TID!

MOS transistors are generally not very sensitive to DD!

paper on 65nm CMOS technology:

Ding, Lili, et al. "Investigation of total ionizing dose effect and displacement damage in 65 nm CMOS transistors exposed to 3 MeV protons." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 796 (2015): 104-107.

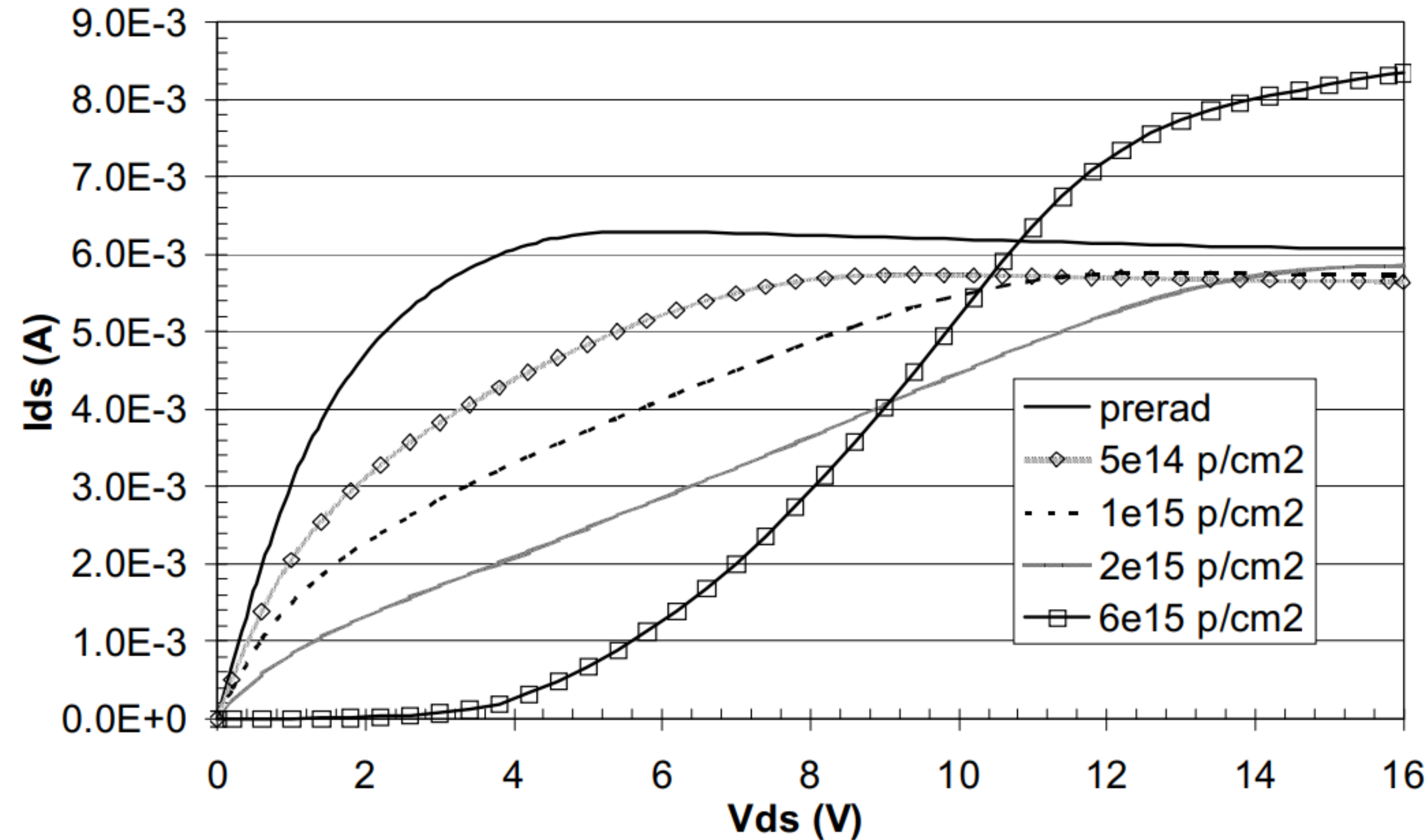


Fig. 12. Evolution of the output characteristics with proton irradiation of n-channel LDMOS transistors in technology D (0.18 µm).

might be relevant for some high-voltage CMOS devices!

Faccio, Federico, et al. "TID and displacement damage effects in vertical and lateral power MOSFETs for integrated DC-DC converters." *2009 European Conference on Radiation and Its Effects on Components and Systems*. IEEE, 2009.

DD in other devices

particle detectors:

[1] Gill, K., G. Hall, and B. MacEvoy. "Bulk damage effects in irradiated silicon detectors due to clustered divacancies." *Journal of applied physics* 82.1 (1997): 126-136.

[2] Leroy, Claude, and Pier-Giorgio Rancoita. "Particle interaction and displacement damage in silicon devices operated in radiation environments." *Reports on Progress in Physics* 70.4 (2007): 493.

[3] Moll, Michael. "Displacement damage in silicon detectors for high energy physics." *IEEE Transactions on Nuclear Science* 65.8 (2018): 1561-1582.

optoelectronics:

[1] Johnston, A. H. "Radiation damage of electronic and optoelectronic devices in space." (2000).

[2] Johnston, Allan H. "Radiation effects in optoelectronic devices." *IEEE Transactions on Nuclear Science* 60.3 (2013): 2054-2073.

GaN HEMT:

[1] Fleetwood, Daniel M., et al. "Radiation effects in AlGaN/GaN HEMTs." *IEEE Transactions on Nuclear Science* 69.5 (2022): 1105-1119.

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- stochastic effects
  - ionizing effects (single event effects [SEE])

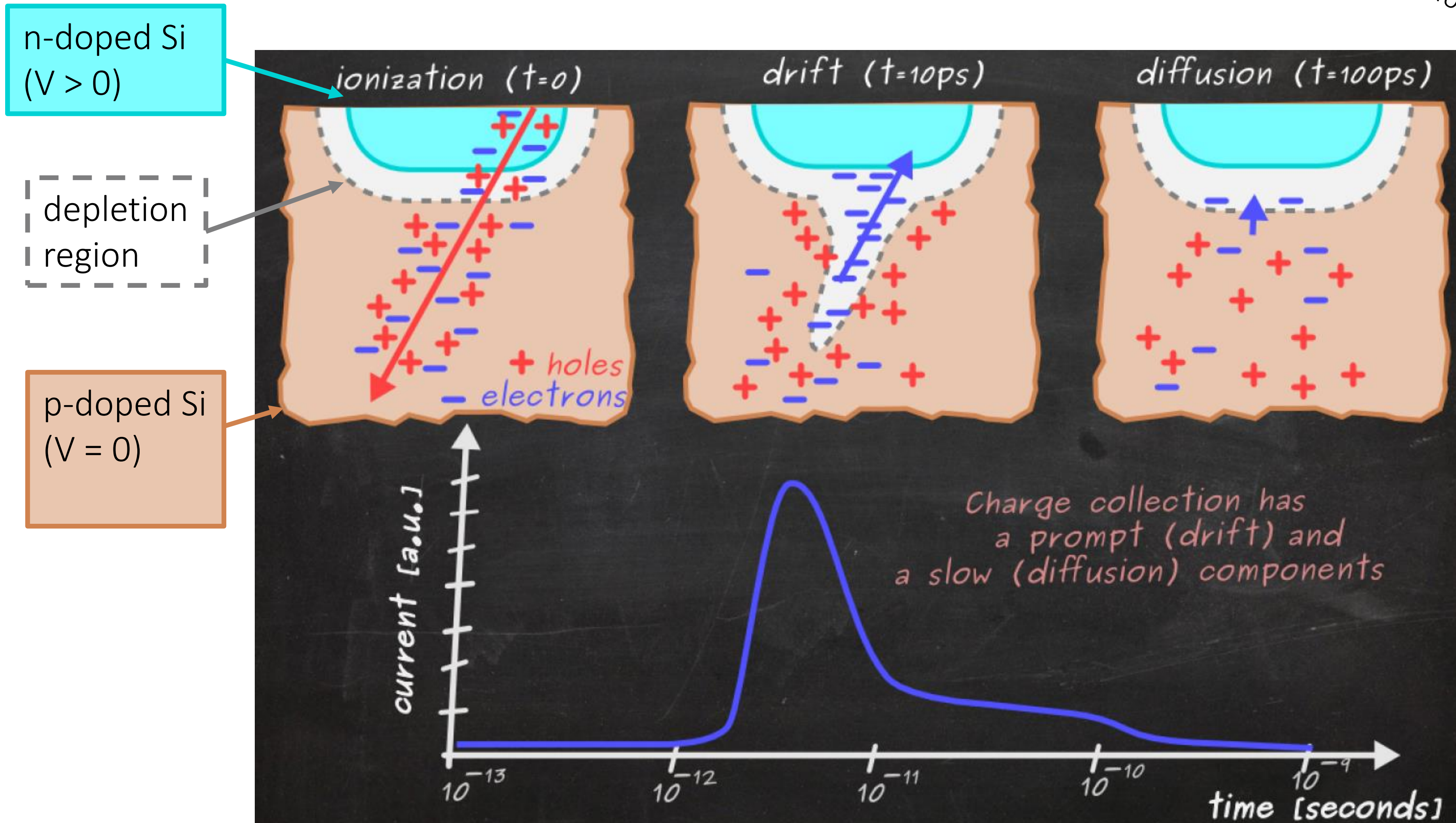
stochastic effects

(a particle may or may not produce an error [probability])
(probability of interaction does not depend on past events [random])

Single Event Effects (SEEs) are any measurable disturbance on a circuit resulting from a **single**, energetic particle strike

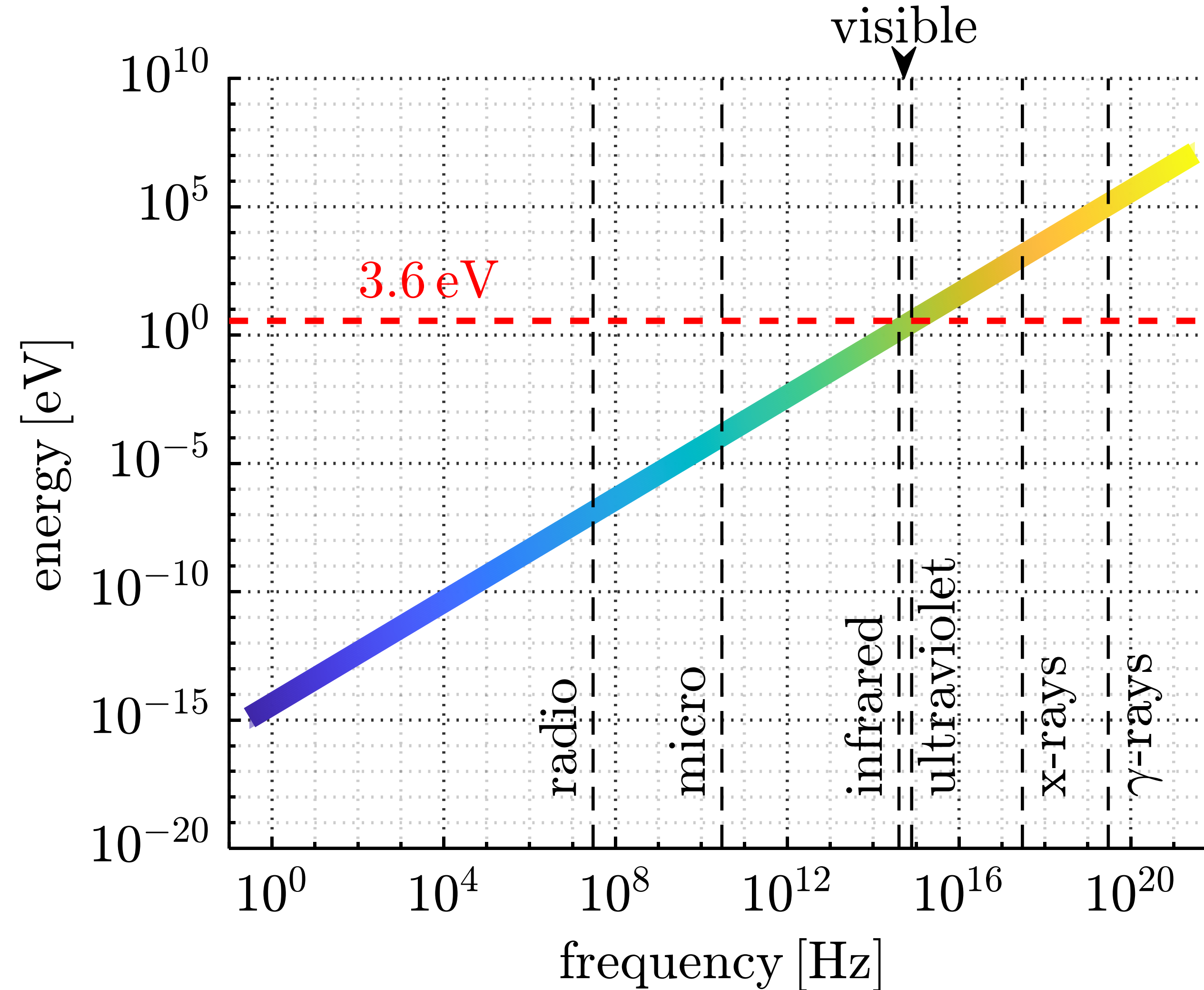
giulio.borghello@cern.ch | CERN EP-ESE-ME

thanks Szymon Kulis for the slide!



https://tmrg.web.cern.ch/tmrg/tmrg_kulis_in2p3.pdf

e-h pair creation energy in Si ~3.6eV



stochastic effects

(a particle may or may not produce an error [probability])
(probability of interaction does not depend on past events [random])

non-destructive

- Single Event Upset
- Single Event Transient
- etc…

destructive

- Single Event Latch-Up
- etc…

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- etc…

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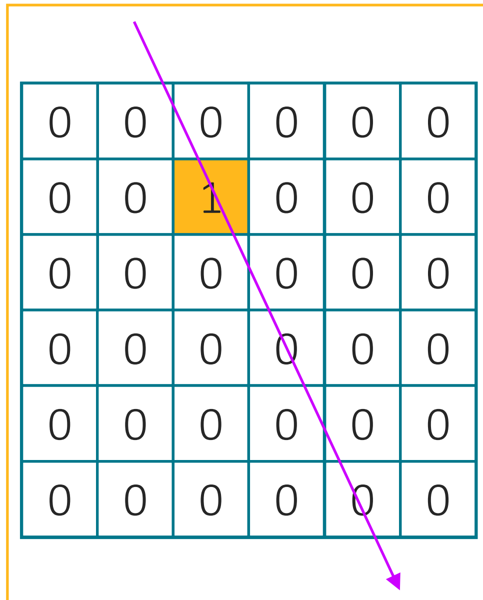
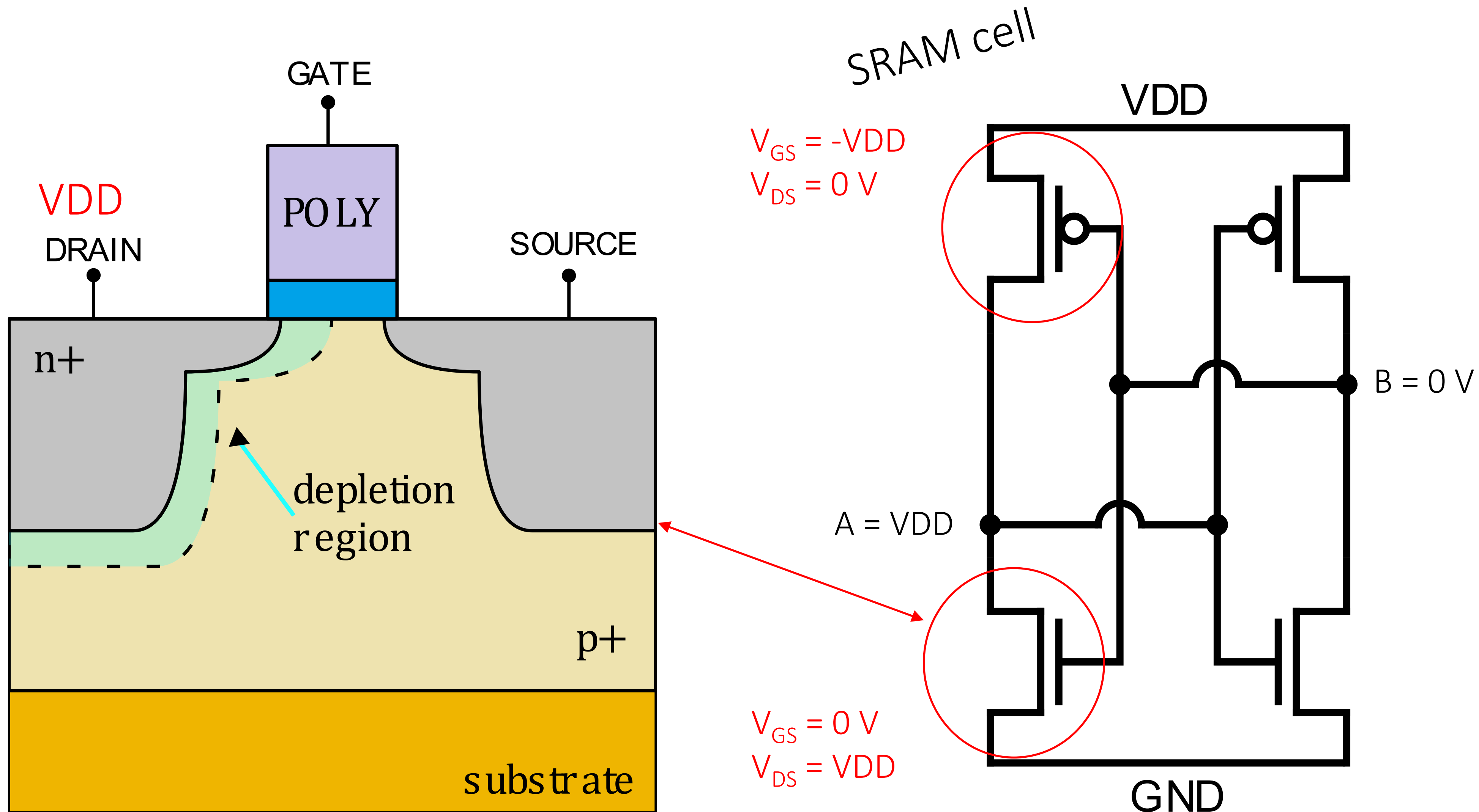
BIT-UPSET = change in the value of a bit caused by a particle

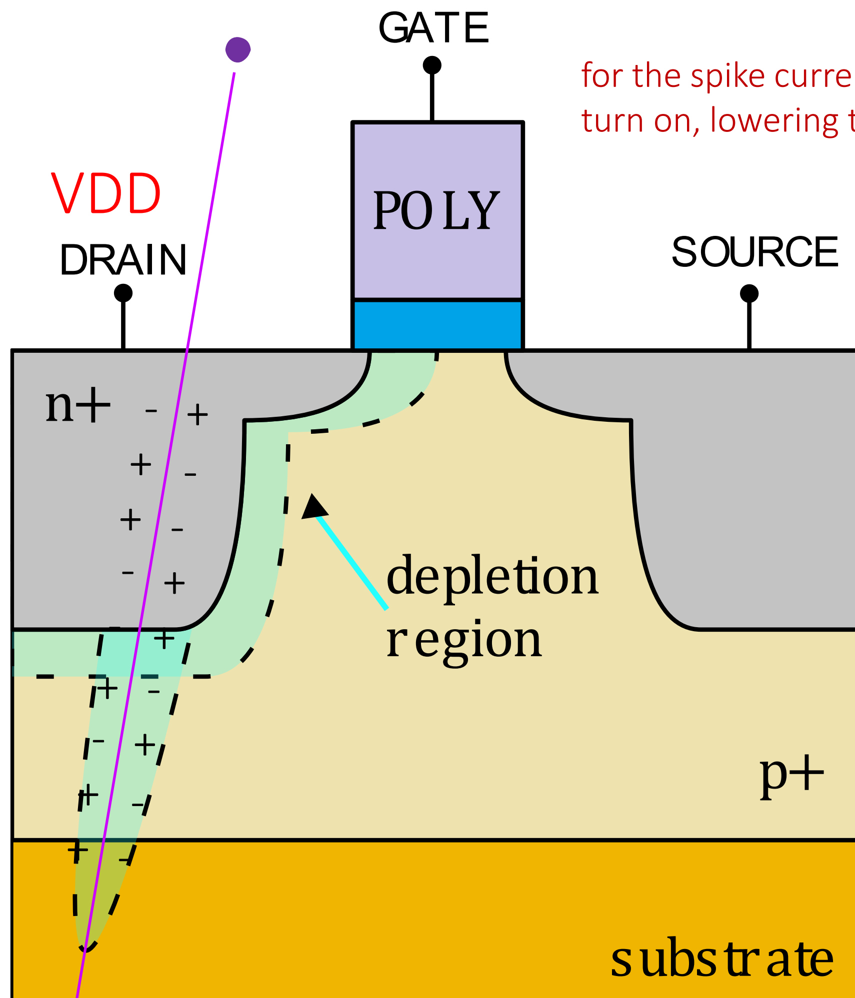
Single-bit-upset (SBU)



EXAMPLE: SRAM



EXAMPLE: SRAM



SRAM cell

for the spike current to flow, the pMOS must turn on, lowering the voltage in node A

If the input voltage of this inverter is low enough -> B = VDD

VDD

B = VDD

A = GND

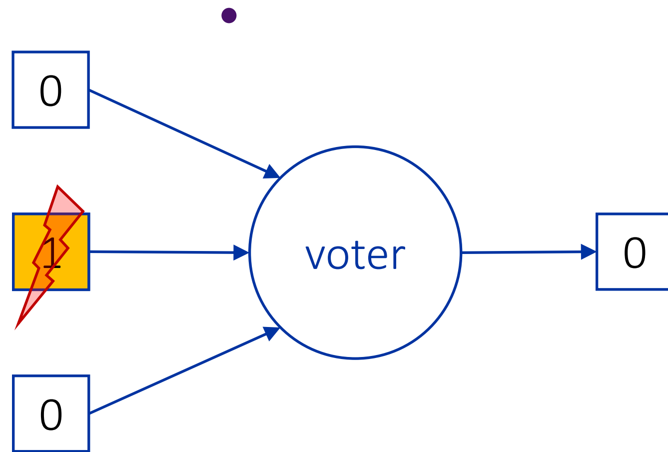
GND

B=VDD enforces A = GND
-> the error is latched into the memory cell!

How to deal with SEU?

TRIPLICATION

(widely used to prevent SEU)



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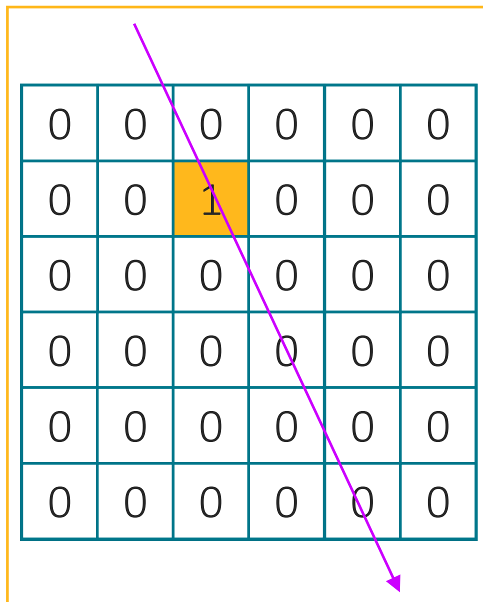
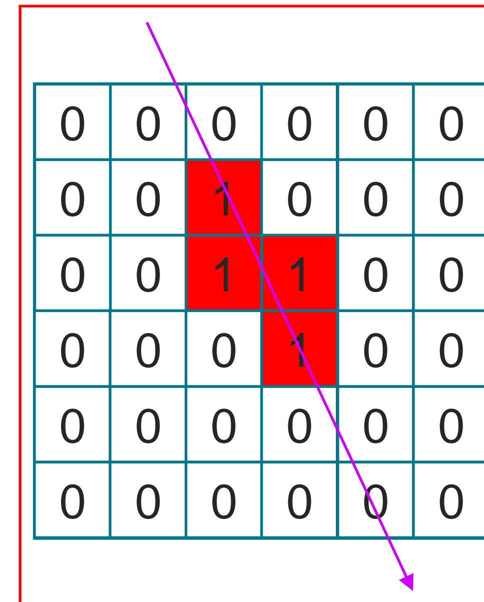
Single-bit-upset (SBU)

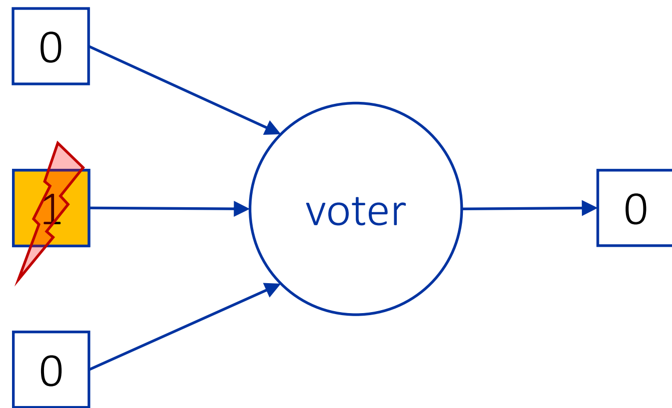


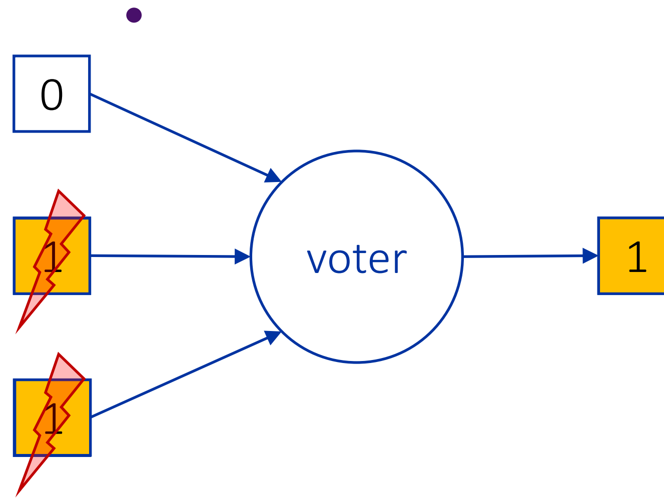
Multi-bit-upset (MBU)

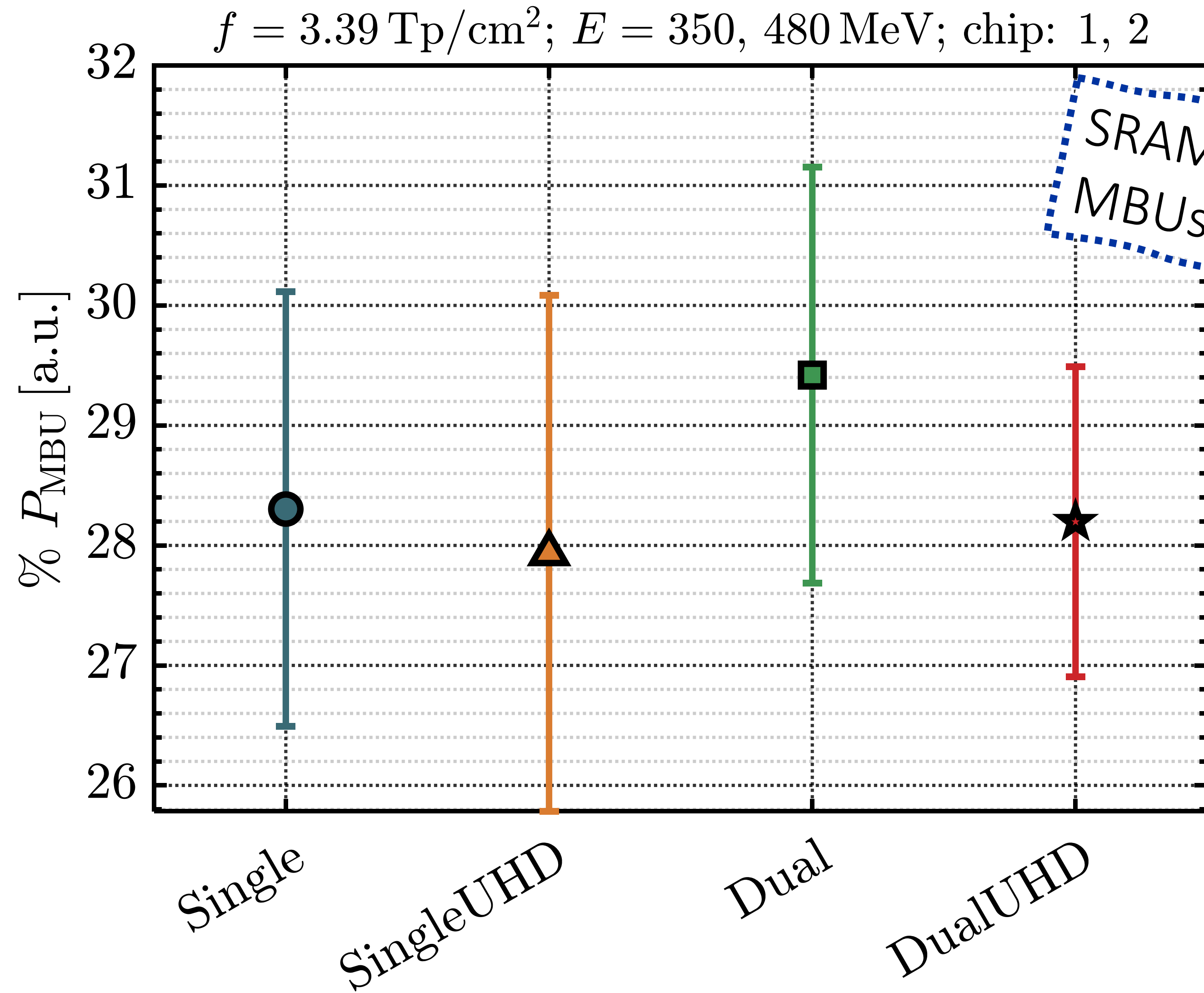


TRIPLICATION

(widely used to prevent SEU)





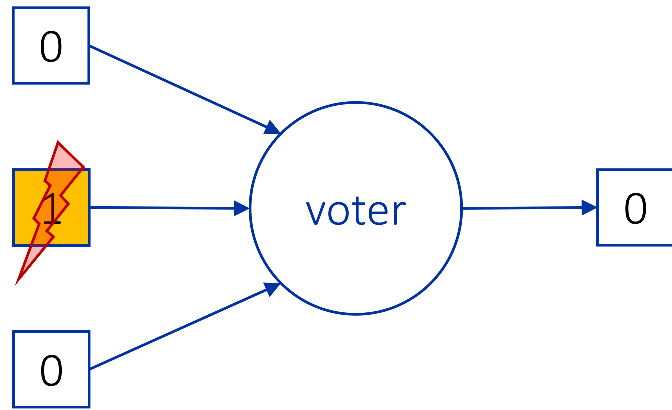


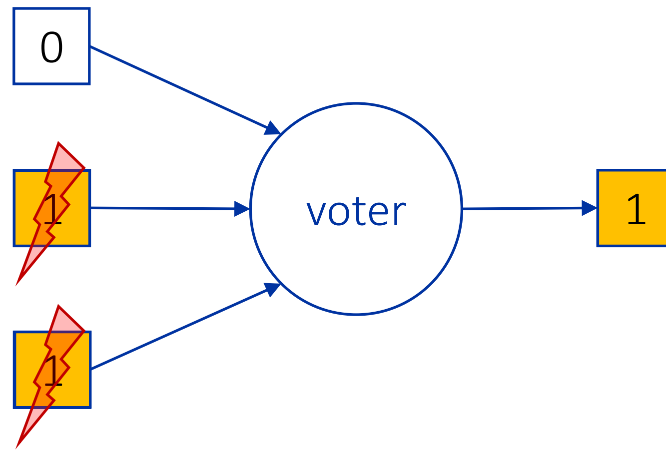
SRAM 28nm irradiated with protons:
MBUs correspond to ~30% of the total errors

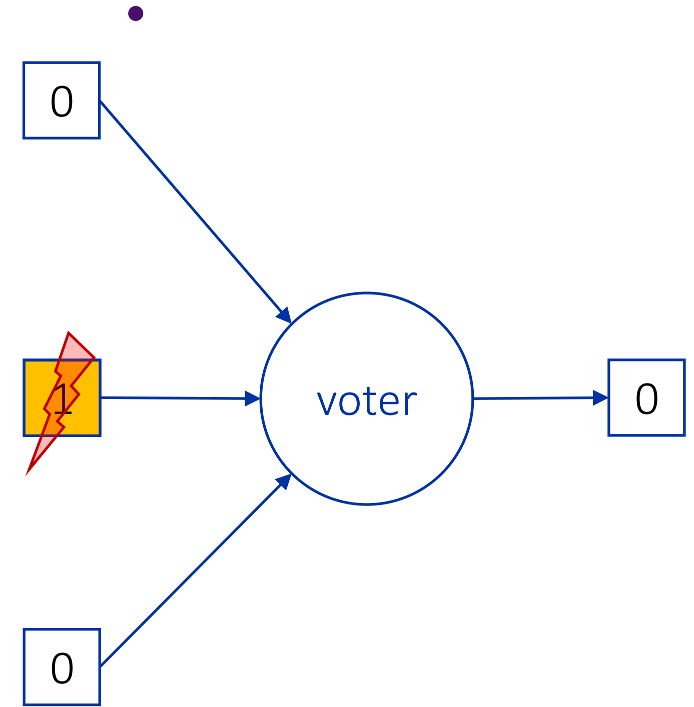
G. Borghello, et al., Single Event Effects characterization of a commercial 28 nm CMOS technology, TWEPP 2023

TRIPLICATION

(widely used to prevent SEU)

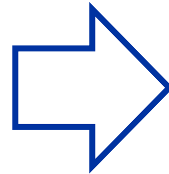


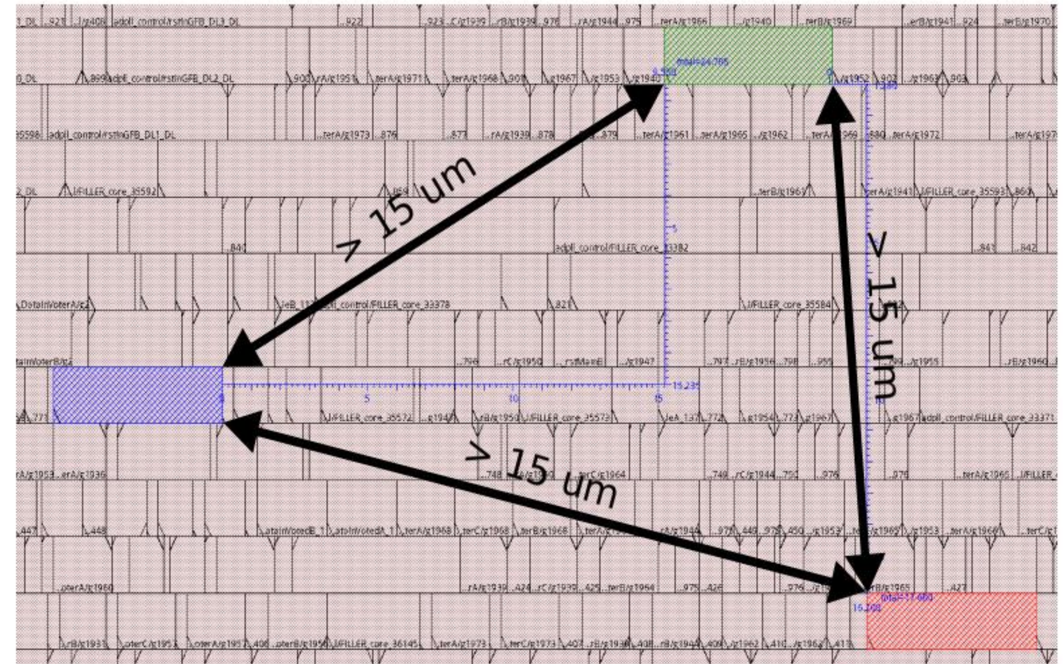




physical distance among triplicated cells reduces the risk of MBU!

15 μm typically used in 65nm technology





Stefan Biereigel: Investigations on Multi-Bit Upsets in 65nm CMOS (https://indico.cern.ch/event/959655)

most likely 15 μm is an overestimation (see https://indico.cern.ch/event/959655).

Recent measurements in 28nm showed that ~6um are enough to prevent MBU
(G. Borghello, et al., *Single Event Effects characterization of a commercial 28 nm CMOS technology*, TWEPP 2023).

stochastic effects

(a particle may or may not produce an error [probability])
(probability of interaction does not depend on past events [random])

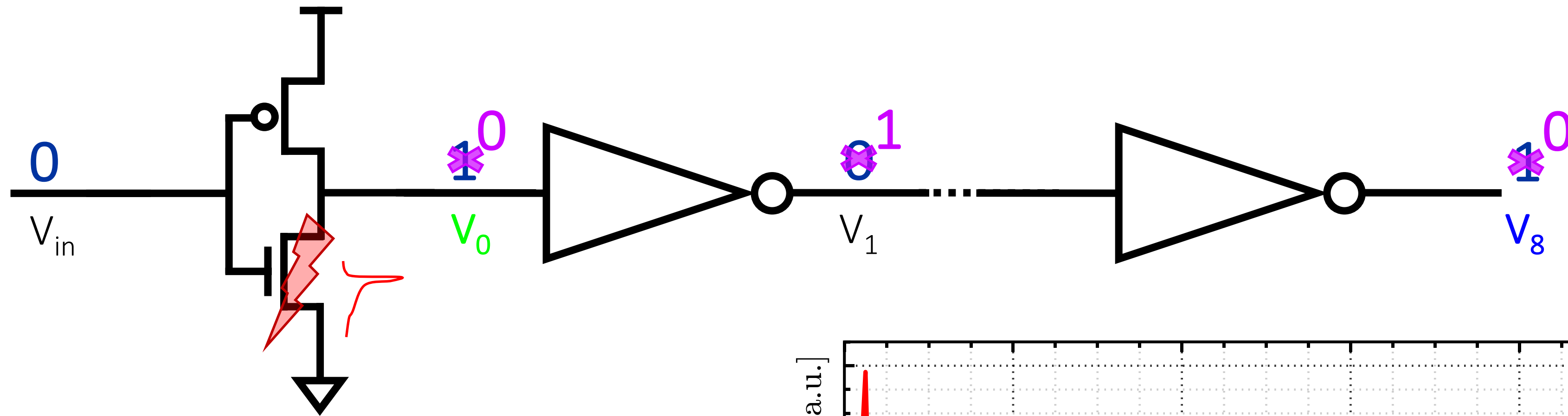
non-destructive

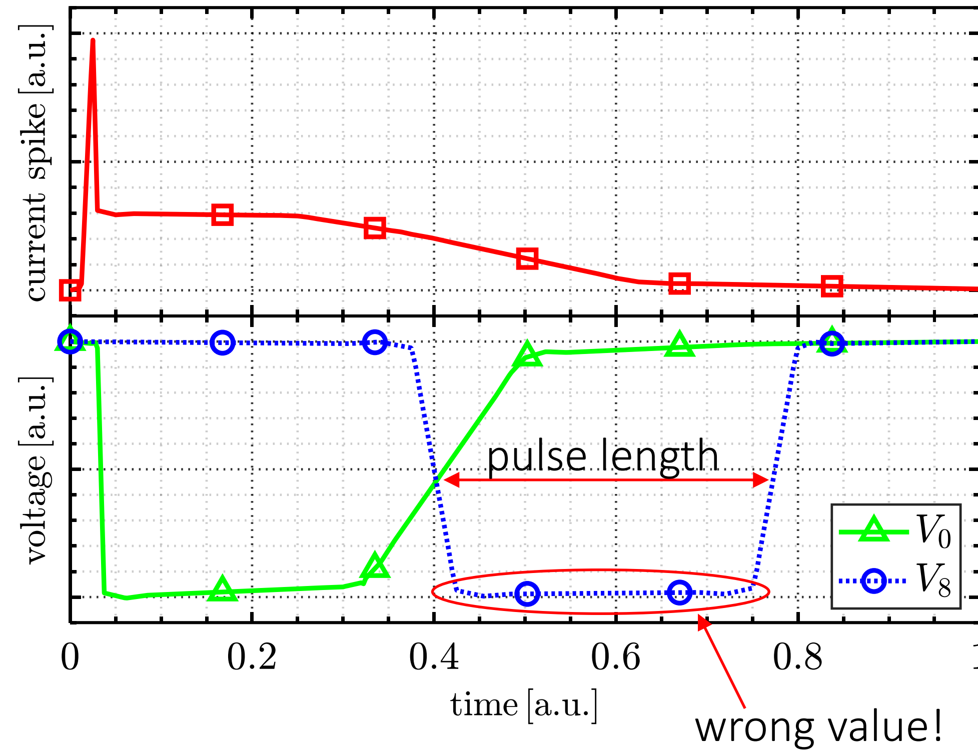
- Single Event Upset
- Single Event Transient
- etc…

destructive

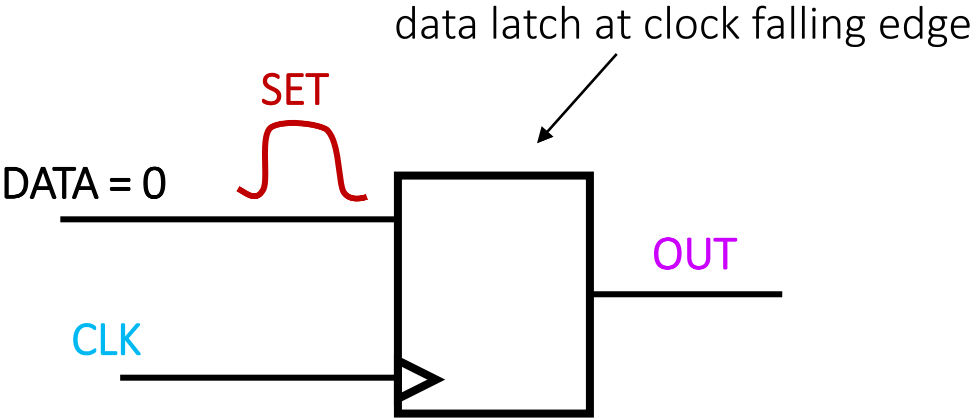
- Single Event Latch-Up
- etc…

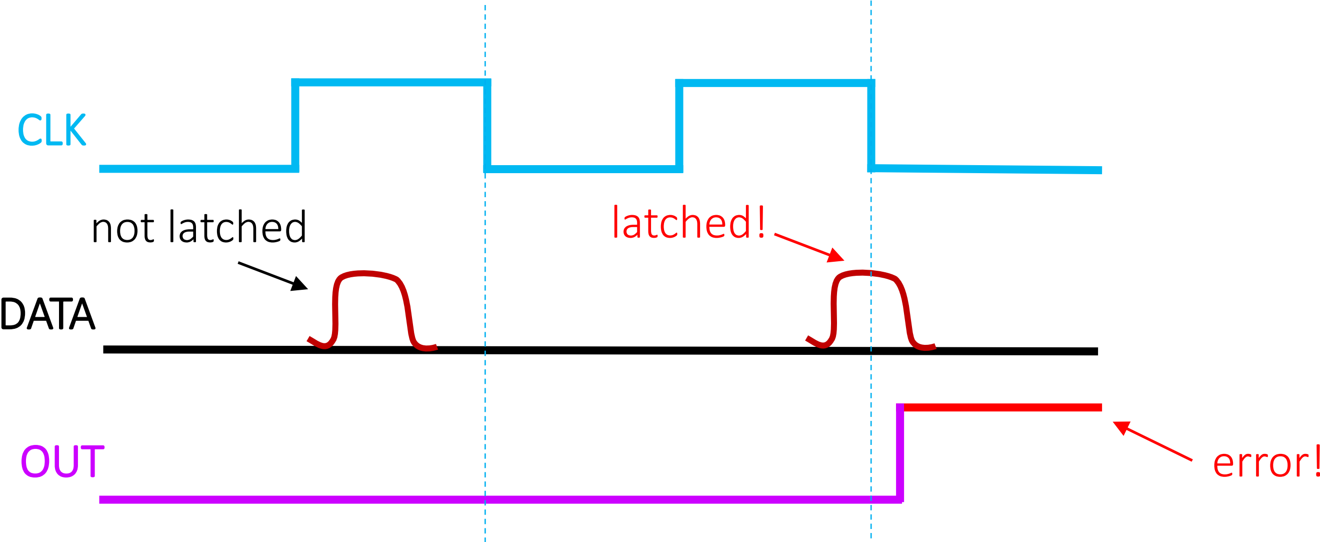
giulio.borghello@cern.ch | CERN EP-ESE-ME



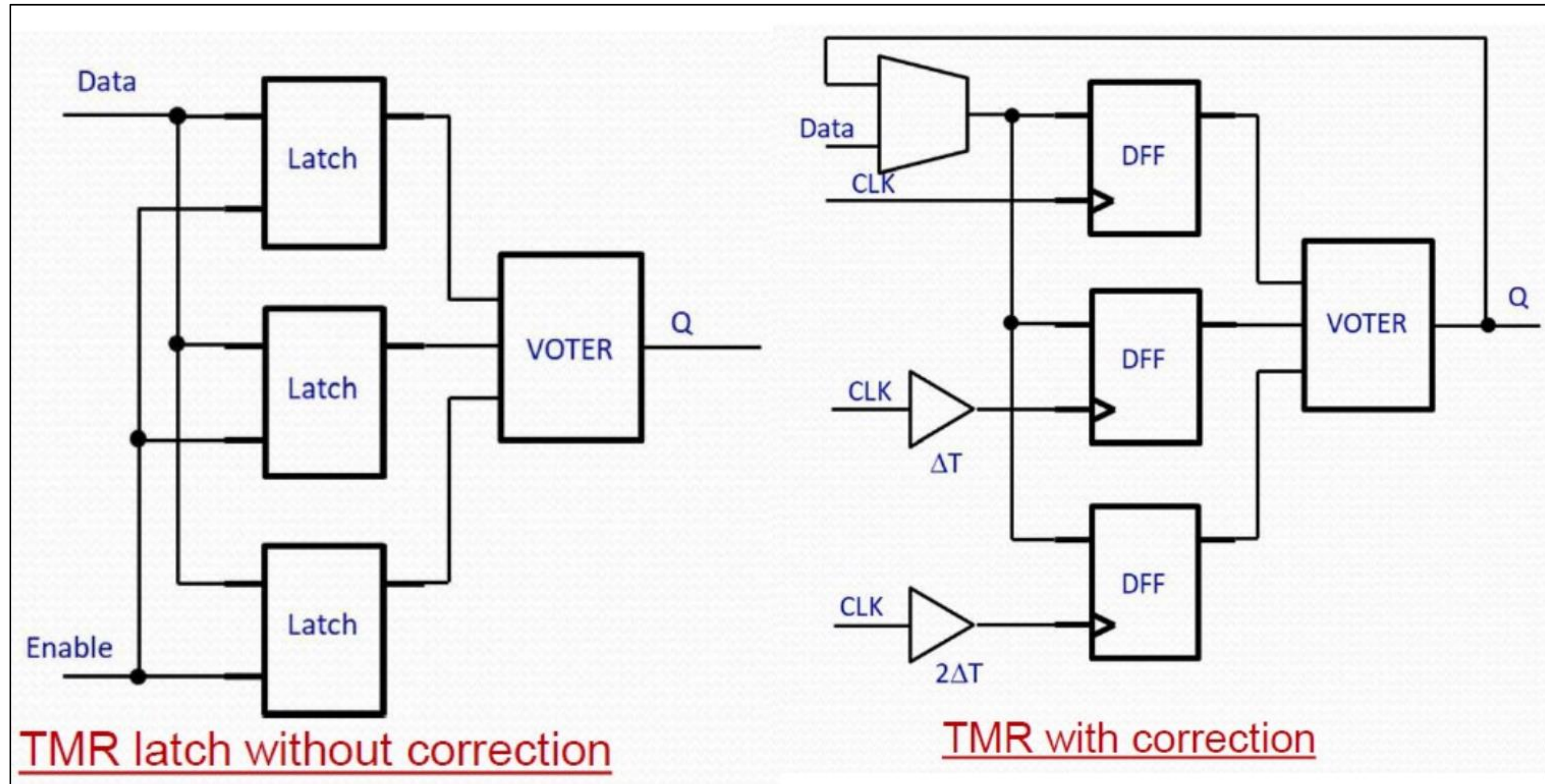


V. Ferlet-Cavrois, L. W. Massengill and P. Gouker, "Single Event Transients in Digital CMOS—A Review," in IEEE Transactions on Nuclear Science, vol. 60, no. 3, pp. 1767-1790, June 2013, doi: 10.1109/TNS.2013.2255624.


data latch at clock falling edge
SET
DATA = 0
OUT
CLK

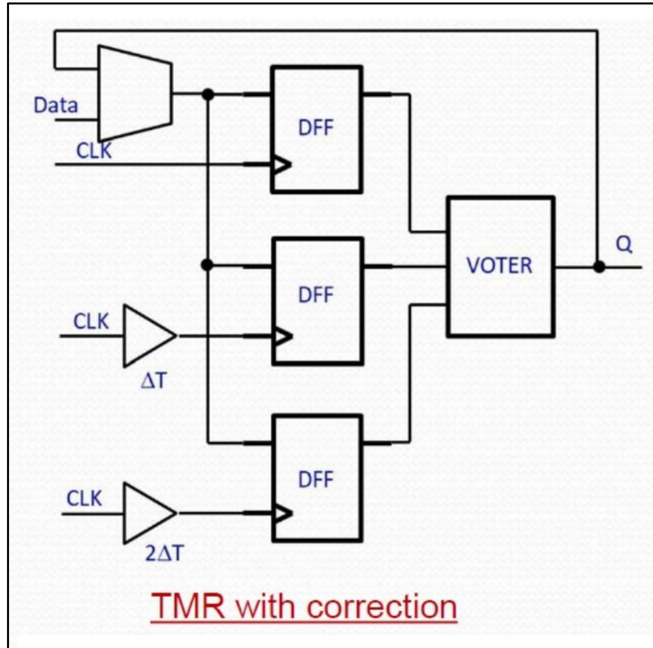

CLK
not latched
latched!
DATA
OUT
error!

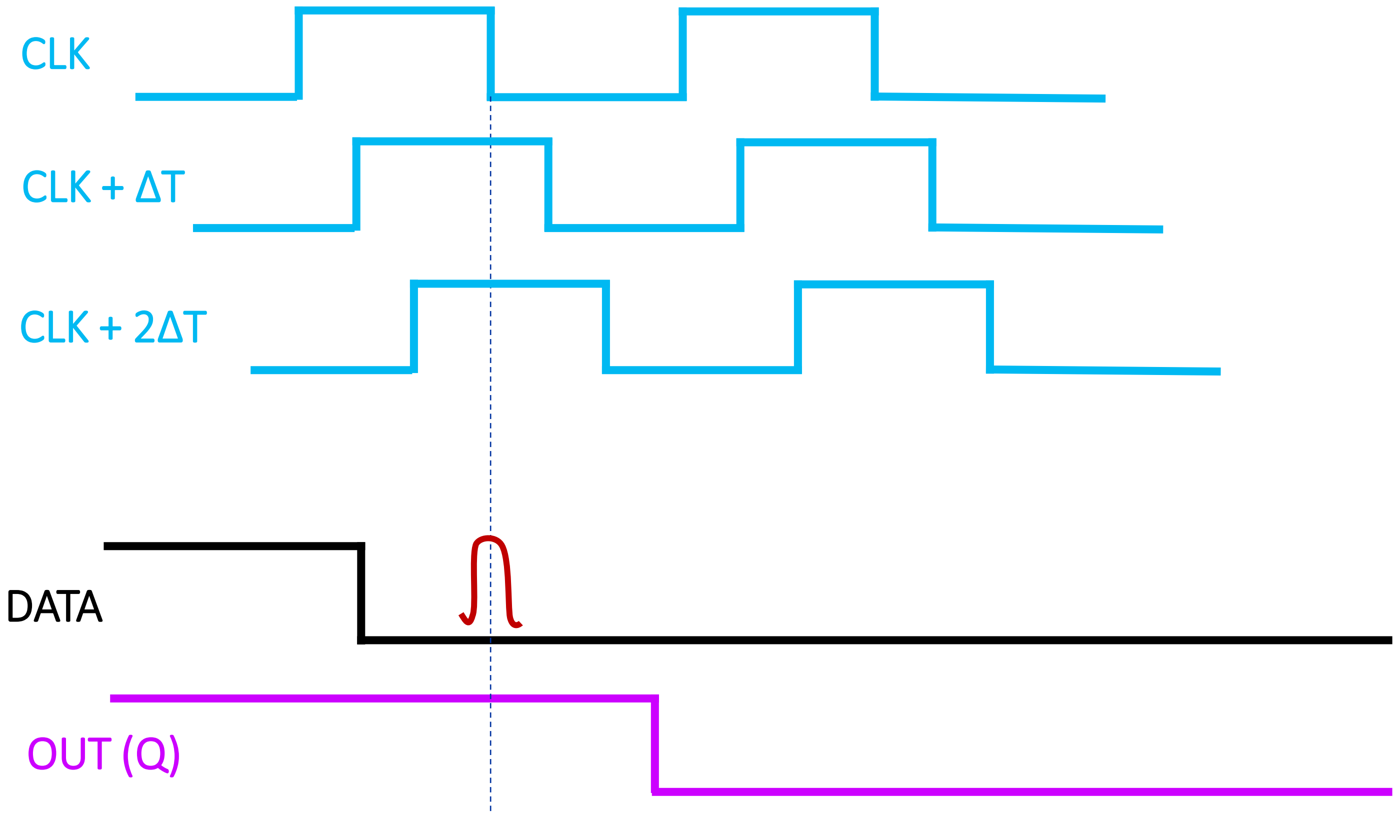
RD53*: triplicated clock tree with skew for SET filtering



https://indico.cern.ch/event/1038992/contributions/4363708/attachments/2256379/3829070/LHCC_RD53_June2021.pdf

*readout chips for the ATLAS and CMS pixel detector (https://rd53.web.cern.ch/)





This hardening techniques requires the knowledge of the SET pulse length!

typical pulse length ~100ps

stochastic effects

(a particle may or m...

(probability of interaction...

recently measured in chips for ALICE and LHCb!
(130nm CMOS technology)

[1] Mahmood S.M., Roeed K., ALICE Collaboration Collaboration, "Investigation of single event latch-up effects in the ALICE SAMPA ASIC", PoS, TWEPP2018 (2019), p. 023 5 p, 10.22323/1.343.0023, URL https://cds.cern.ch/record/2710375
[2] Lemos Cid E., Vázquez Regueiro P., "The VeloPix ASIC test results", PoS, Vertex 2017 (2018), p. 052, 10.22323/1.309.0052
[3] Faccio, Federico. "ASIC survival in the radiation environment of the LHC experiments: 30 years of struggle and still tantalizing." NIMA (2023)

non-destructive

- Single Event Upset
- Single Event Transient
- etc…

destructive

- Single Event Latch-Up
- etc…

$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1-\alpha_F) I_E$$

GND

VDD

V_D = VDD

p+ n+ n+ p+ p+ n+

Q_1

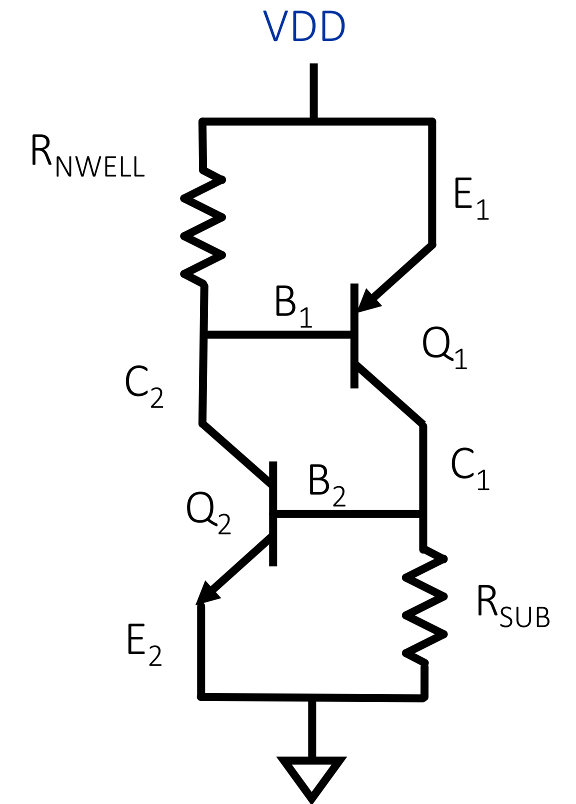
R_{NWELL}

n-well

Q_2

R_{SUB}

p-substrate



$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1 - \alpha_F) I_E$$

GND

V_D = VDD

VDD

p+ n+ n+ p+ p+ n+

Q_1

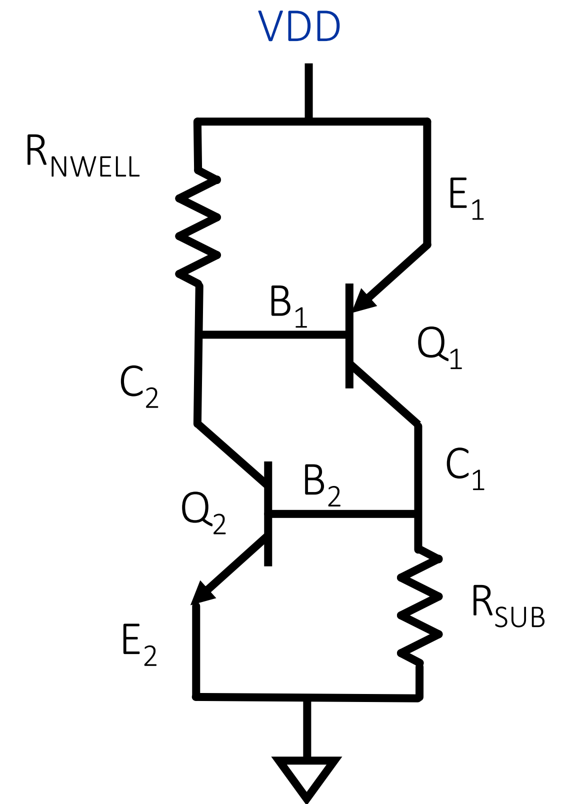
R_{NWELL}

n-well

R_{SUB}

Q_2

p-substrate



for this current to flow, V_{B1} must fall below V_D (diode in forward) ⇨ $V_{BE1} < 0$ ⇨ I_{E1} ↗↗

$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1 - \alpha_F) I_E$$

GND

VDD

V_D = VDD

p+ n+ n+ p+ p+ n+

Q_1

R_{NWELL}

n-well

Q_2

R_{SUB}

V_{B1} ↘↘

I_{C2} ↗↗

I_{E1} ↗↗

I_{E2} ↗↗

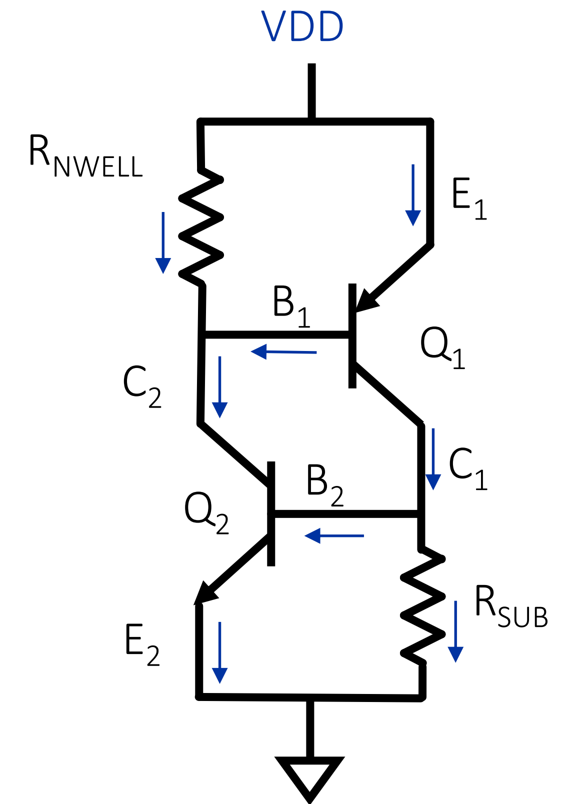
I_{C1} ↗↗

V_{B2} ↗↗

thyristor

p-substrate

if R_{SUB} high enough, V_{B2} can increase well above GND ⇨ $V_{BE2} > 0$ ⇨ I_{E2} ↗↗



Latch-up sensitivity depends on the value of R_{SUB} and R_{NWELL}

The higher their value, the higher the risk of latch-up.

R_{SUB} and R_{NWELL} depend on

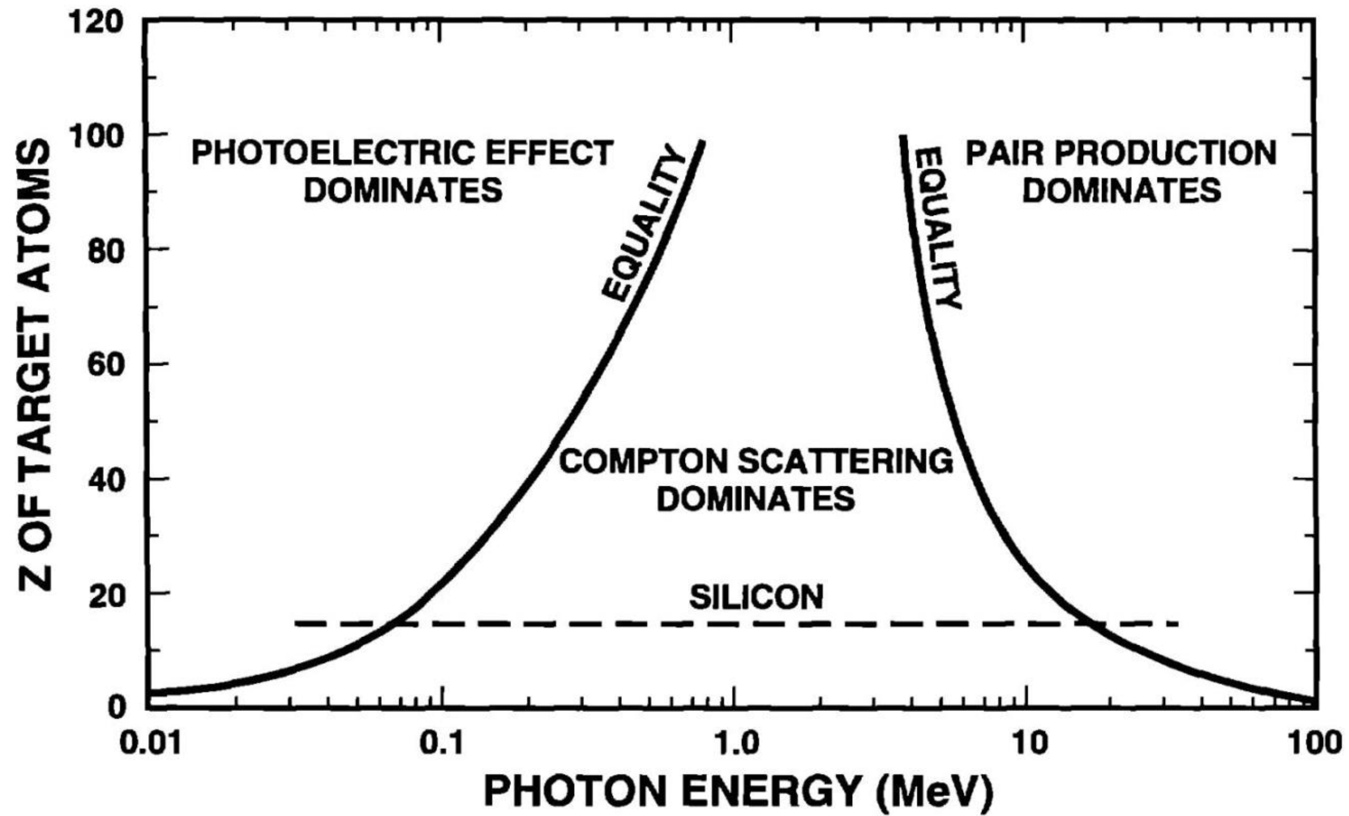
- doping levels (which cannot be changed in commercial technologies)
- distance between p-sub and n-well contacts

A common solution to reduce the risk of latch-up is to add **tap cells** in your design!
Tap cells connect p-sub to GND and n-well to VDD, limiting the physical distance between the contacts

THE END!

questions?

EXTRA SLIDES



R. D. Evans. *The atomic nucleus*. McGraw-Hill New York, 1955.

CERN & CMOS technology

We are using COMMERCIAL CMOS technologies:

- absolutely no control on the fabrication process
- no rad-hard components
- great performance/reliability
- great design tools

normalized $I_D(V_G=0V)$

channel width of parasitic channels (unknown**)

TID-induced parasitic current (normalized)

channel width

$$I_{OFF}(TID) =^{*} I_D(V_{GS}=0V) + I_{PAR}(TID) = \frac{W}{L} J_{OFF}^{MOS} + 2\frac{W_{PAR}}{L} J_{PAR}(TID)$$

channel length

$$\frac{I_{OFF}(TID)}{I_{OFF}(0)} = 1 + 2\frac{1}{W}\frac{W_{PAR}J_{PAR}(TID)}{J_{OFF}^{MOS}}$$

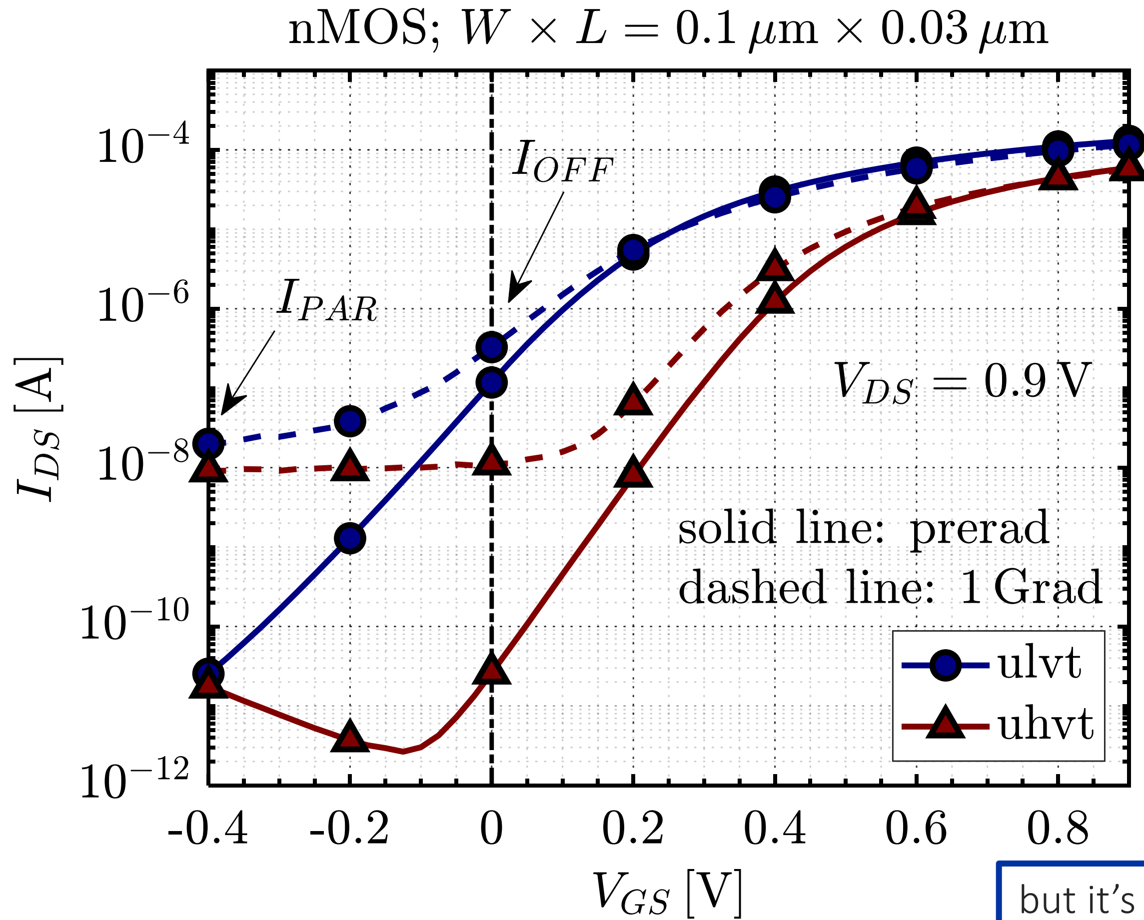
transistors with a smaller W or a lower J_{OFF}^{MOS} (e.g., high-VT) will see a higher **relative** increase!

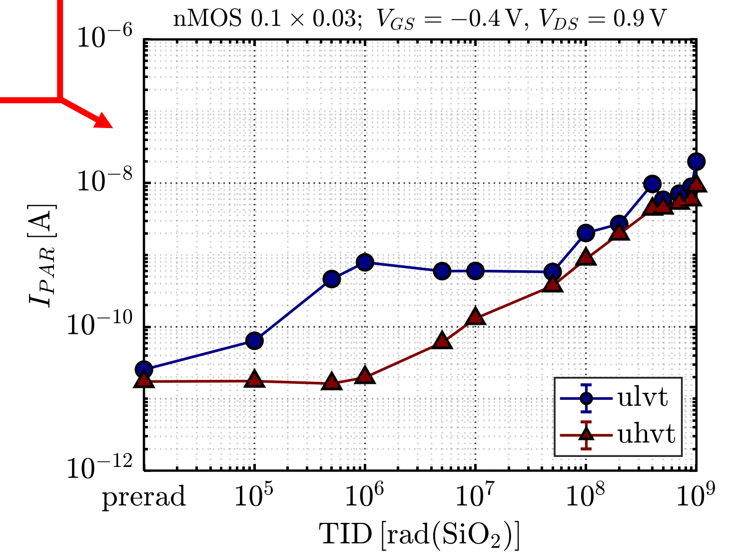
does not depend on L!

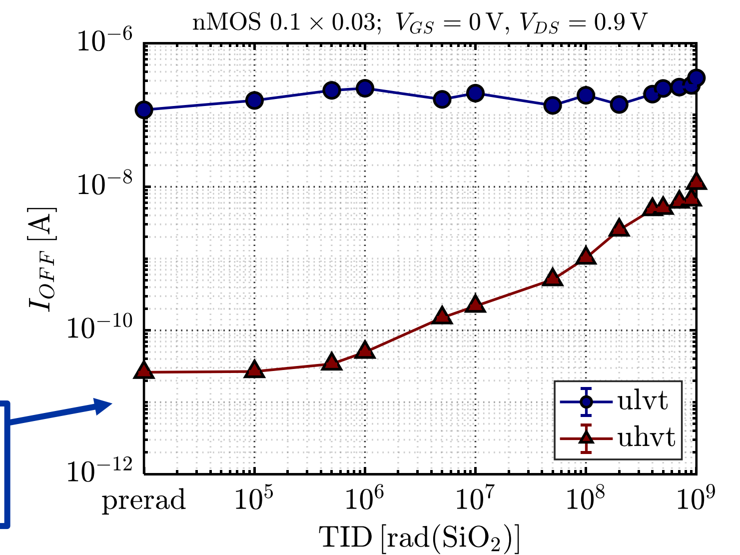
*these equations are a dreadful simplification of the actual behavior; they just serve to give a rough idea.

** I. S. Esqueda, et. al, "Two-dimensional methodology for modeling radiation-induced off-state leakage in CMOS technologies," in *TNS*, vol. 52, no. 6, pp. 2259-2264, Dec. 2005.

the parasitic current is only slightly dependent on the vth of the transistor



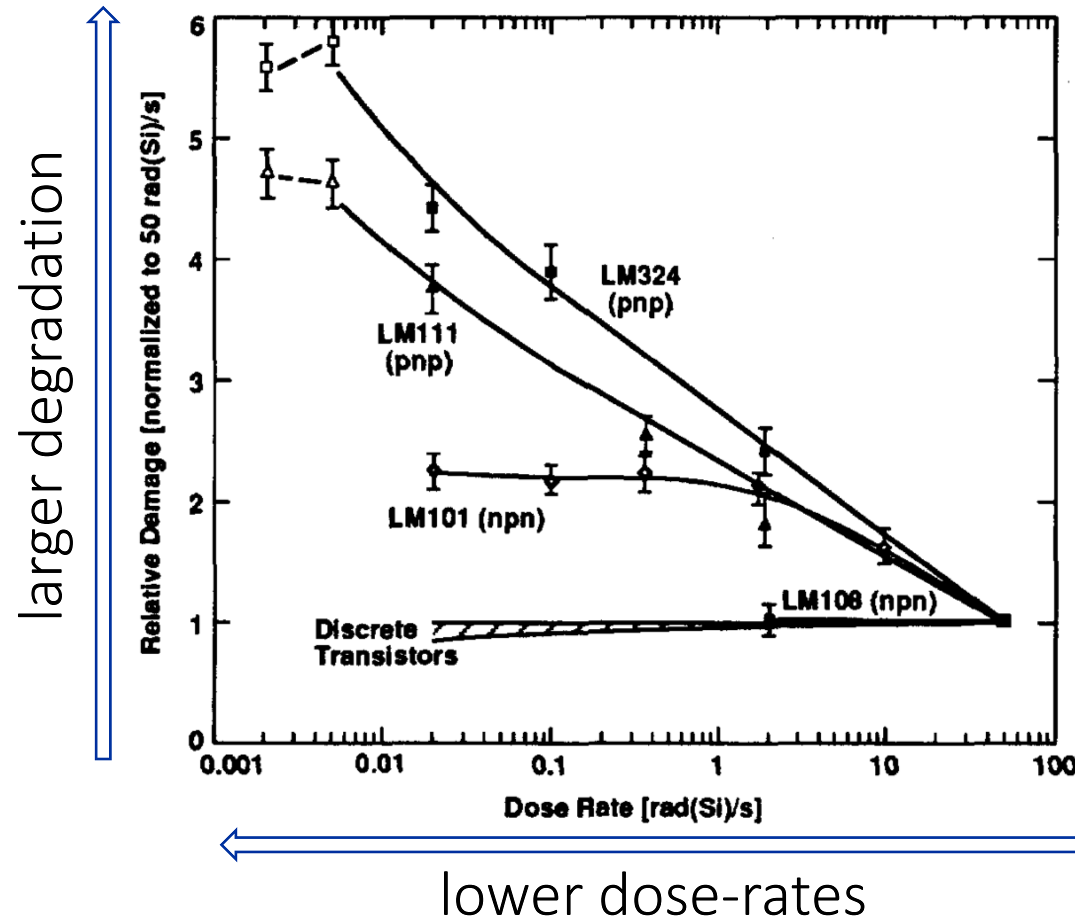




but it's impact on the I_{OFF} can be dramatically different!

enhanced low dose-rate sensitivity is a well-known phenomen in linear bipolar transistors[1] (not a time-dependent effect!)

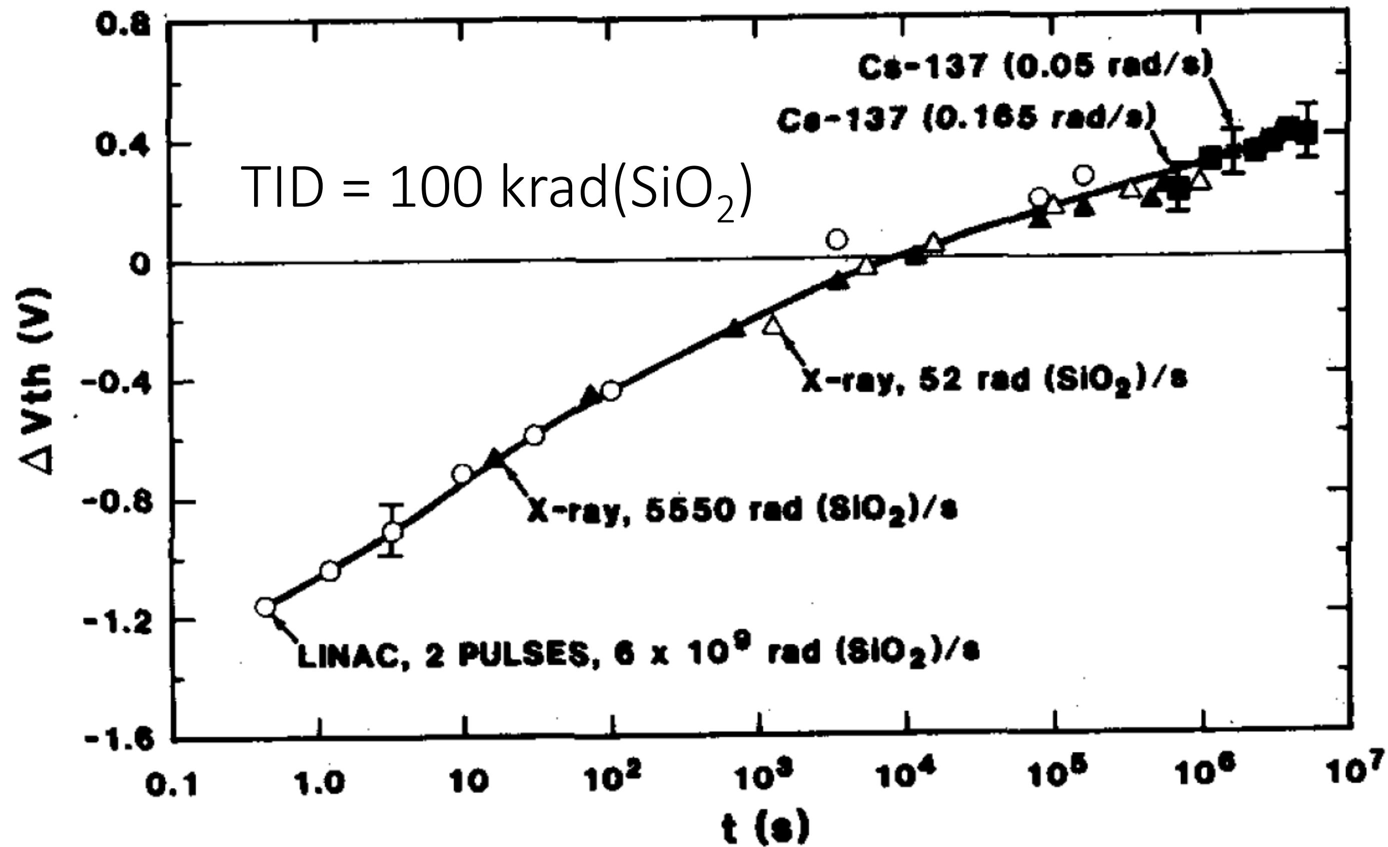
larger degradation



lower dose-rates

[1] A. H. Johnston, *et al.*, "Total dose effects in conventional bipolar transistors and linear integrated circuits," in *IEEE Trans. on Nucl. Sci.*, vol. 41, no. 6, pp. 2427-2436, Dec. 1994

CMOS technology is known to be immune to true dose-rate effects[2]



same time = same degradation

[2] D. M. Fleetwood, *et al.*, "Using laboratory X-ray and cobalt-60 irradiations to predict CMOS device response in strategic and space environments," in *IEEE Trans. on Nucl. Sci.*, vol. 35, no. 6, pp. 1497-1505, Dec. 1988

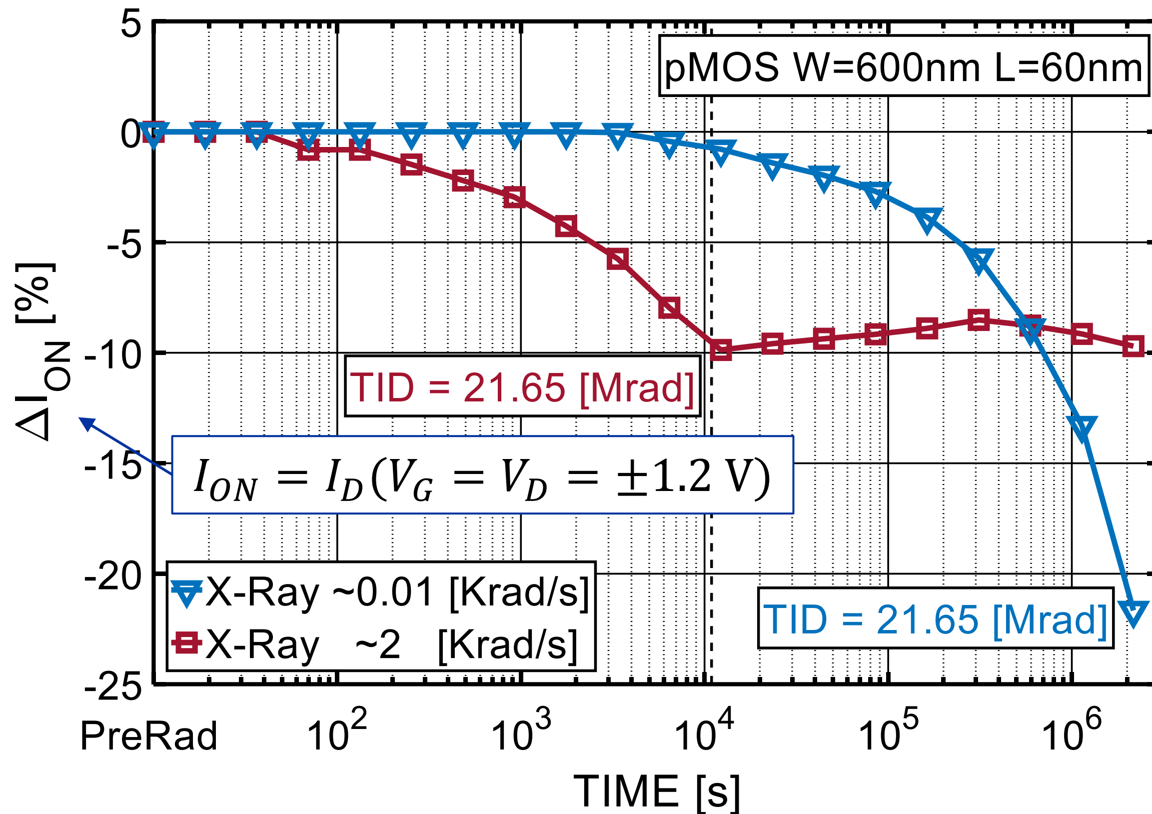
this difference is caused by the different charcteristics of the oxides dominating the radiation response[3]

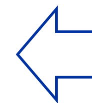
bipolar transistors → thick oxides, high defect density, low electric fields

CMOS technology (old) → gate oxide (thin, low defect density, high electric field)

[3] D. M. Fleetwood, "Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices," in *IEEE Trans. on Nucl. Sci.*, vol. 60, no. 3, pp. 1706-1730, June 2013

true enhanced low-dose-rate sensitivity in 65nm CMOS exposed to ultra-high TID[6]



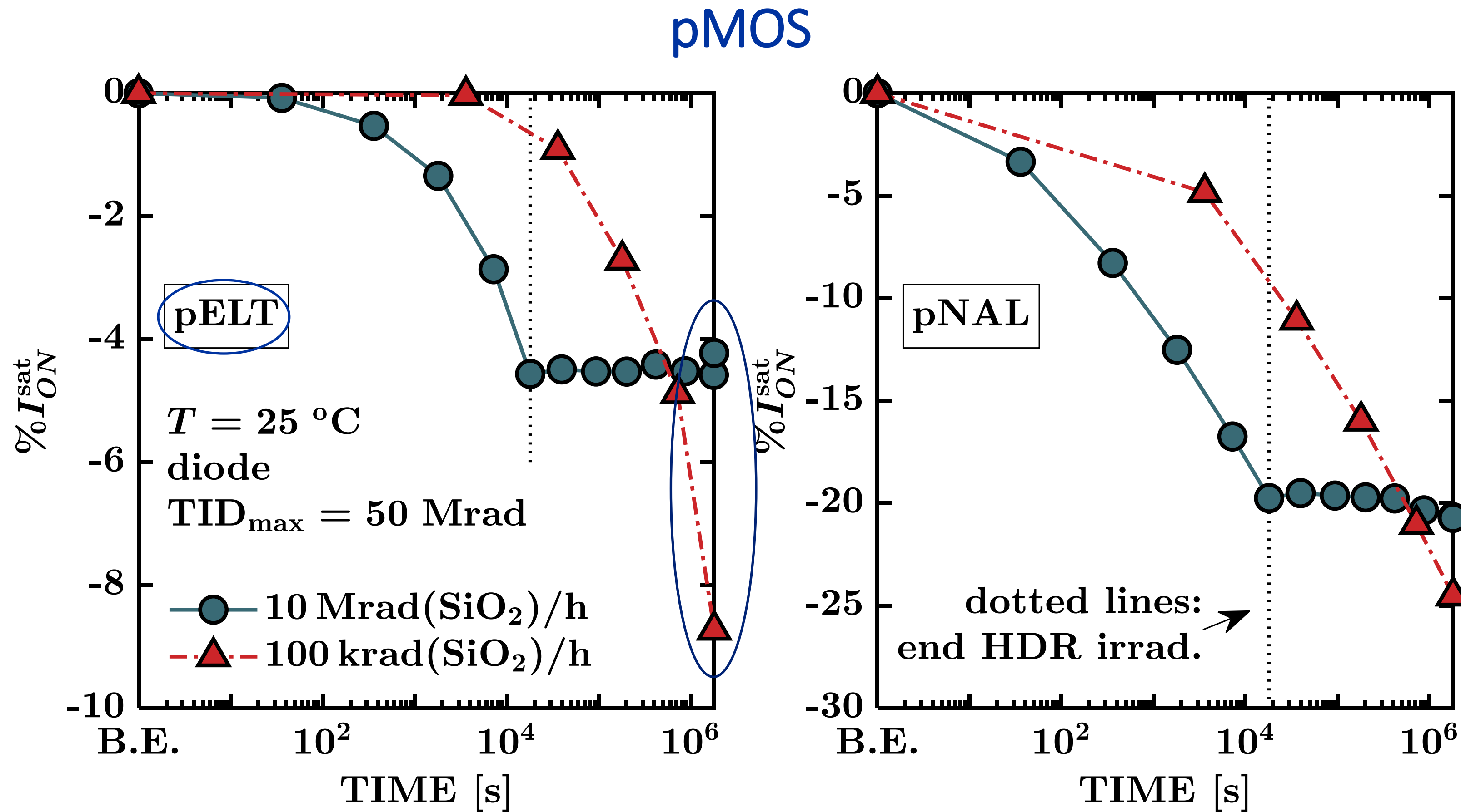


not a time-dependent effect!

[6] G. Borghello *et al.*, "Dose-Rate Sensitivity of 65-nm MOSFETs Exposed to Ultrahigh Doses," in *IEEE Trans. on Nucl. Sci.*, vol. 65, no. 8, pp. 1482-1487, Aug. 2018

ELT (spacers): true dose-rate sensitivity

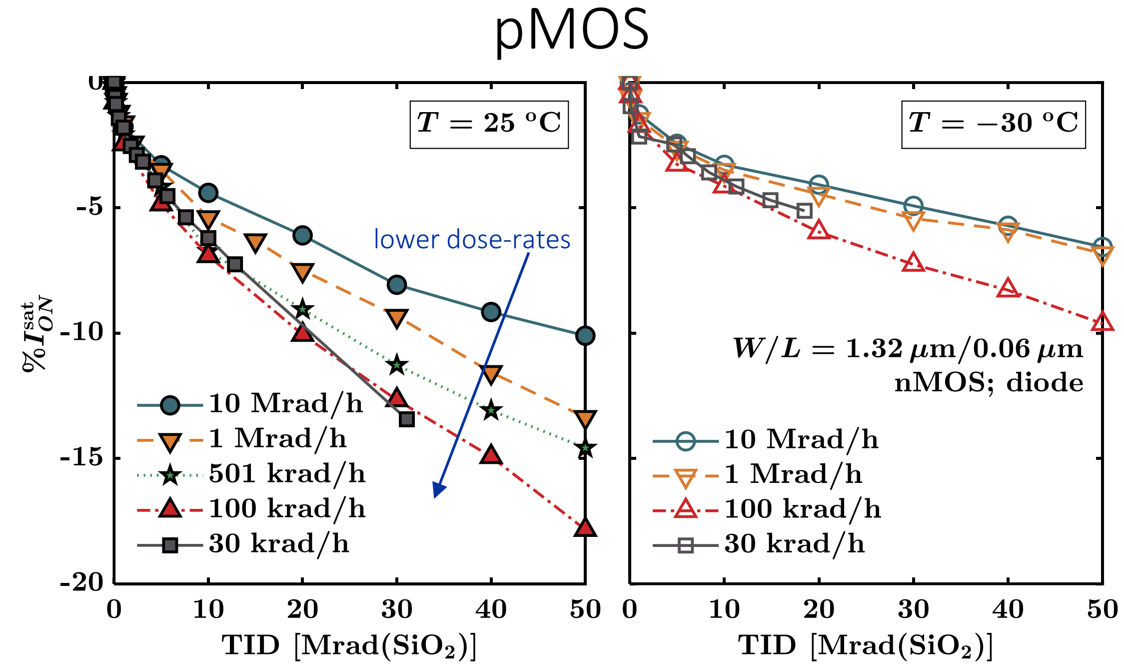
narrow and long (STI): ~same degradation at both high and low dose-rate



G. Borghello *et al.*, "Effects of Bias and Temperature on the Dose-Rate Sensitivity of 65-nm CMOS Transistors," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 573-580, May 2021, doi: 10.1109/TNS.2021.3062622.

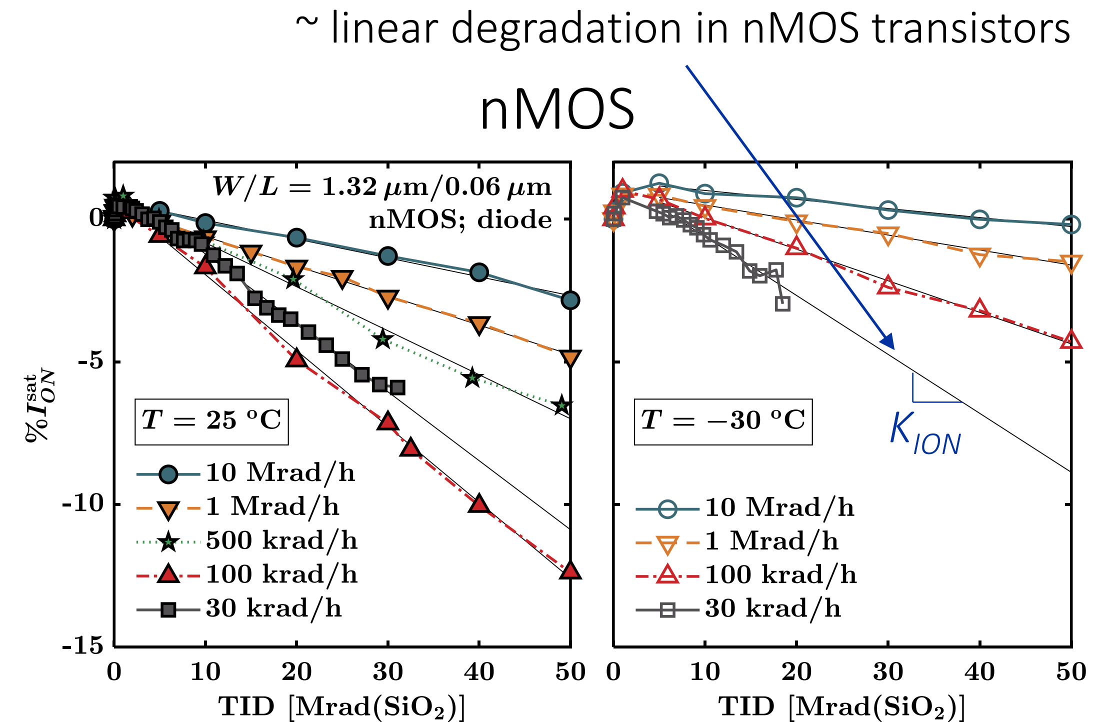
reduced dose-rate sensitivity at low-temperature

pMOS



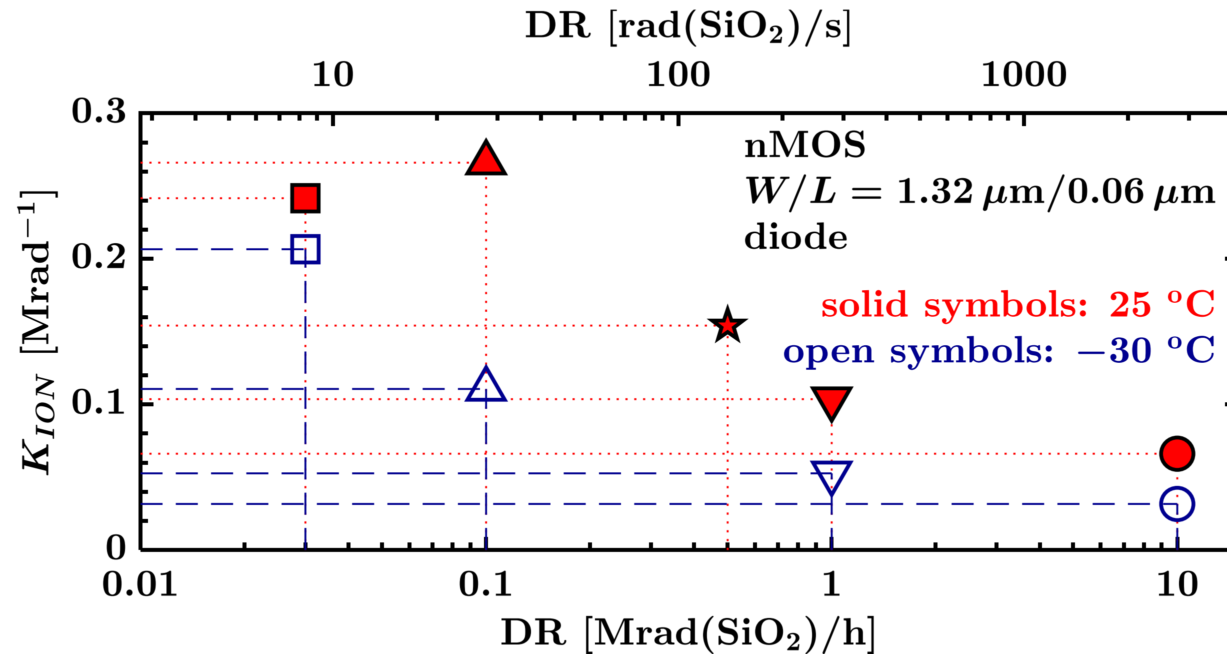
~ linear degradation in nMOS transistors

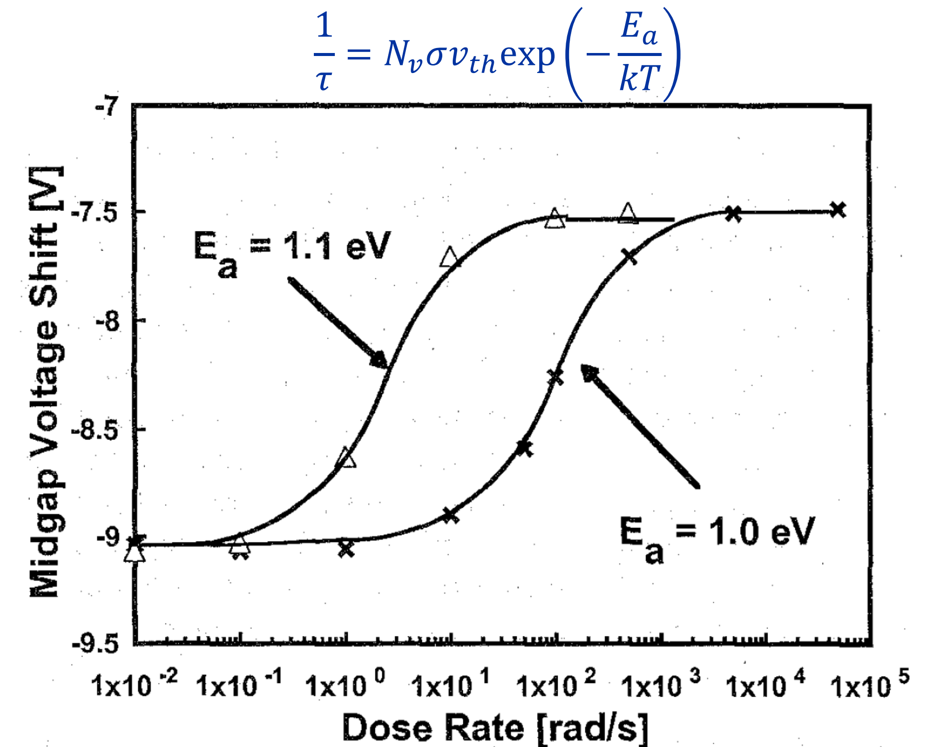
nMOS



G. Borghello *et al.*, "Effects of Bias and Temperature on the Dose-Rate Sensitivity of 65-nm CMOS Transistors," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 573-580, May 2021, doi: 10.1109/TNS.2021.3062622.

trend qualitatively similar to the enhanced low dose-rate sensitivity (ELDRS) measured in linear bipolar transistors (S-shaped curve)!!

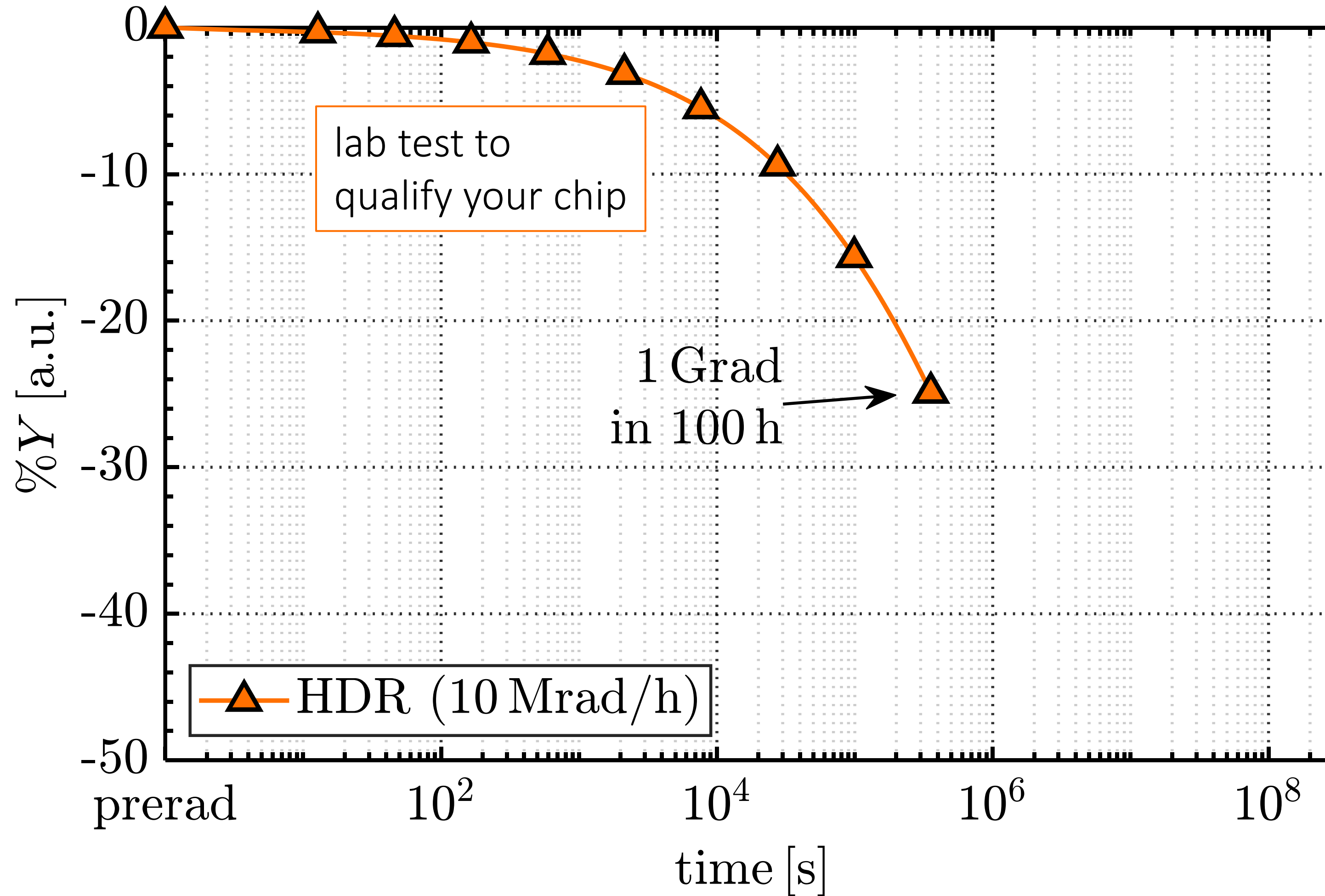




G. Borghello *et al.*, "Effects of Bias and Temperature on the Dose-Rate Sensitivity of 65-nm CMOS Transistors," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 573-580, May 2021, doi: 10.1109/TNS.2021.3062622.

[9] R. J. Graves, *et al.*, "Modeling low-dose-rate effects in irradiated bipolar-base oxides," IEEE Trans. Nucl. Sci. vol. 45, no. 6, pp. 2352–2360, Dec. 1998.

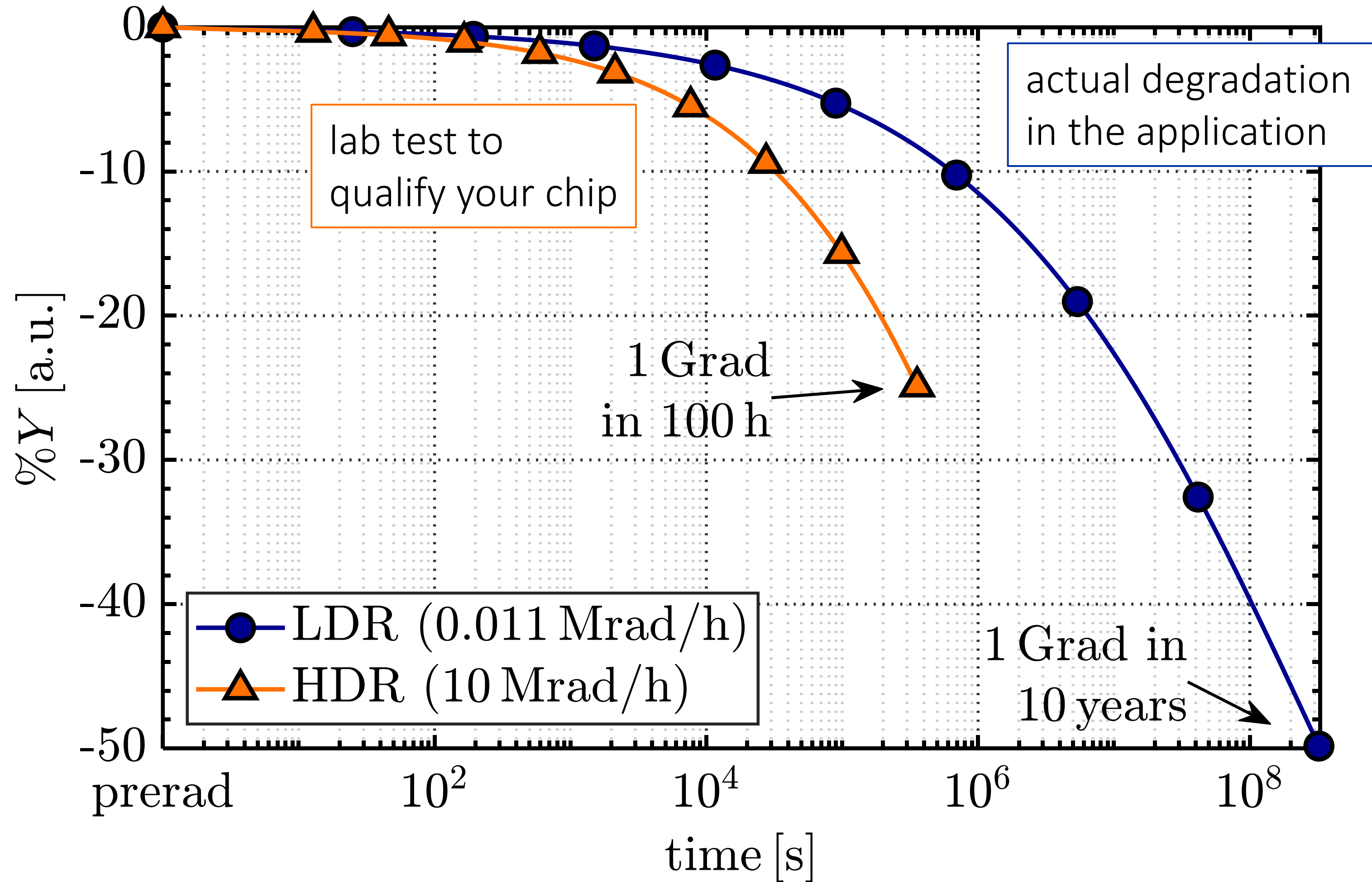
dose-rate (DR) VS time-dependent (TD) effects



Y = some parameter monitored during irradiation

100h = 3.6×10^5 s
10y = 3.15×10^8 s

dose-rate (DR) VS time-dependent (TD) effects



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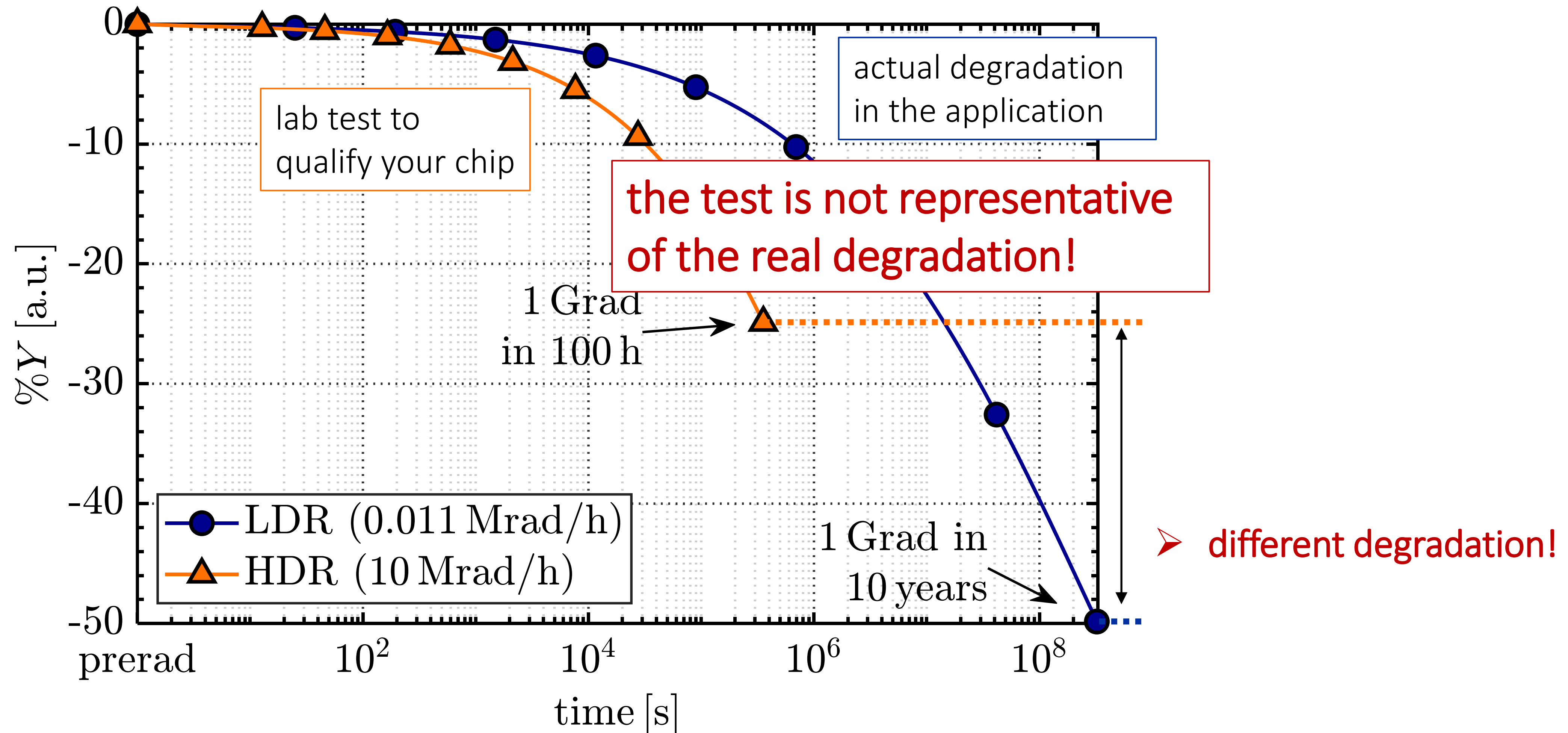
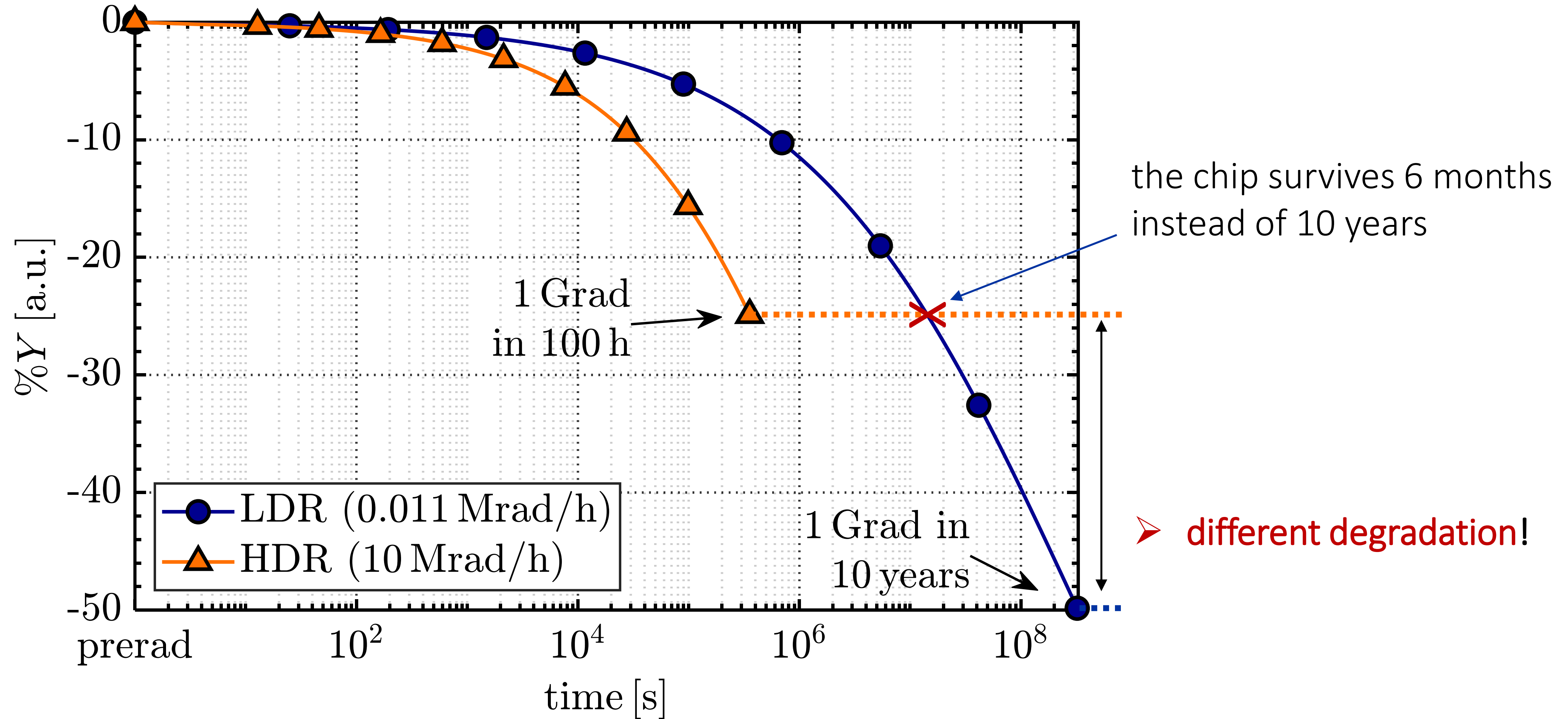
dose-rate (DR) VS time-dependent (TD) effects



- different degradation!

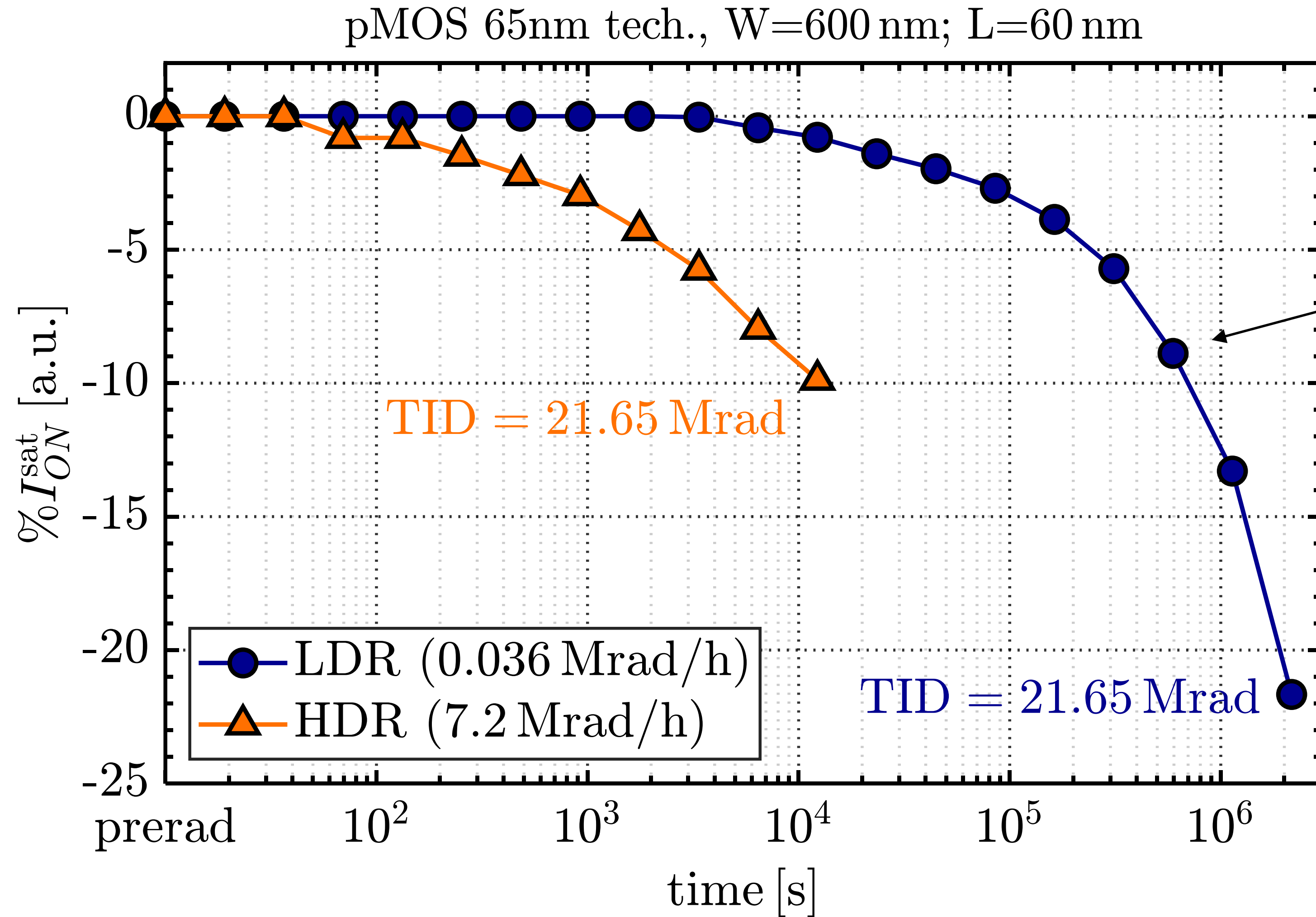
dose-rate (DR) VS time-dependent (TD) effects



the chip survives 6 months instead of 10 years

➢ different degradation!

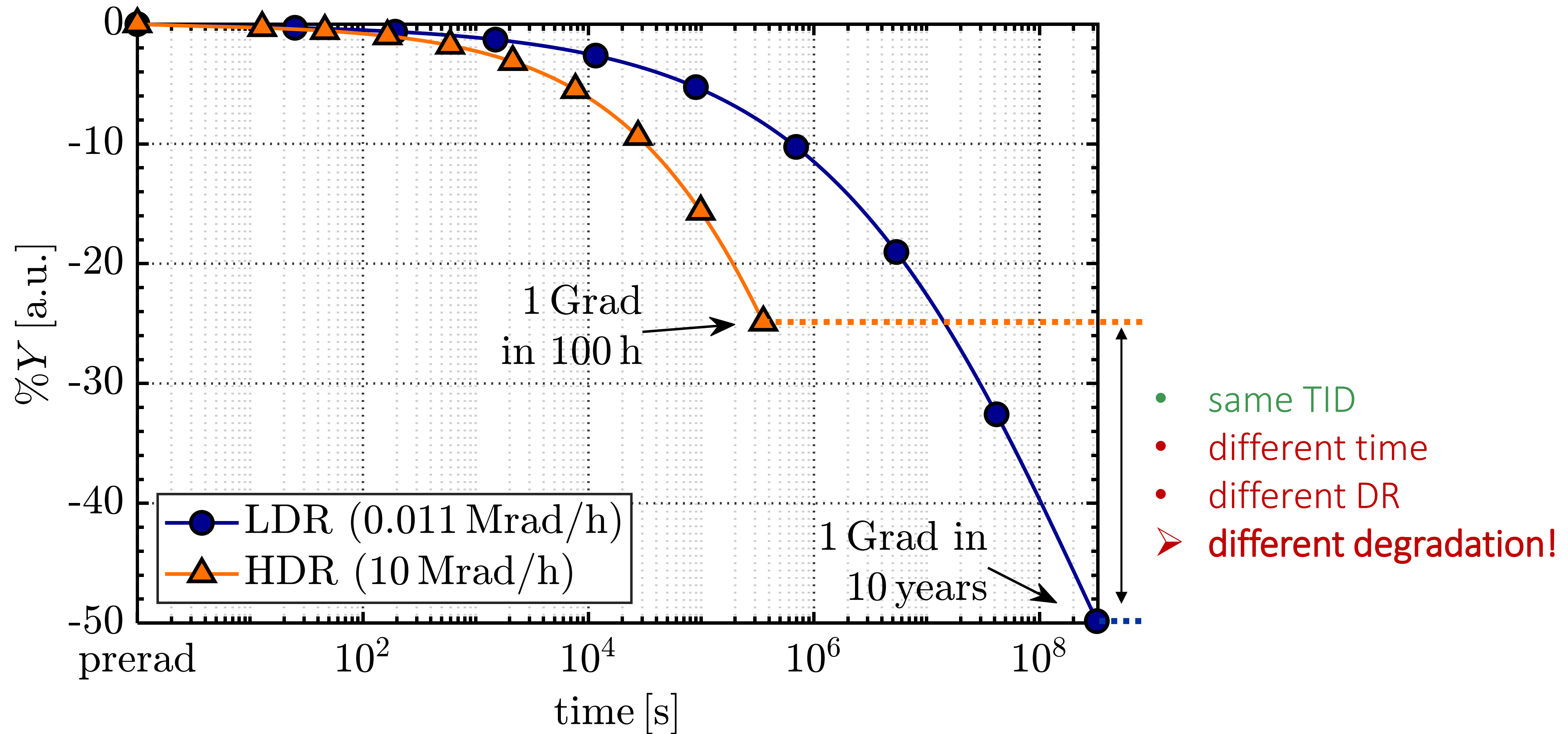
dose-rate (DR) VS time-dependent (TD) effects



real test in 65nm CMOS technology!

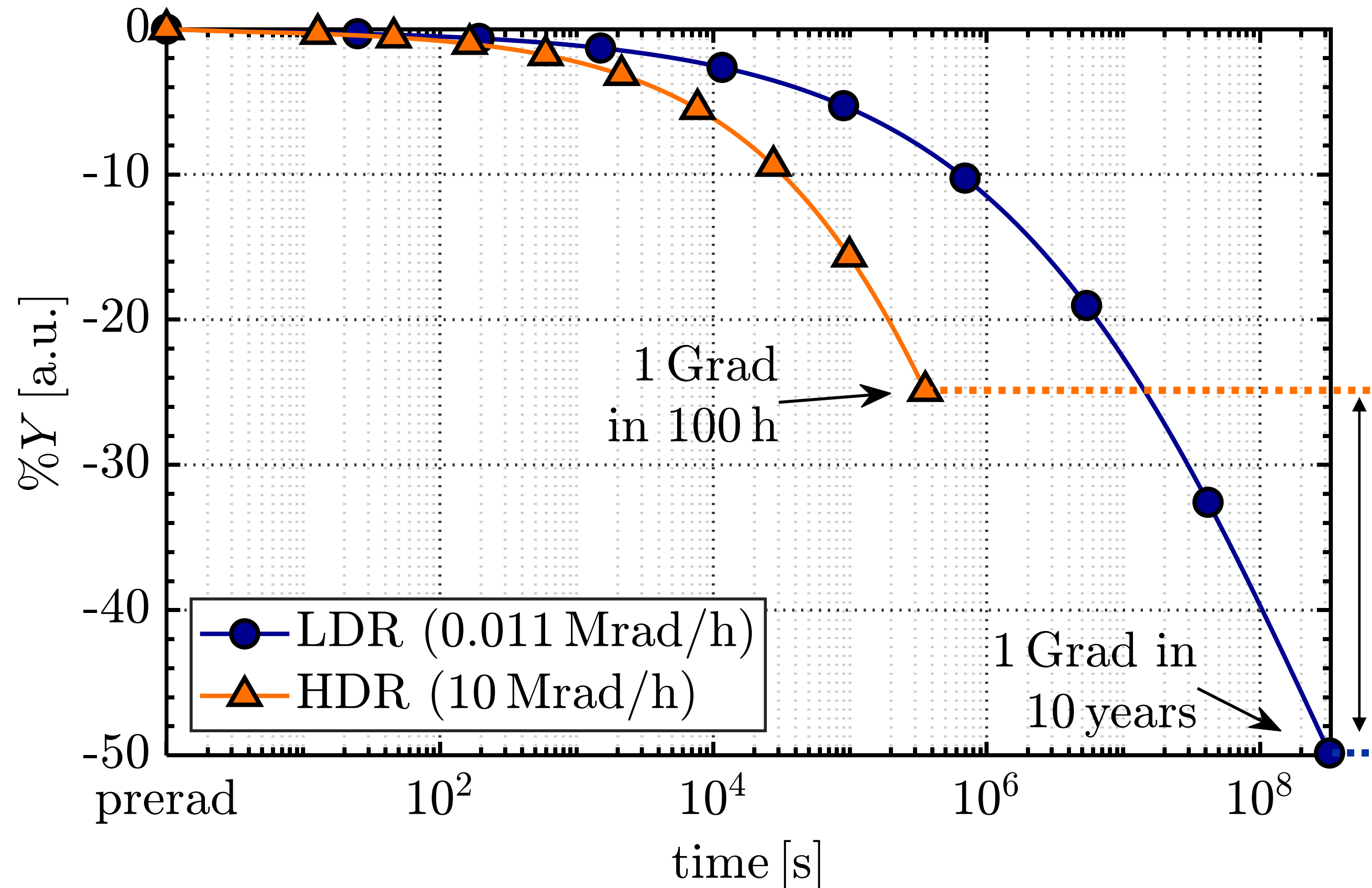
[1] G. Borghello et al., "Dose-Rate Sensitivity of 65-nm MOSFETs Exposed to Ultrahigh Doses," in IEEE Transactions on Nuclear Science, vol. 65, no. 8, pp. 1482-1487, Aug. 2018.
[2] G. Borghello et al., "Effects of Bias and Temperature on the Dose-Rate Sensitivity of 65-nm CMOS Transistors," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 573-580, May 2021

dose-rate (DR) VS time-dependent (TD) effects



- same TID
- different time
- different DR
- **different degradation!**

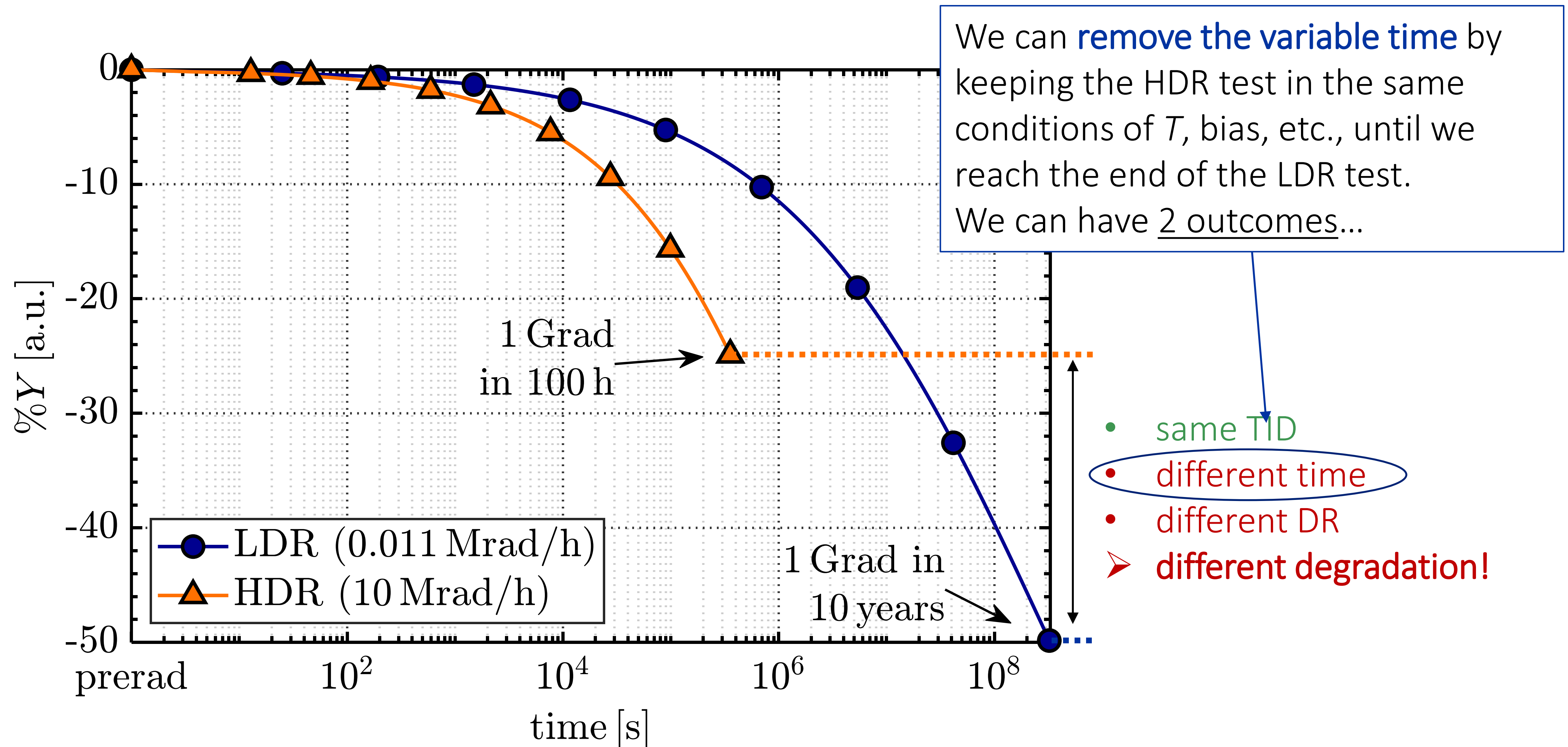
dose-rate (DR) VS time-dependent (TD) effects



Is the difference in degradation due to difference in time or difference in DR?

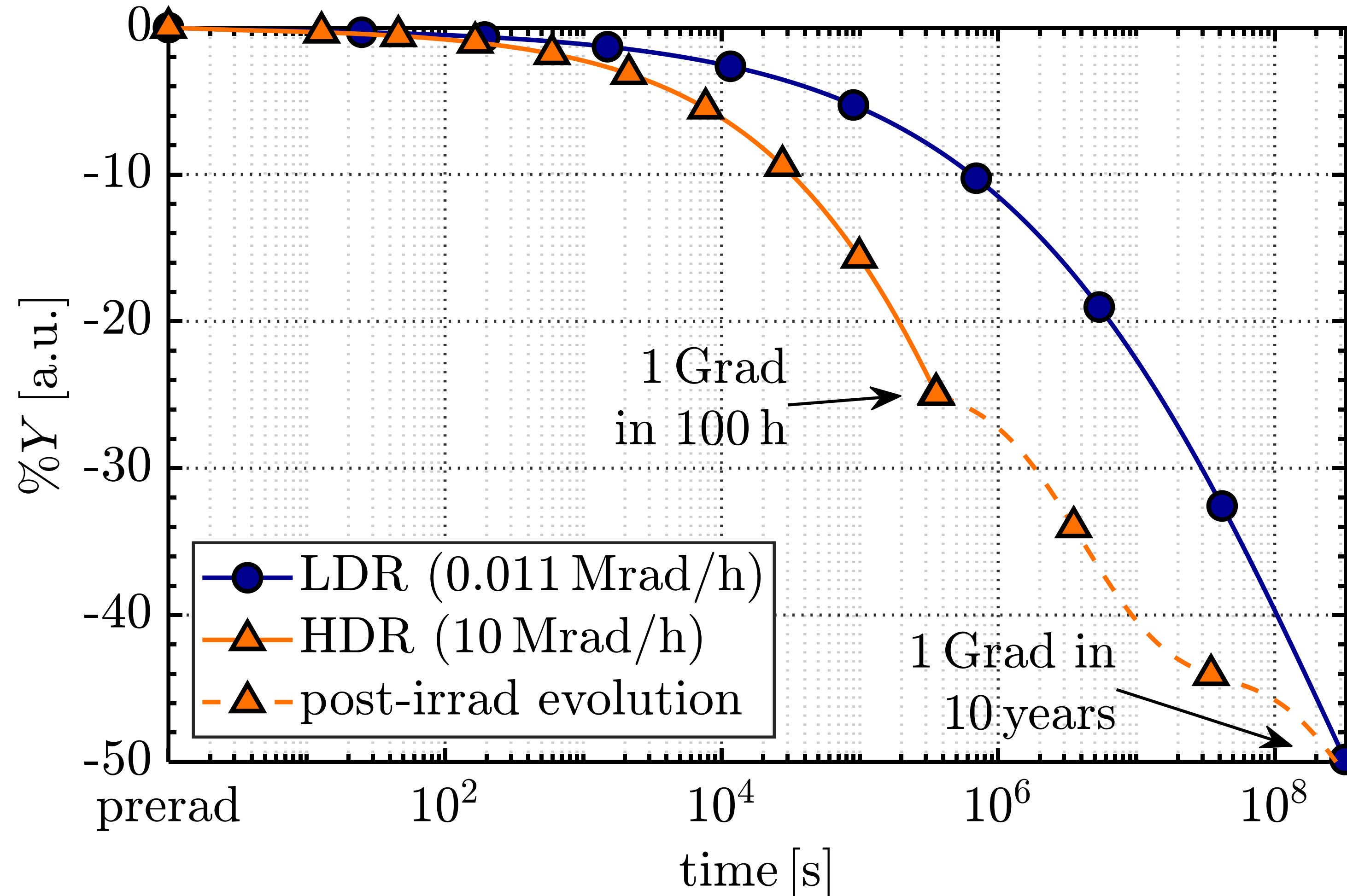
- same TID
- different time
- different DR
- **different degradation!**

dose-rate (DR) VS time-dependent (TD) effects



dose-rate (DR) VS time-dependent (TD) effects

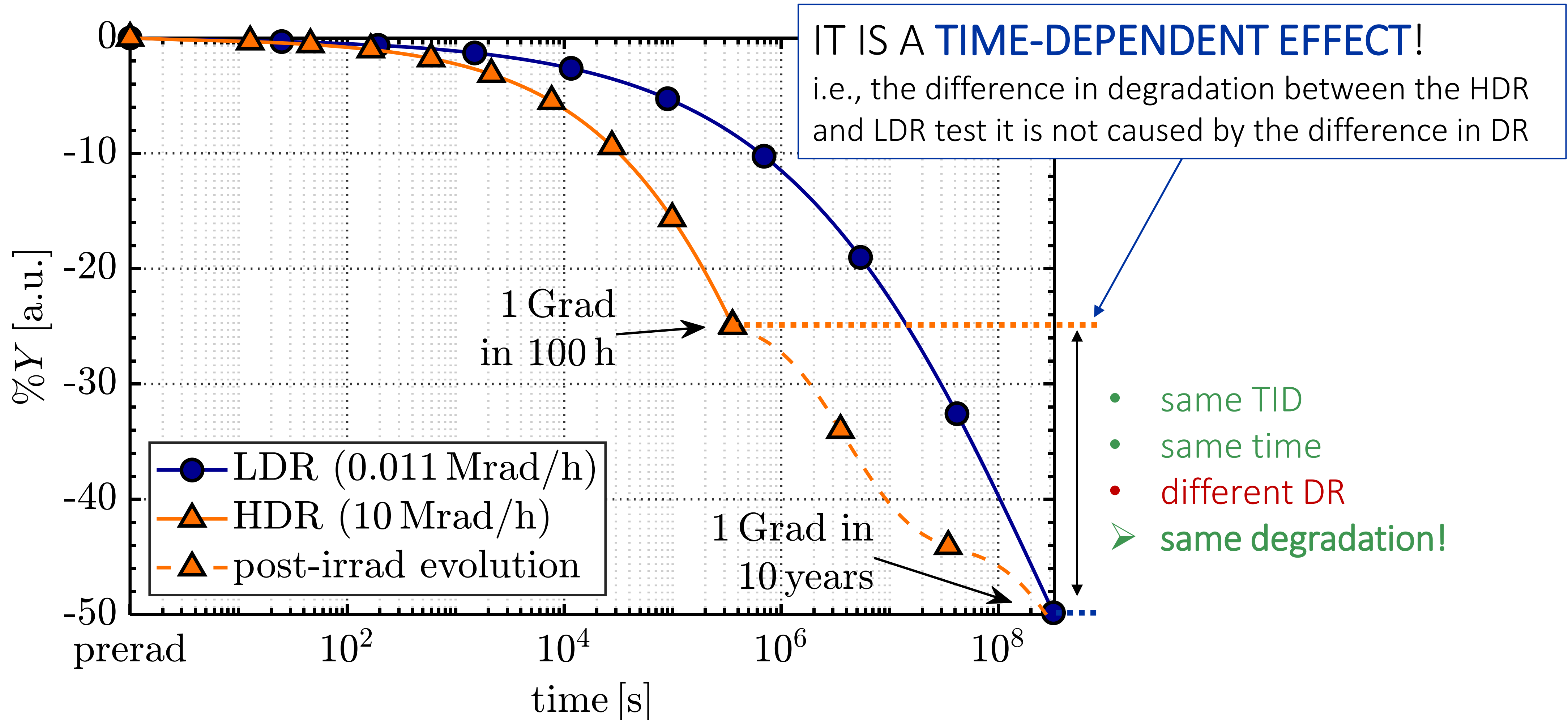
CASE 1: HDR and LDR tests have the **same degradation** at the end of the experiment



- same TID
- same time
- different DR
- ➢ **same degradation!**

dose-rate (DR) VS time-dependent (TD) effects

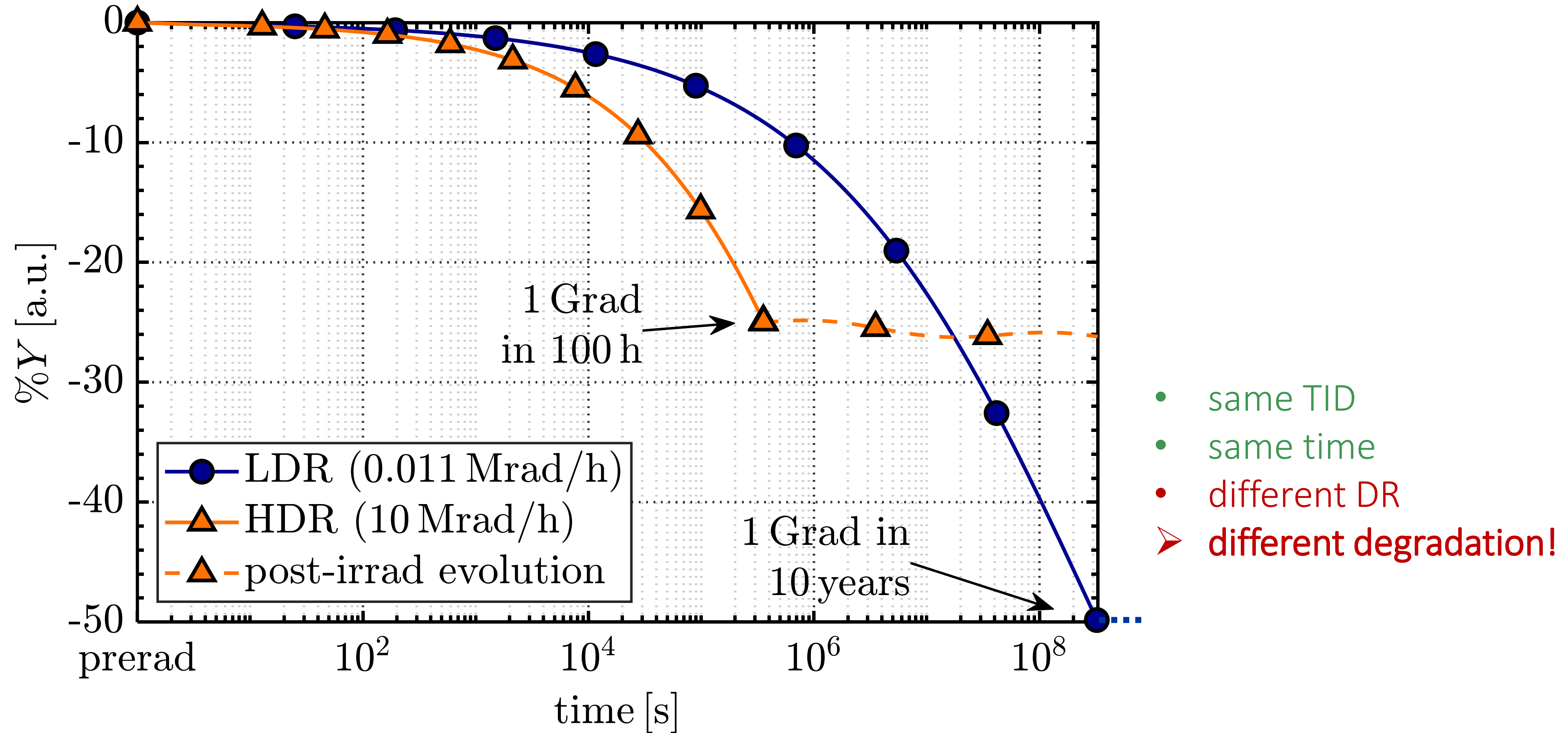
CASE 1: HDR and LDR tests have the same degradation at the end of the experiment



- same TID
- same time
- different DR
- ➢ same degradation!

dose-rate (DR) VS time-dependent (TD) effects

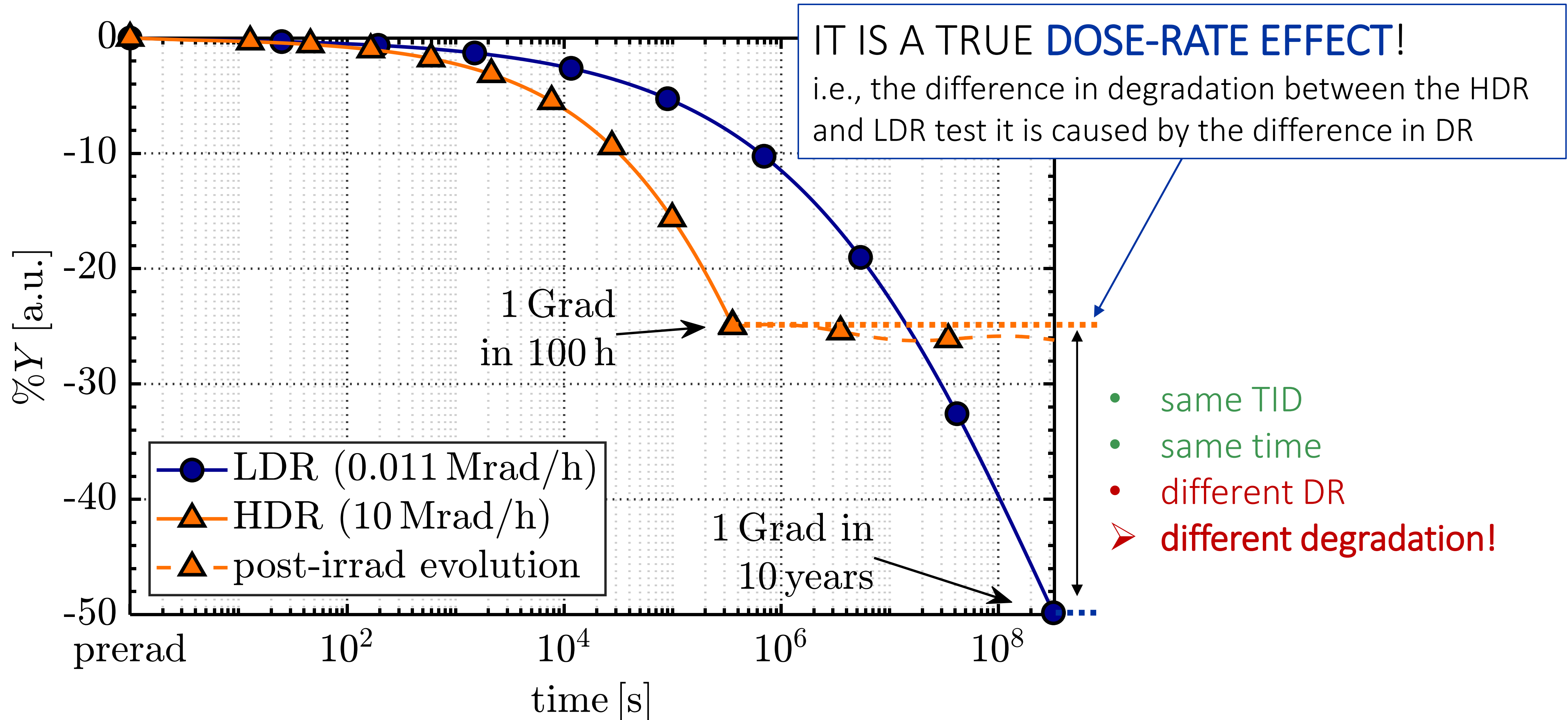
CASE 2: HDR and LDR tests have the different degradation at the end of the experiment



- same TID
- same time
- different DR
- ➢ different degradation!

dose-rate (DR) VS time-dependent (TD) effects

CASE 2: HDR and LDR tests have the different degradation at the end of the experiment

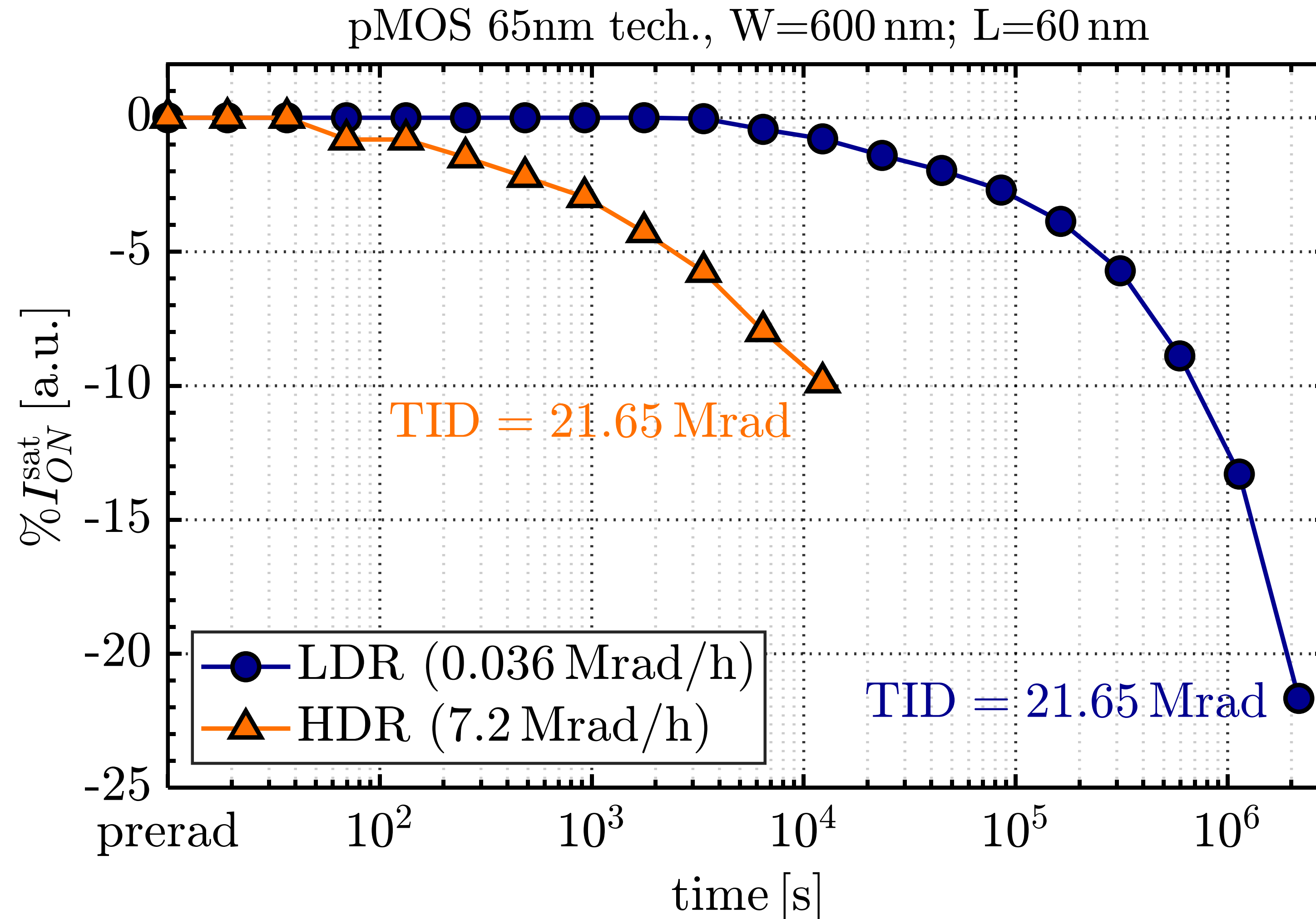


IT IS A TRUE DOSE-RATE EFFECT!
i.e., the difference in degradation between the HDR and LDR test it is caused by the difference in DR

- same TID
- same time
- different DR
- ➢ **different degradation!**

dose-rate (DR) VS time-dependent (TD) effects

CASE 2: HDR and LDR tests have the **different degradation** at the end of the experiment



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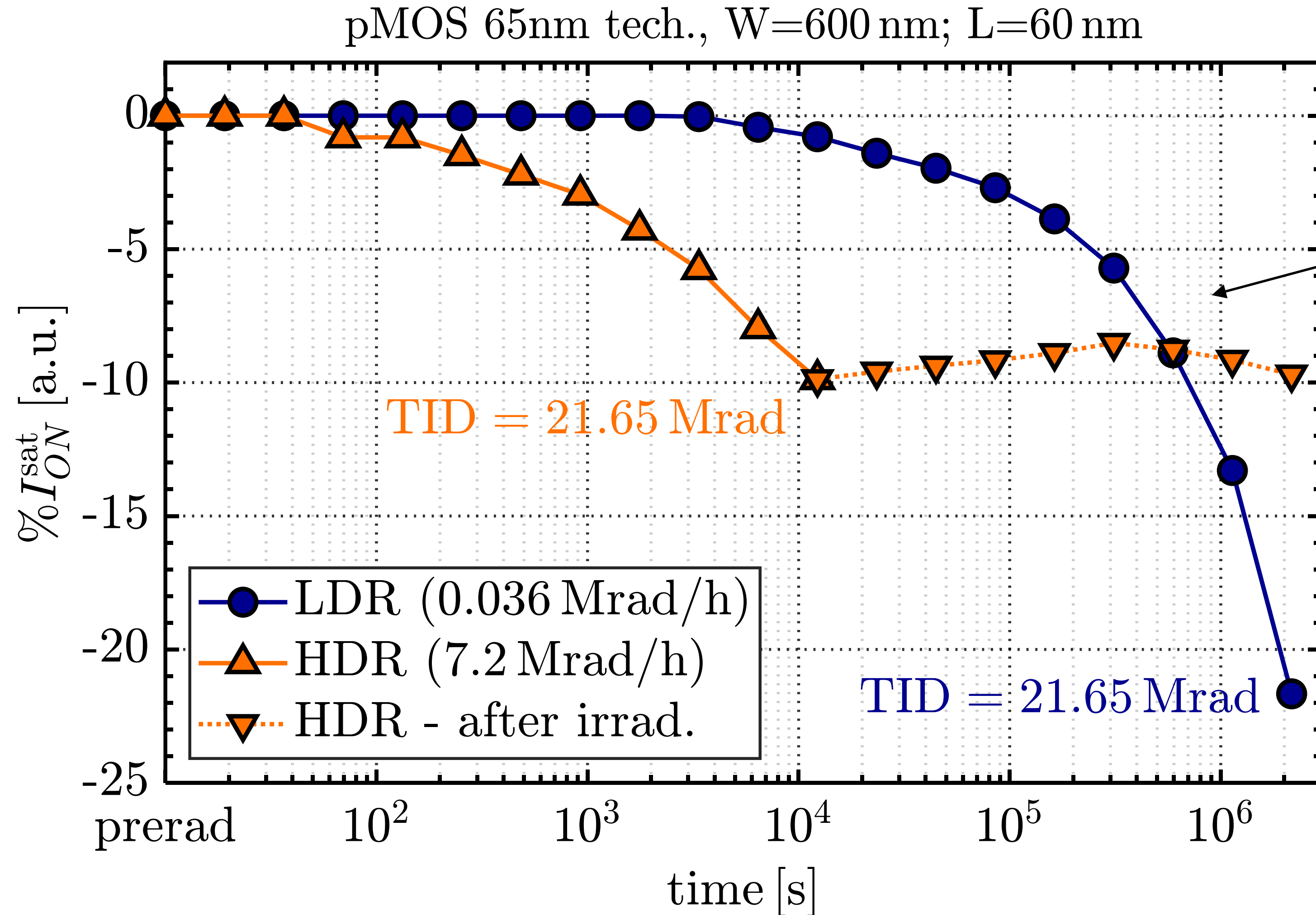
[2] G. Borghello et al., "Effects of Bias and Temperature on the Dose-Rate Sensitivity of 65-nm CMOS Transistors," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 573-580, May 2021

dose-rate (DR) VS time-dependent (TD) effects

CASE 2: HDR and LDR tests have the different degradation at the end of the experiment



True DR effect in 65nm CMOS technology!

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dose-rate (DR) VS time-dependent (TD) effects

How to estimate actual degradation (in a reasonable time)?

dose-rate (DR) VS time-dependent (TD) effects

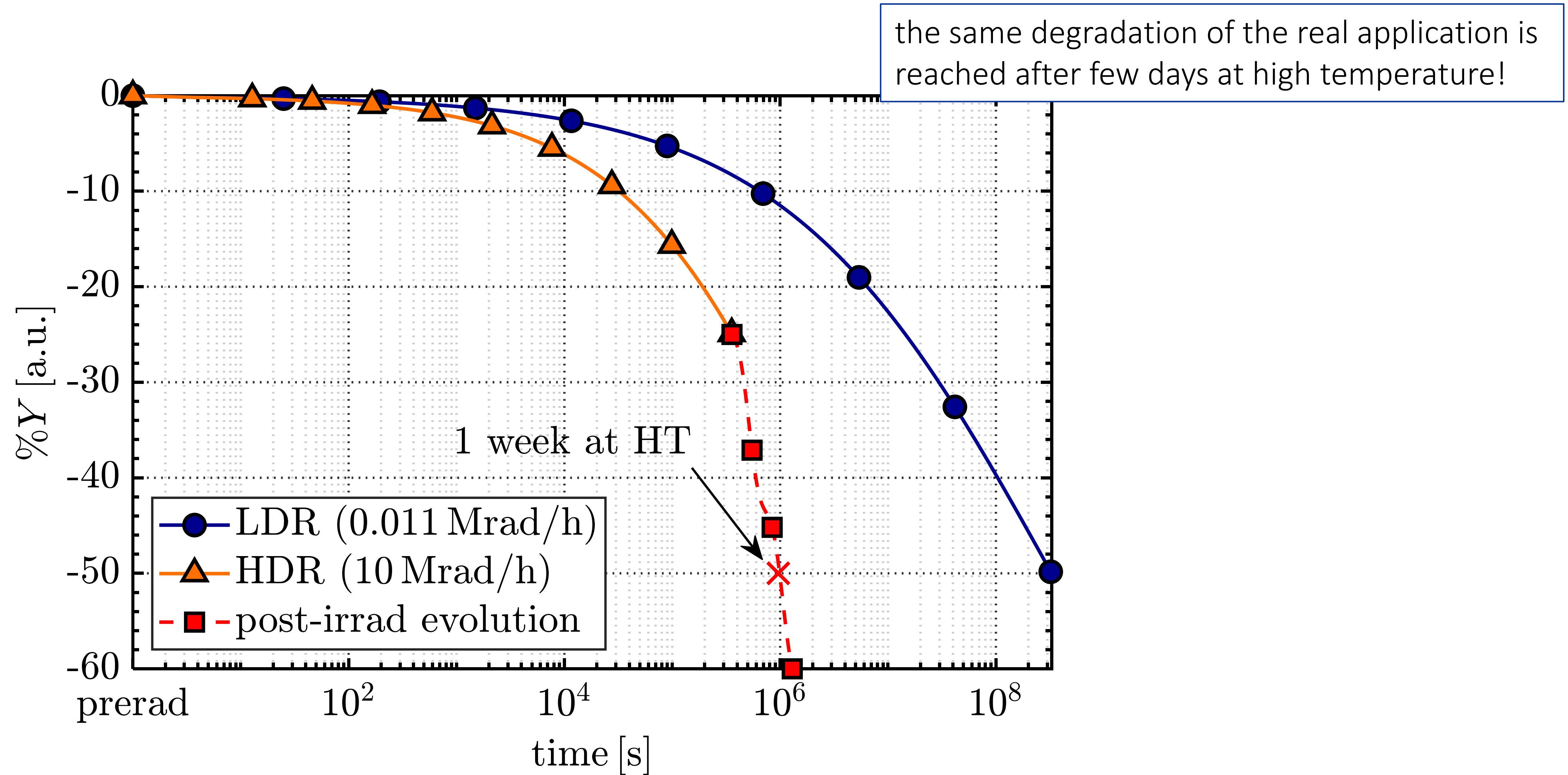
How to estimate actual degradation (in a reasonable time)?

TD effects are caused by transport/annealing of charge in the oxides

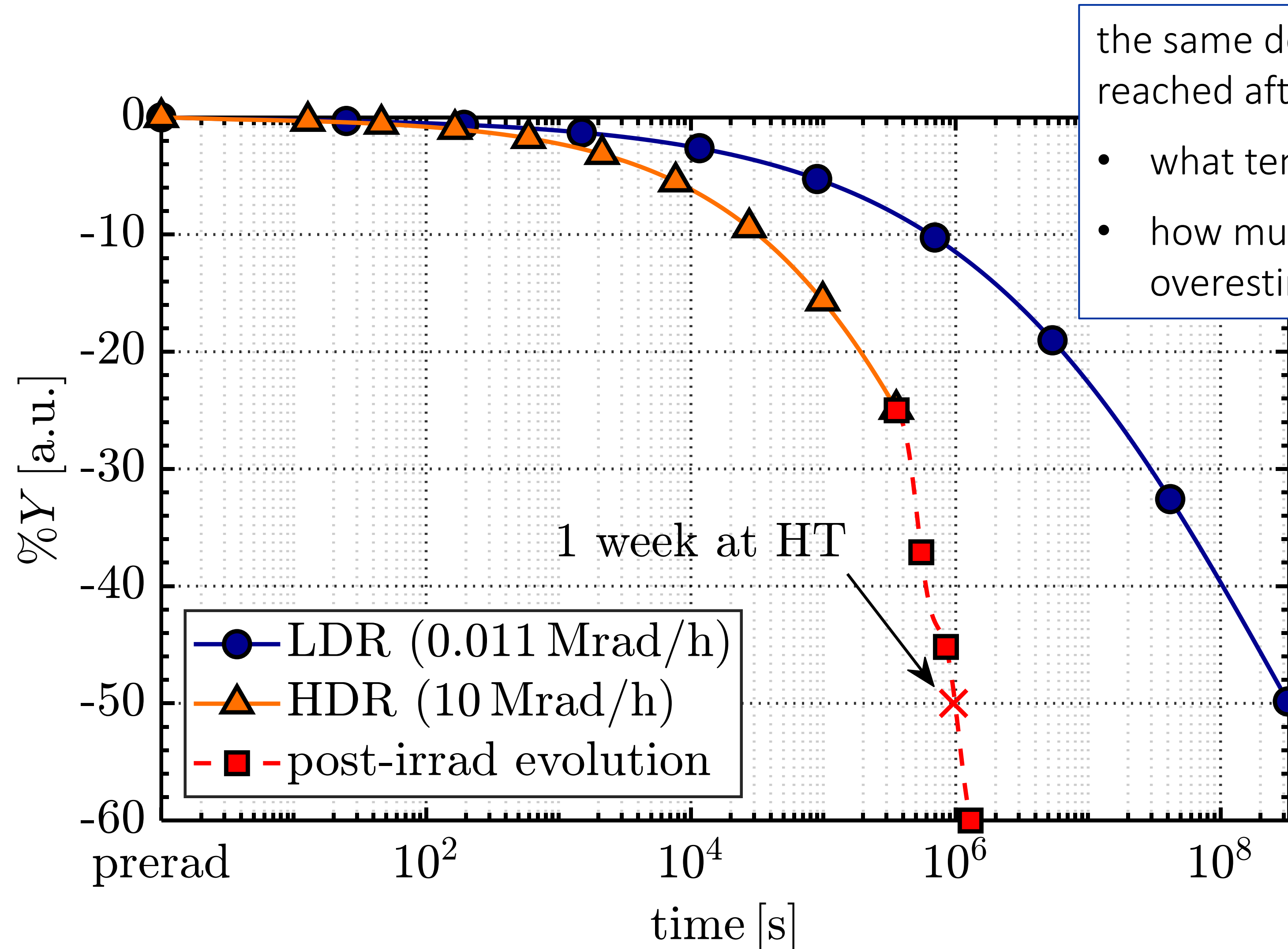
- these mechanisms can be accelerated by temperature!
- high temperature can be applied even after irradiation

time-dependent effects

the same degradation of the real application is reached after few days at high temperature!



time-dependent effects



the same degradation of the real application is reached after few days at high temperature!

- what temperature?
- how much time? (how not to under or overestimate the degradation)

time-dependent effects

Arrhenius equation:

$$Y(t,T) = Y_0 e^{-\sigma_A t}$$

$$\sigma_A = \frac{1}{\tau_I} e^{-\frac{E_A}{kT}}$$

E_A = activation energy [eV]: indicates how much a process is sensitive to temperature

τ_I = intrinsic time constant*: determines the rate of a process at a given temperature and E_A

*"Intrinsic time constant" is a name I made up for this presentation. In literature, 1/ τ_I is usually written as "*A*" and it is quite boringly called "pre-exponential factor".

dose-rate (DR) VS time-dependent (TD) effects

How to estimate actual degradation (in a reasonable time)?

We want to find the time t_{TEST} at which the degradation at temperature T_{TEST} is equal to the degradation in the condition of the real application T_{APP}, t_{APP}

$$Y(t_{TEST}, T_{TEST}) = Y(t_{APP}, T_{APP})$$

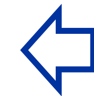
time-dependent effects

We want to find the time t_{TEST} at which the degradation at temperature T_{TEST} is equal to the degradation in the condition of the real application T_{APP}, t_{APP}

$$Y(t_{TEST}, T_{TEST}) = Y(t_{APP}, T_{APP}) =$$

$$= \cancel{Y_0} e^{-\sigma_A(T_{TEST})t_{TEST}} = \cancel{Y_0} e^{-\sigma_A(T_{APP})t_{APP}}$$

$$\Rightarrow \frac{t_{TEST}}{\cancel{\tau_I}} e^{-\frac{E_A}{kT_{TEST}}} = \frac{t_{APP}}{\cancel{\tau_I}} e^{-\frac{E_A}{kT_{APP}}}$$



independent from τ_I!

$$\Rightarrow t_{TEST} = t_{APP} e^{-\frac{E_A}{k}\left(\frac{1}{T_{APP}} - \frac{1}{T_{TEST}}\right)}$$

time-dependent effects

$t_{APP} = 10$ years, $\quad T_{APP} = 25$ °C

$$t_{TEST} = t_{APP} e^{-\frac{E_A}{k}\left(\frac{1}{T_{APP}} - \frac{1}{T_{TEST}}\right)}$$

time-dependent effects

$t_{APP} = 10$ years, $\quad T_{APP} = 25\ °C$

$$t_{TEST} = t_{APP}\, e^{-\frac{E_A}{k}\left(\frac{1}{T_{APP}} - \frac{1}{T_{TEST}}\right)}$$

t_{TEST}	$T_{TEST} = 100\ °C$	$T_{TEST} = 60\ °C$	$T_{TEST} = 30\ °C$	$T_{TEST} = 25\ °C$	$T_{TEST} = 0\ °C$	$T_{TEST} = -20\ °C$	$T_{TEST} = -30\ °C$
$E_A = 0.20$ eV	2.09 Y	4.41 Y	8.8 Y	10 Y	20.39 Y	39.9 Y	58.17 Y
$E_A = 0.40$ eV	159.7 d	1.95 Y	7.74 Y	10 Y	41.58 Y	1.59 C	3.38 C
$E_A = 0.60$ eV	33.41 d	313.9 d	6.8 Y	10 Y	84.77 Y	6.35 C	1.97 M
$E_A = 0.80$ eV	6.99 d	138.55 d	5.98 Y	10 Y	1.73 C	2.53 M	11.45 M
$E_A = 1.00$ eV	1.46 d	61.16 d	5.26 Y	10 Y	3.52 C	10.11 M	66.61 M

d = days, Y = years, C = centuries, M = millennia

time-dependent effects

E_A depends on the type of process

e.g.:

- removal of TID-induced positive charge in the oxide: $E_A \approx 0.4\ \mathrm{eV}$ [1]
- build-up of TID-induced charge at Si/SiO_2 the interface: $E_A \approx 0.8\ \mathrm{eV}$ [2, 3]

[1] Schwank, J. R., et al. "Physical mechanisms contributing to device" rebound"." IEEE Transactions on Nuclear Science 31.6 (1984): 1434-1438.
[2] Winokur, P. S., et al. "Field- and Time-Dependent Radiation Effects at the SiO2/Si Interface of Hardened MOS Capacitors," in IEEE Transactions on Nuclear Science, vol. 24, no. 6, pp. 2113-2118, Dec. 1977
[3] Saks, N. S., et al. "Time dependence of interface trap formation in MOSFETs following pulsed irradiation," in IEEE Transactions on Nuclear Science, vol. 35, no. 6, pp. 1168-1177, Dec. 198

time-dependent effects

E_A depends on the type of process

always* beneficial!

e.g.:

- removal of TID-induced positive charge in the oxide: $E_A \approx 0.4$ eV [1]
- build-up of TID-induced charge at Si/SiO_2 the interface: $E_A \approx 0.8$ eV [2, 3]

*almost

[1] Schwank, J. R., et al. "Physical mechanisms contributing to device" rebound"." IEEE Transactions on Nuclear Science 31.6 (1984): 1434-1438.
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time-dependent effects

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e.g.:

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can be detrimental!

[1] Schwank, J. R., et al. "Physical mechanisms contributing to device" rebound"." IEEE Transactions on Nuclear Science 31.6 (1984): 1434-1438.
[2] Winokur, P. S., et al. "Field- and Time-Dependent Radiation Effects at the SiO2/Si Interface of Hardened MOS Capacitors," in IEEE Transactions on Nuclear Science, vol. 24, no. 6, pp. 2113-2118, Dec. 1977
[3] Saks, N. S., et al. "Time dependence of interface trap formation in MOSFETs following pulsed irradiation," in IEEE Transactions on Nuclear Science, vol. 35, no. 6, pp. 1168-1177, Dec. 198

time-dependent effects

$t_{APP} = 10 \text{ years}, \quad T_{APP} = 25\ °\text{C}$

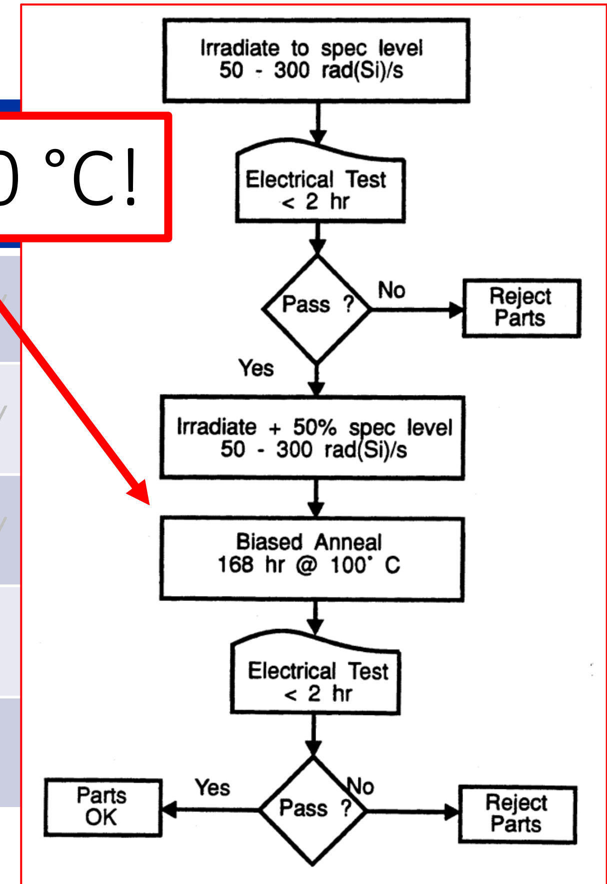
$$t_{TEST} = t_{APP}\, e^{-\frac{E_A}{k}\left(\frac{1}{T_{APP}} - \frac{1}{T_{TEST}}\right)}$$

t_{TEST}	$T_{TEST} = 100\ °\text{C}$	$T_{TEST} = 60\ °\text{C}$	$T_{TEST} = 30\ °\text{C}$		
$E_A = 0.20$ eV	2.09 Y			10 Y	20.39 Y
$E_A = 0.40$ eV	159.7			10 Y	41.58 Y
$E_A = 0.60$ eV	33.41 d	313.9 d	6.8 Y	10 Y	84.77 Y
$E_A = 0.80$ eV	6.99 d	138.55 d	5.98 Y	10 Y	1.73 C
$E_A = 1.00$ eV	1.46 d	61.16 d	5.26 Y	10 Y	3.52 C

d = days, Y = years, C = centuries, M = millennia

7 days at 100°C
=
10 years at 25°C

1 week at 100 °C!



Fleetwood, D. M., and H. A. Eisen. "Total-dose radiation hardness assurance." IEEE Transactions on Nuclear Science 50.3 (2003): 552-564.

time-dependent effects

How to extract E_A?

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$$\frac{Y}{Y_0} = e^{-\frac{t}{\tau_I}e^{-\frac{E_A}{kT}}}$$

time-dependent effects

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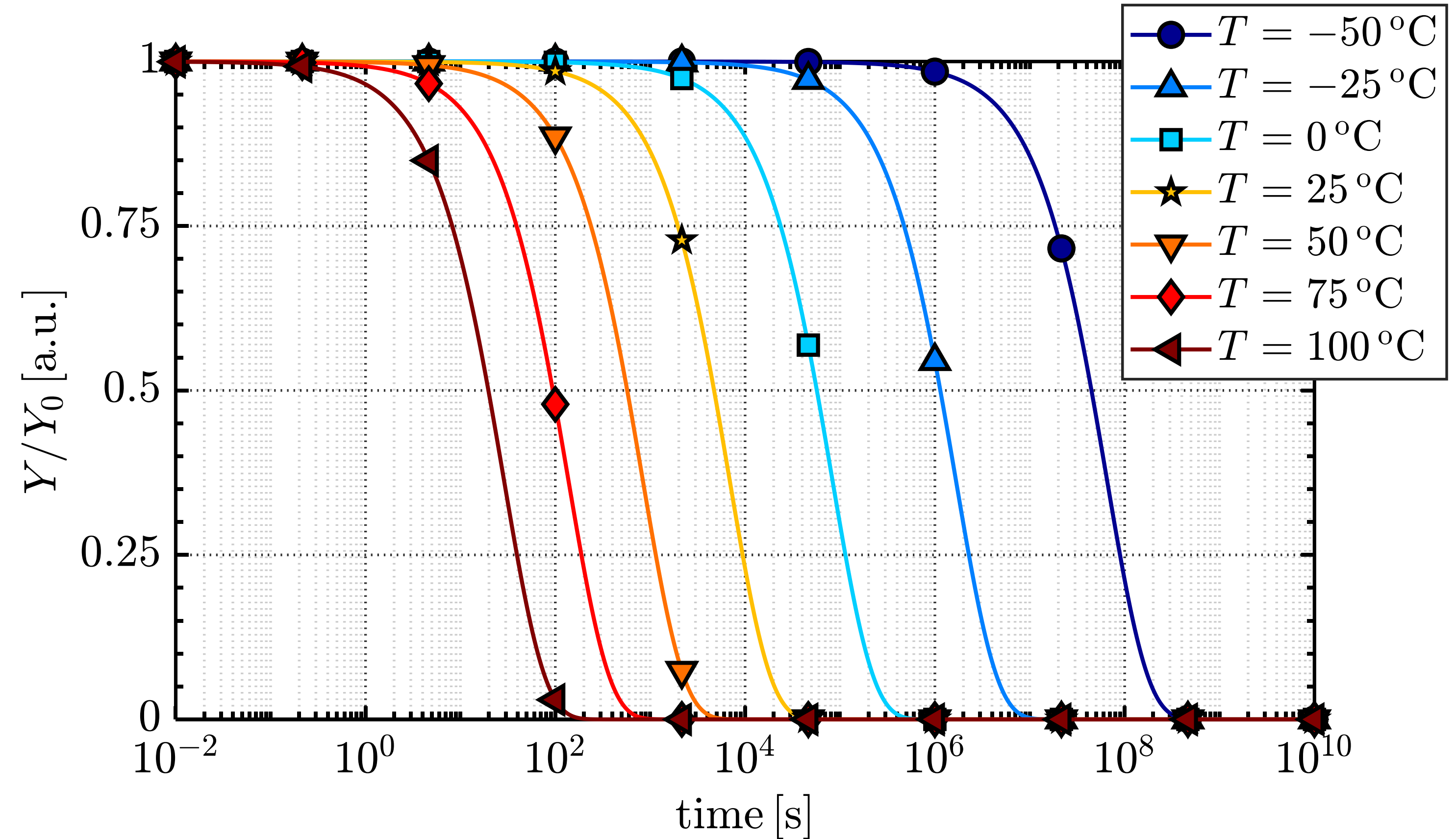
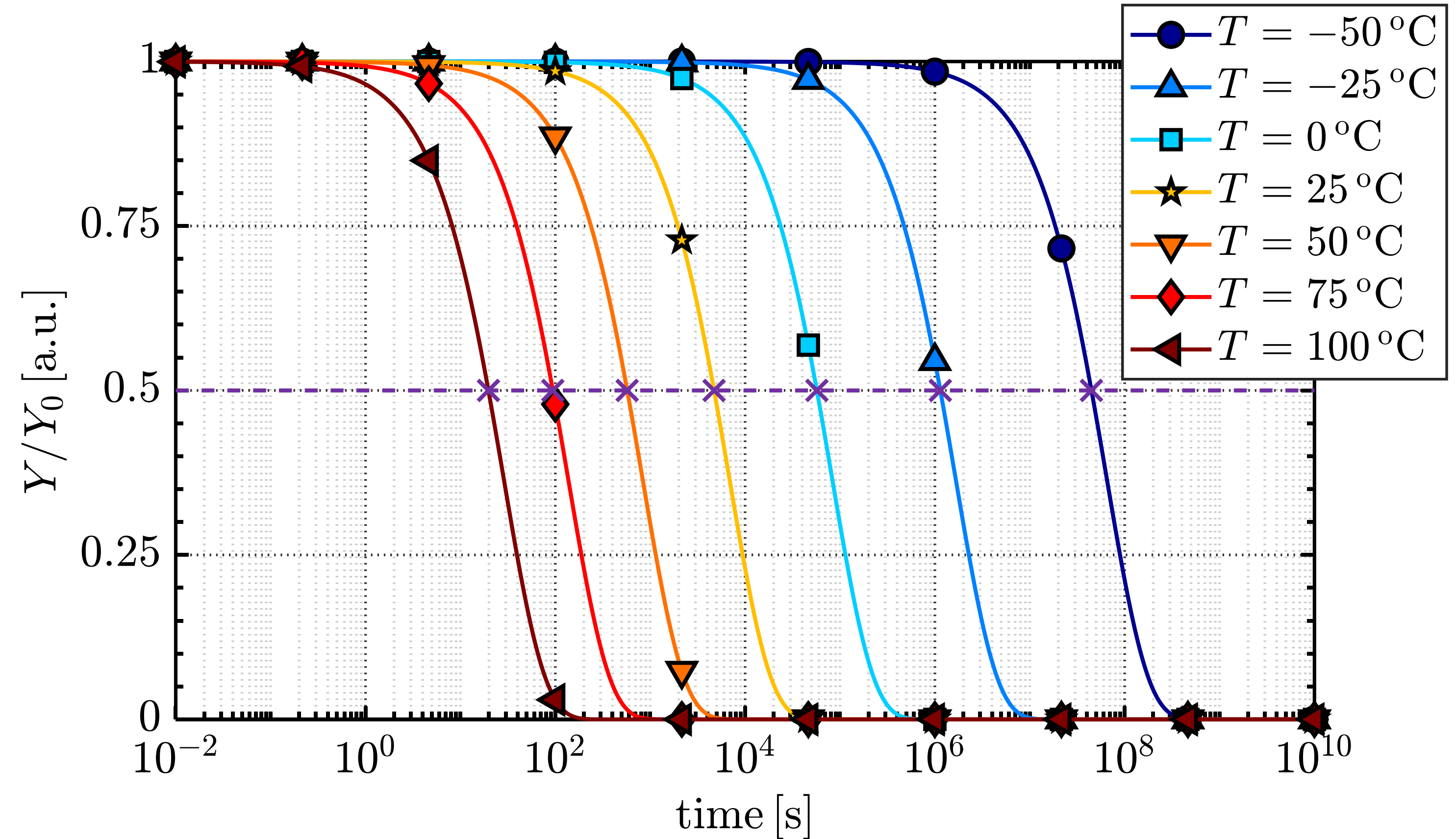


time-dependent effects

How to extract E_A?

$$\frac{Y_X}{Y_0} = e^{-\frac{t_X}{\tau_I}e^{-\frac{E_A}{kT}}} = 0.5$$



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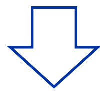
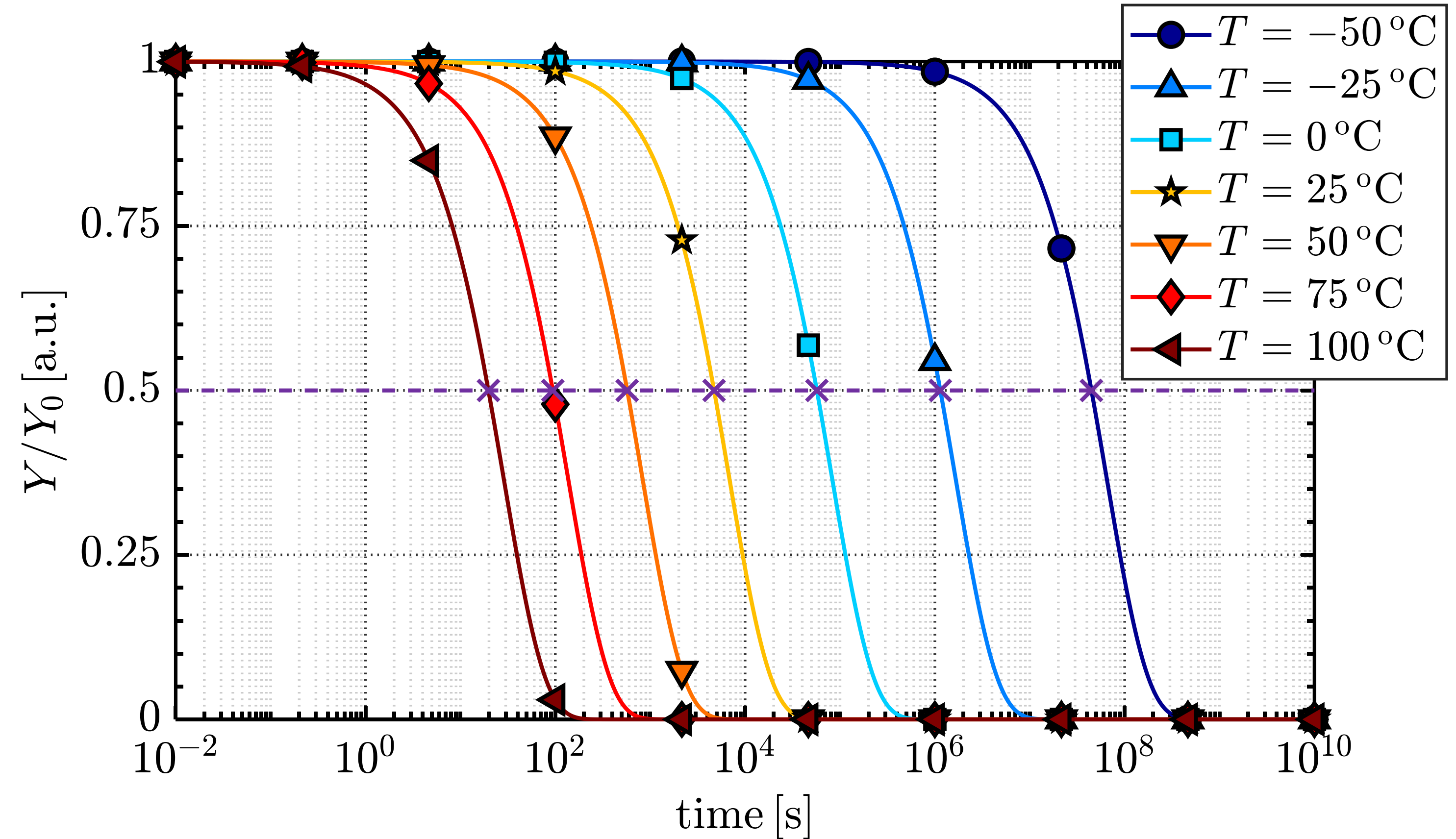


$$\frac{-\ln(0.5)}{t_X} = \frac{1}{\tau_I} e^{-\frac{E_A}{kT}}$$



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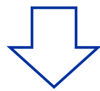
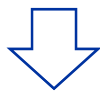
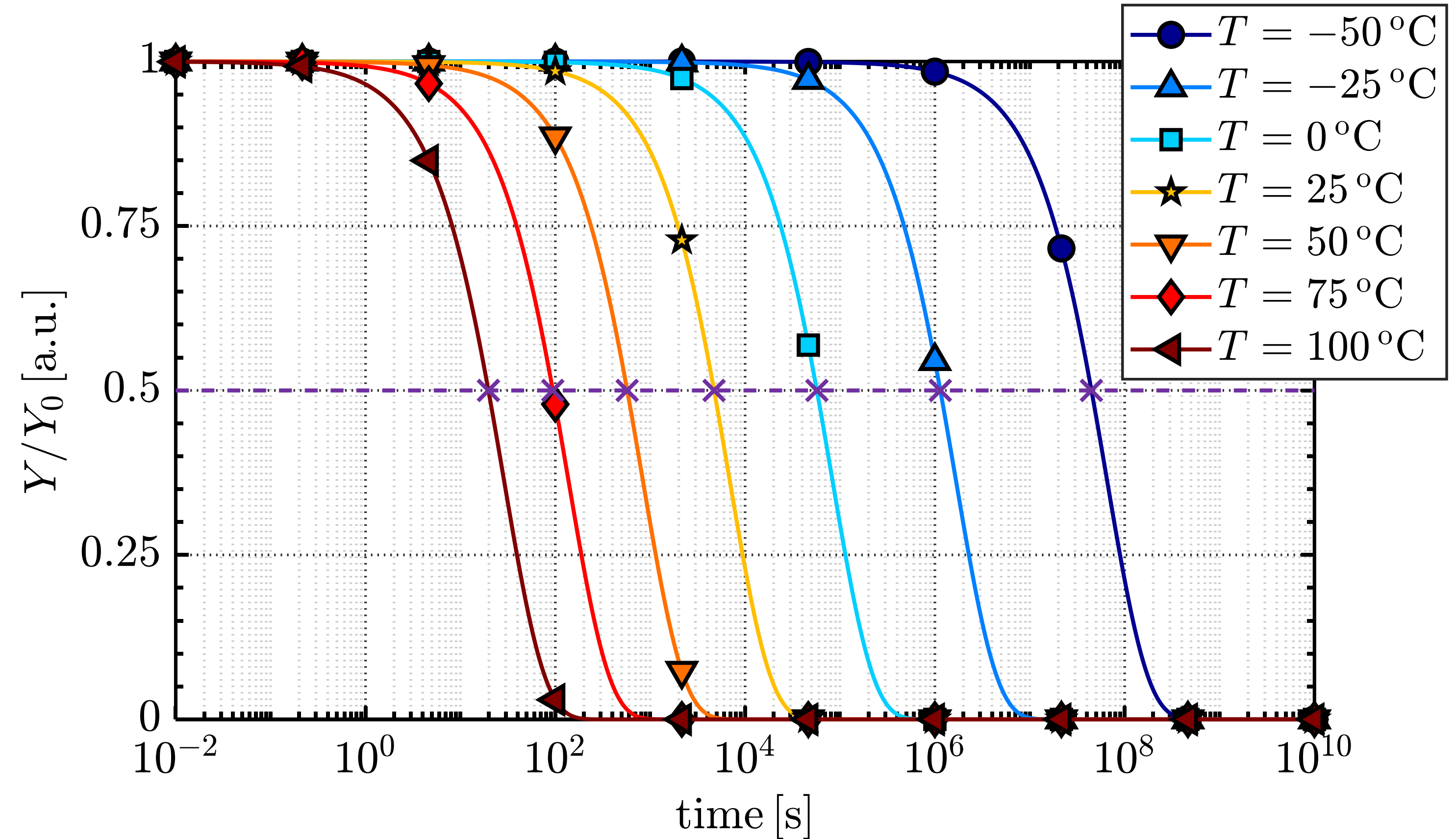


$$\frac{-\ln(0.5)}{t_X} = \frac{1}{\tau_I} e^{-\frac{E_A}{kT}}$$



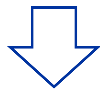
$$\ln\left(\frac{-\ln(0.5)}{t_X}\right) = \ln\left(\frac{1}{\tau_I}\right) - \frac{E_A}{kT}$$



time-dependent effects

How to extract E_A?

$$\frac{Y_X}{Y_0} = e^{-\frac{t_X}{\tau_I} e^{-\frac{E_A}{kT}}} = 0.5$$



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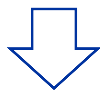
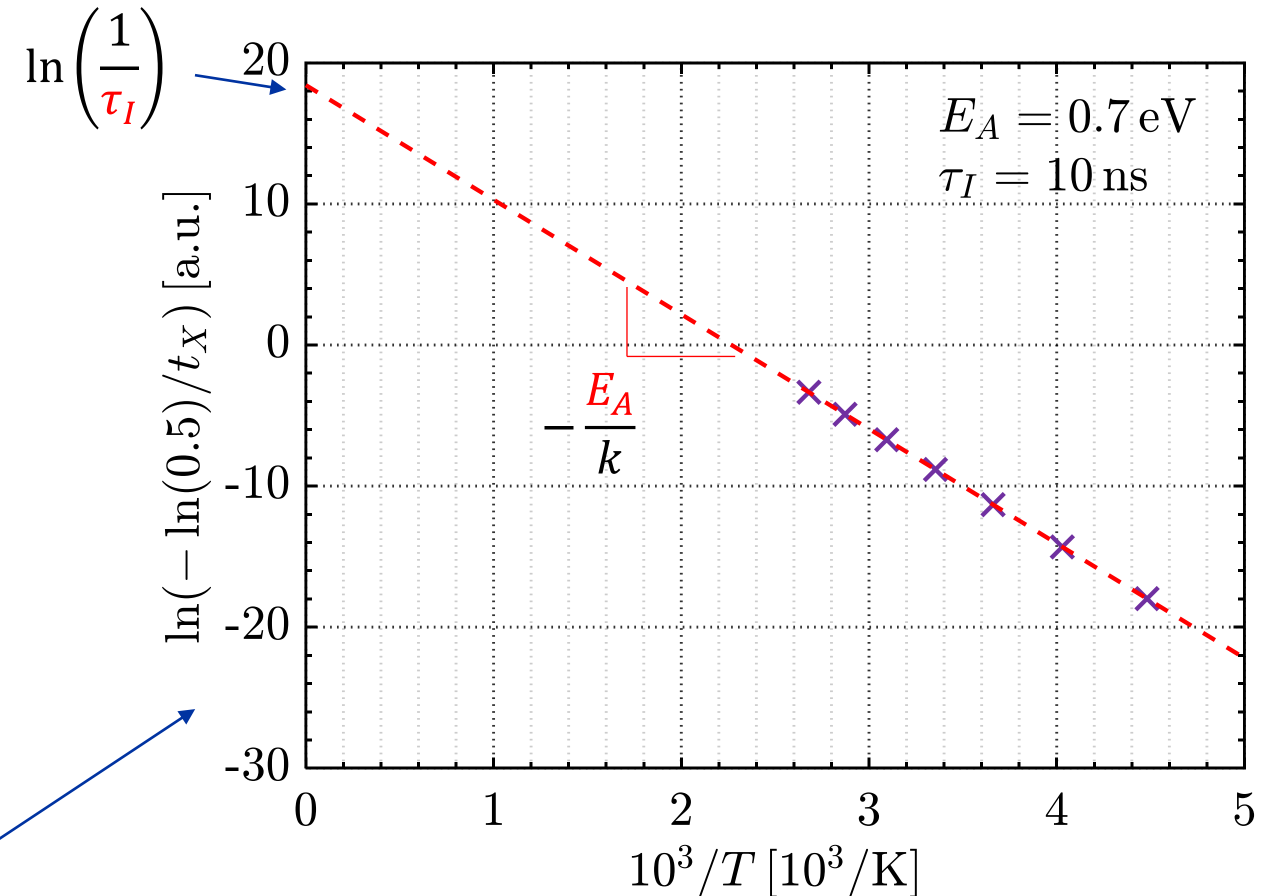


$$\ln\left(\frac{-\ln(0.5)}{t_X}\right) = \ln\left(\frac{1}{\tau_I}\right) - \frac{E_A}{kT}$$



SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET

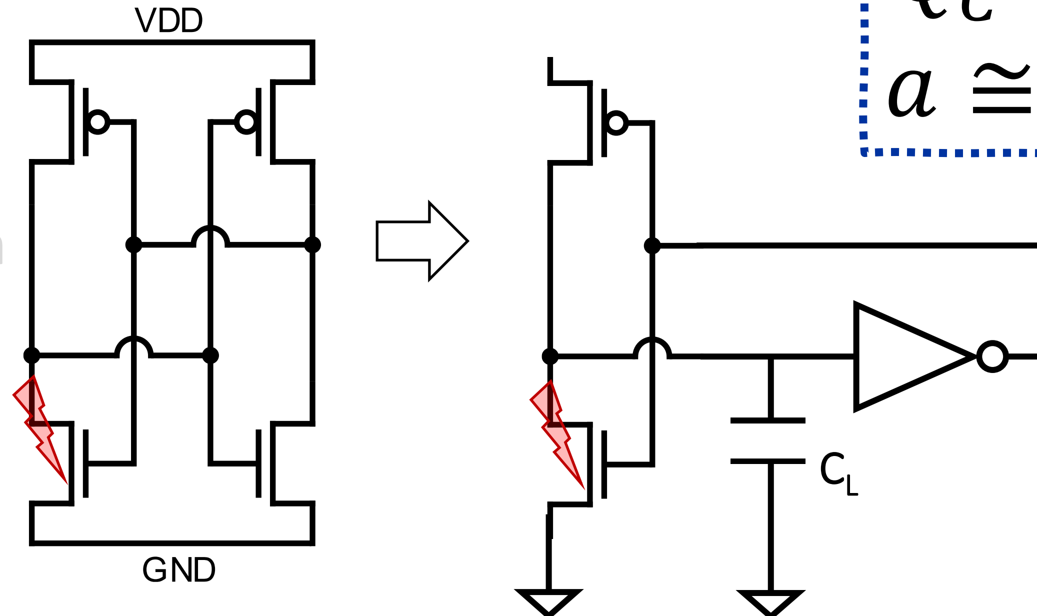
σ_∞ = saturated cross section

SEU relevant parameters (example: SRAM)

Q_C = critical charge → minimum charge needed to flip a bit

L_T = threshold LET

σ_∞ = saturated cross section



$$Q_C = aC_L V_{DD}$$
$$a \cong 2$$

D. Kobayashi, "Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance," in *IEEE TNS*, vol. 68, no. 2, pp. 124-148, Feb. 2021,

SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET

σ_∞ = saturated cross section

$$Q_C = aC_L V_{DD}$$
$$a \cong 2$$

smaller V_{DD} in advanced CMOS technologies

smaller C_L in advanced CMOS technologies ($C_L \simeq C_g + C_p$)

⟹ advanced technologies have a small Q_C
i.e., they need less charge to be upset

D. Kobayashi, "Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance," in *IEEE TNS*, vol. 68, no. 2, pp. 124-148, Feb. 2021,

SEU relevant parameters (example: SRAM)

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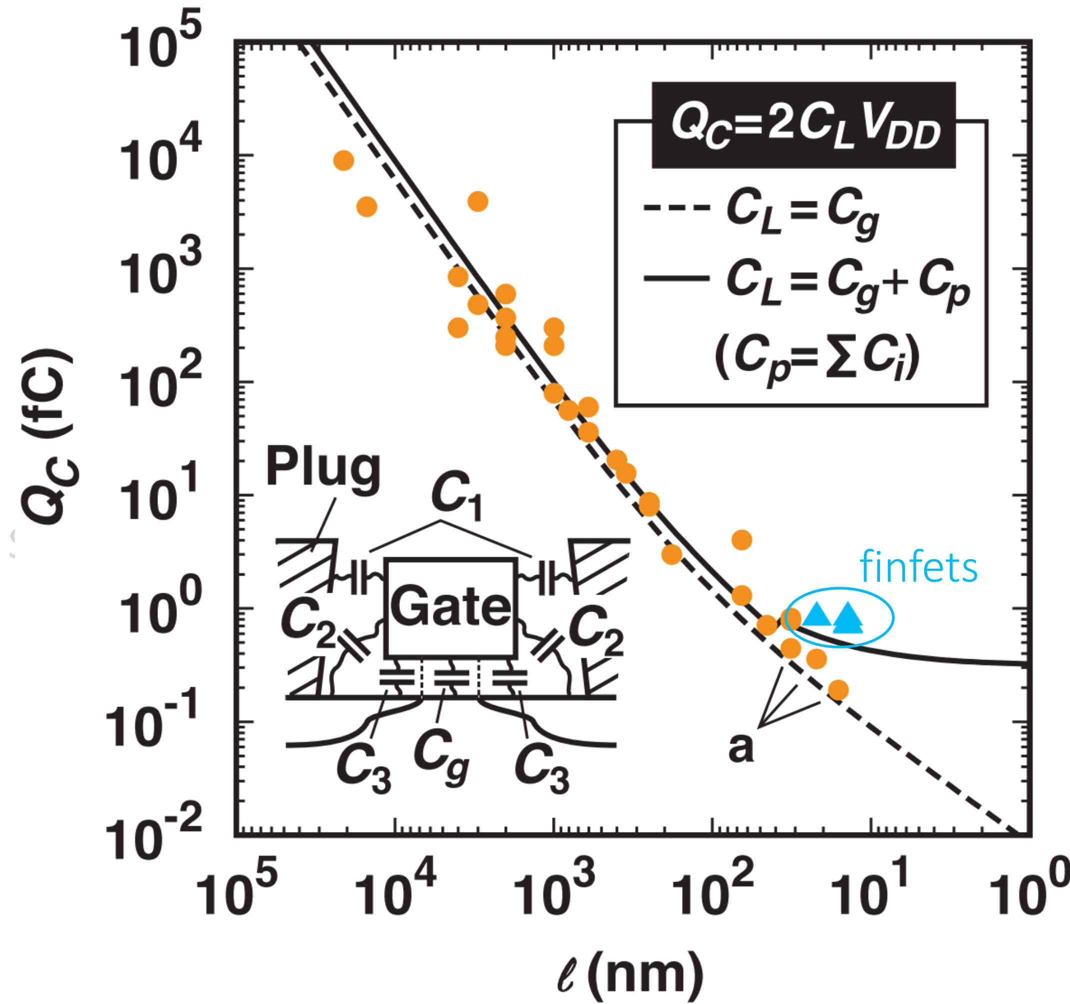


D. Kobayashi, "Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance," in *IEEE TNS*, vol. 68, no. 2, pp. 124-148, Feb. 2021,

SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET → linear energy transfer

σ_∞ = saturated cross section

the amount of energy that an ionizing particle transfers to the material traversed per unit distance

$$LET = \frac{dE}{dx}$$

often LET is divided by the density of the target material ρ.

While this quantity $\left(\frac{1}{\rho}\frac{dE}{dx}\right)$ should be called **mass stopping power**, the term LET is commonly used for both $\frac{dE}{dx}$ and $\frac{1}{\rho}\frac{dE}{dx}$

SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET

σ_∞ = saturated cross section

with LET is possible to calculate the amount of charge deposited in a material by a particle

example:

- particle with *LET* = 20.4 [MeV·cm^2/mg]
- in silicon (ρ_{Si} = 2.33 [g/cm^3], eh_{Si} = 3.6 [eV])

$$Q_d = q \times \frac{LET \times \rho_{Si}}{eh_{Si}} = 0.212 \left[\frac{\mathrm{pC}}{\mu\mathrm{m}}\right]$$

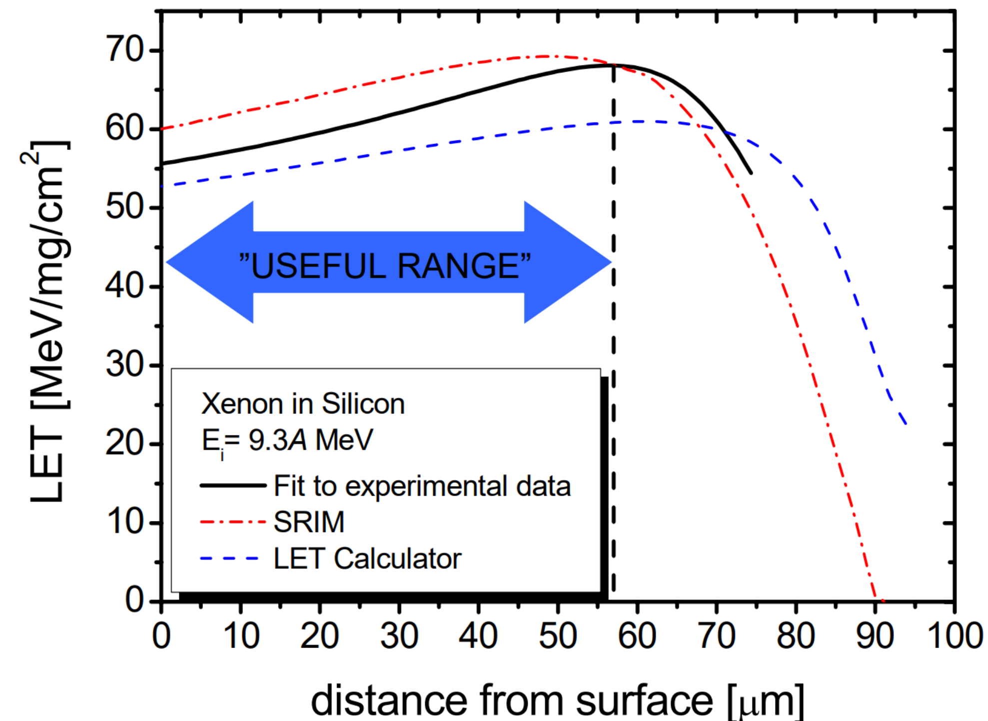
SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET

σ_∞ = saturated cross section

- LET changes during the passage in the material
- particles travelling in a material stop after some distance (range)
- in practice, average LET and average range are used



A. Javanainen, "Heavy ion LET in Silicon", https://escies.org/download/webDocumentFile?id=19698

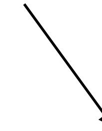
SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET

σ_∞ = saturated cross section

range decreases with LET!



M/Q	Ion	DUT energy [MeV]	Range [µm Si]	LET [MeV/(mg/cm²)]
3.25	$^{13}C^{4+}$	131	269.3	1.3
3.14	$^{22}Ne^{7+}$	238	202.0	3.3
3.37	$^{27}Al^{8+}$	250	131.2	5.7
3.27	$^{36}Ar^{11+}$	353	114.0	9.9
3.31	$^{53}Cr^{16+}$	505	105.5	16.1
3.22	$^{58}Ni^{18+}$	582	100.5	20.4
3.35	$^{84}Kr^{25+}$	769	94.2	32.4
3.32	$^{103}Rh^{31+}$	957	87.3	46.1
3.54	$^{124}Xe^{35+}$	995	73.1	62.5

https://uclouvain.be/en/research-institutes/irmp/heavy-ion-facility-hif.html

SEU relevant parameters (example: SRAM)

Q_C = critical charge

L_T = threshold LET

σ_∞ = saturated cross section

$$\text{cross section } \sigma = \frac{\text{number of SEU}}{\text{fluence} \times \text{number of bits in SRAM}} \quad [\text{cm}^2]$$

$$\text{fluence} = \text{number of particles}$$

SEU relevant parameters (example: SRAM)

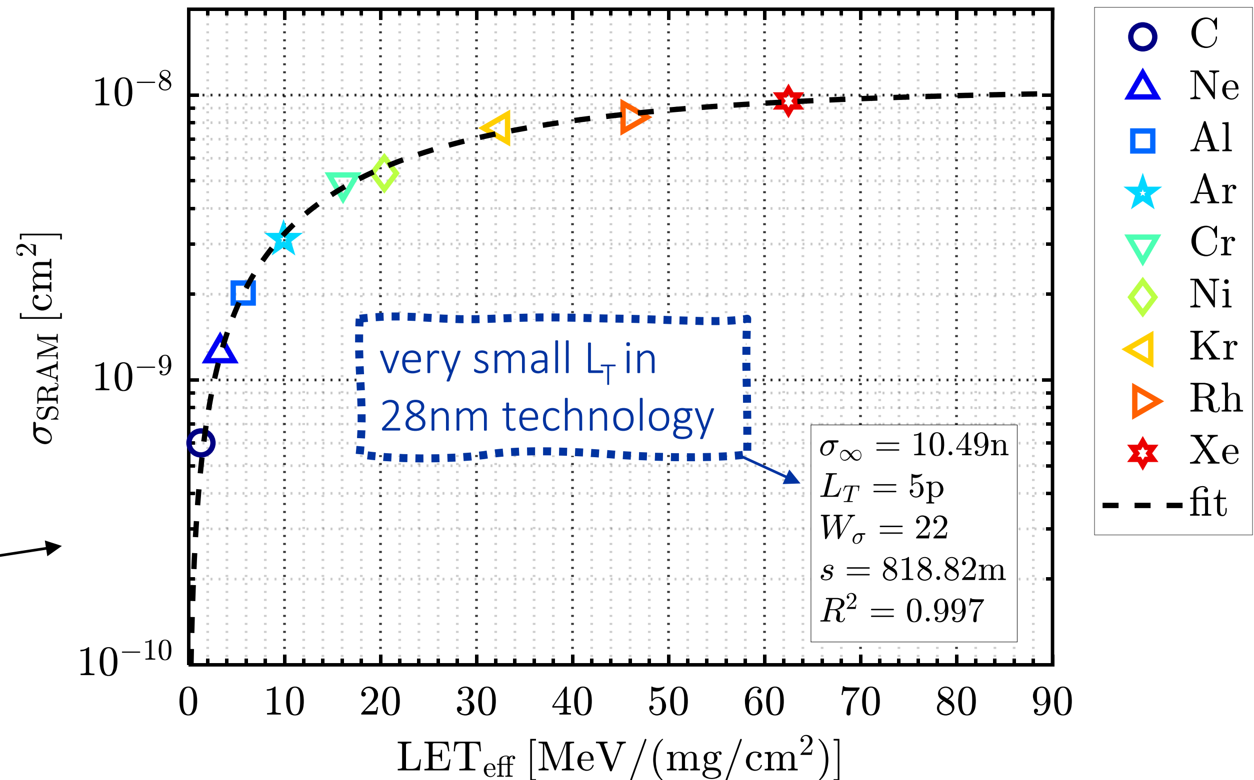
Weibull fit → $\sigma = \boldsymbol{\sigma_\infty}\left(1 - e^{-\left[\frac{LET - \boldsymbol{L_T}}{\boldsymbol{W_\sigma}}\right]^{\boldsymbol{s}}}\right)$

Q_C = critical charge

L_T = threshold LET

σ_∞ = saturated cross section

example in 28nm technology →



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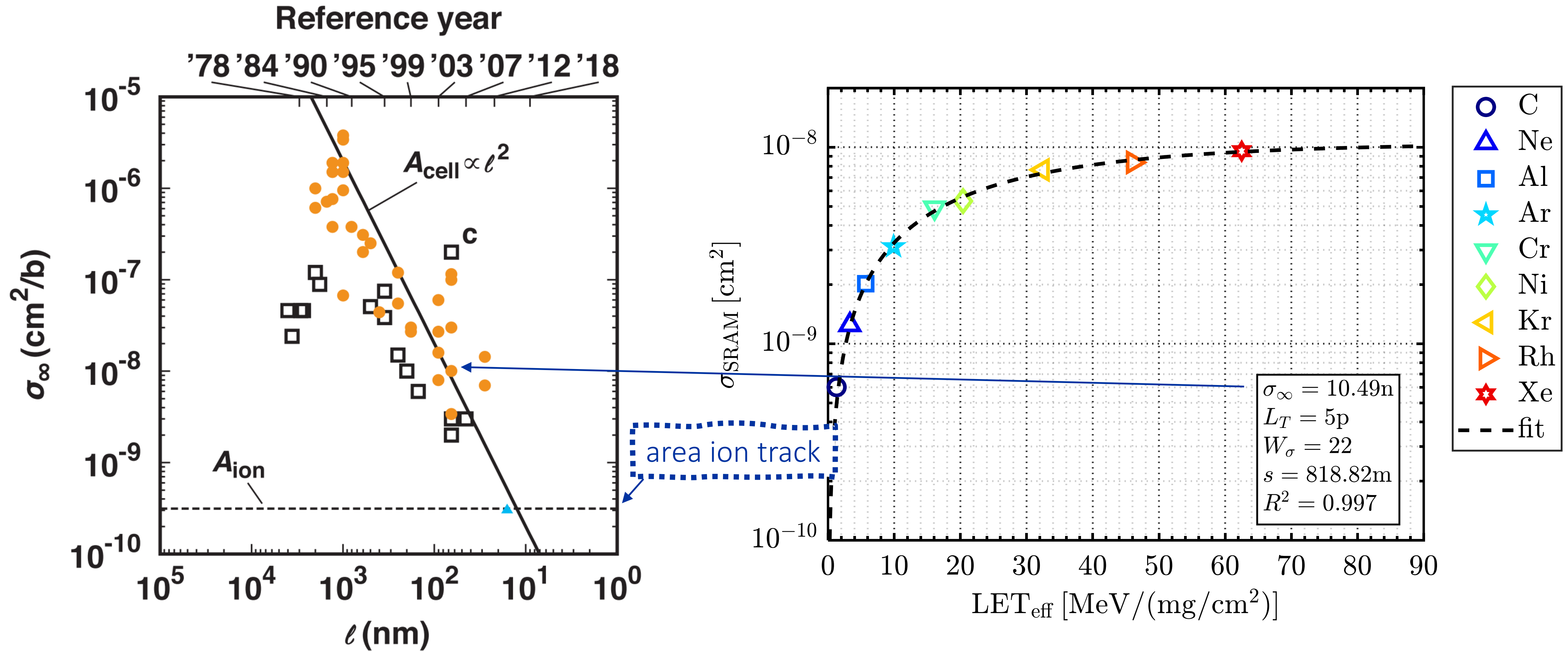
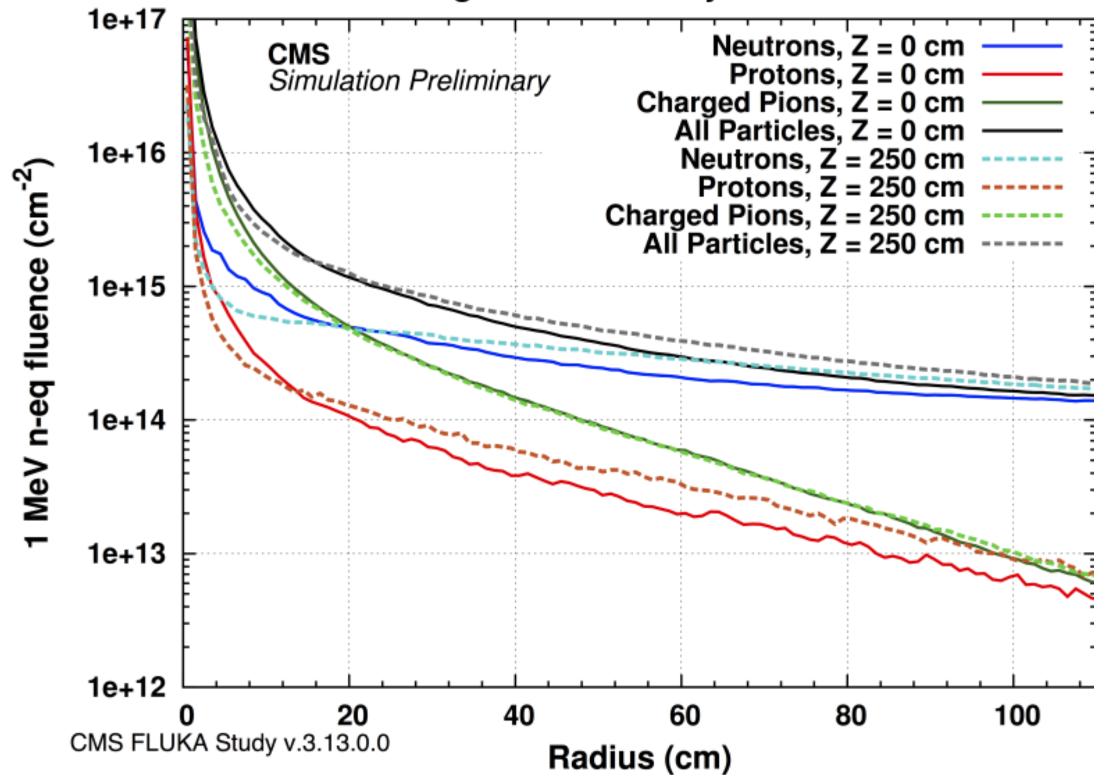
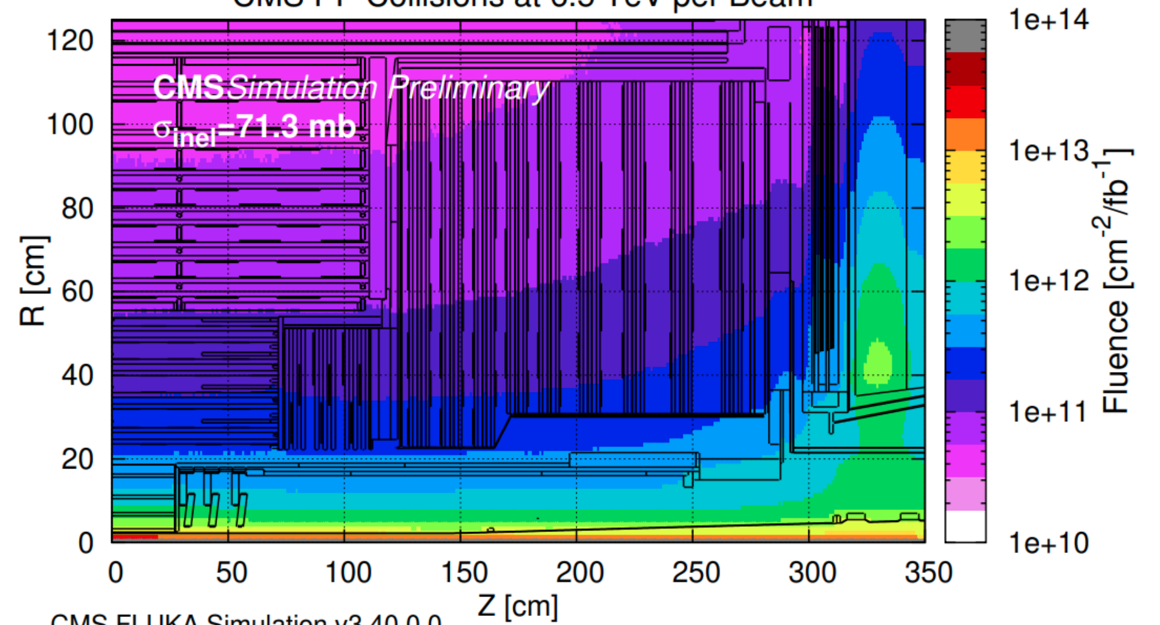
σ_∞ VS scaling



D. Kobayashi, "Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance," in *IEEE TNS*, vol. 68, no. 2, pp. 124-148, Feb. 2021,

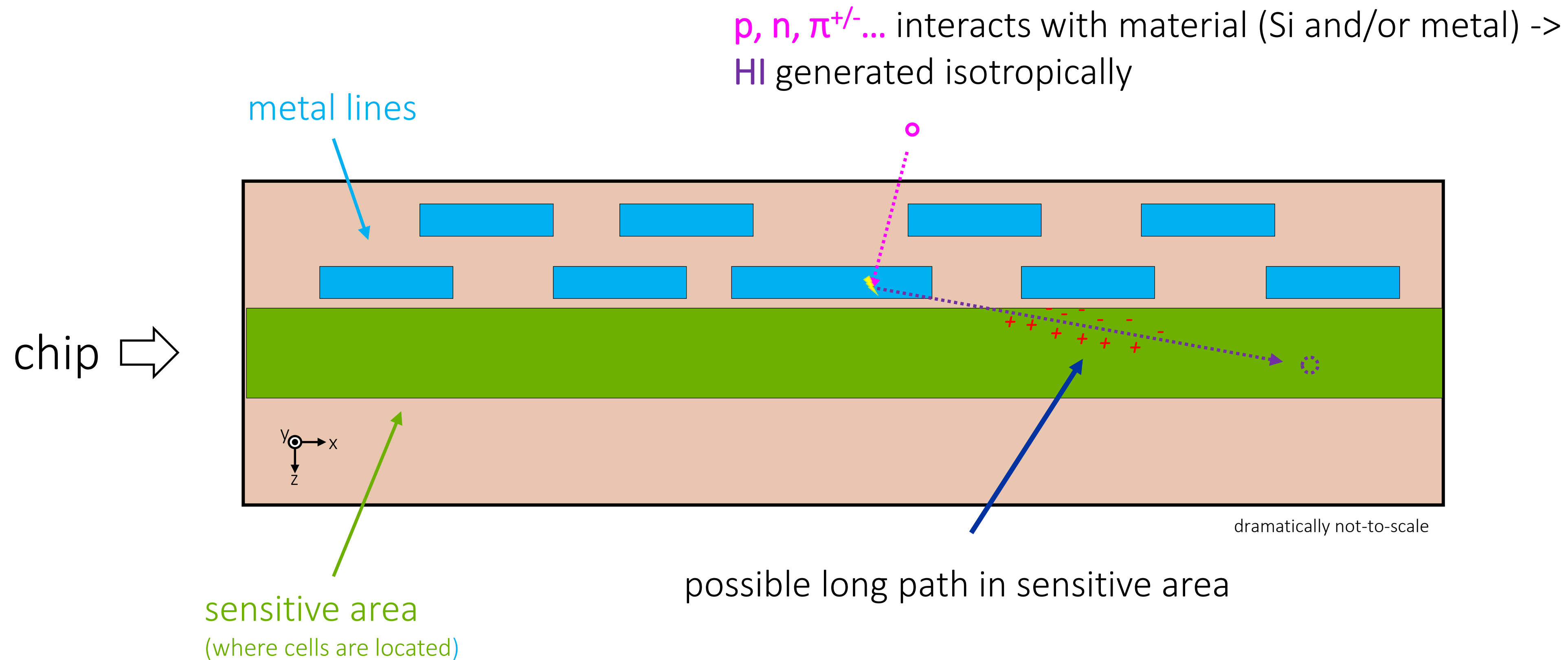
No heavy-ions in the real environment!





https://cds.cern.ch/record/2773266/files/10.23731_CYRM-2021-001.35.pdf

HI vs PROTONS



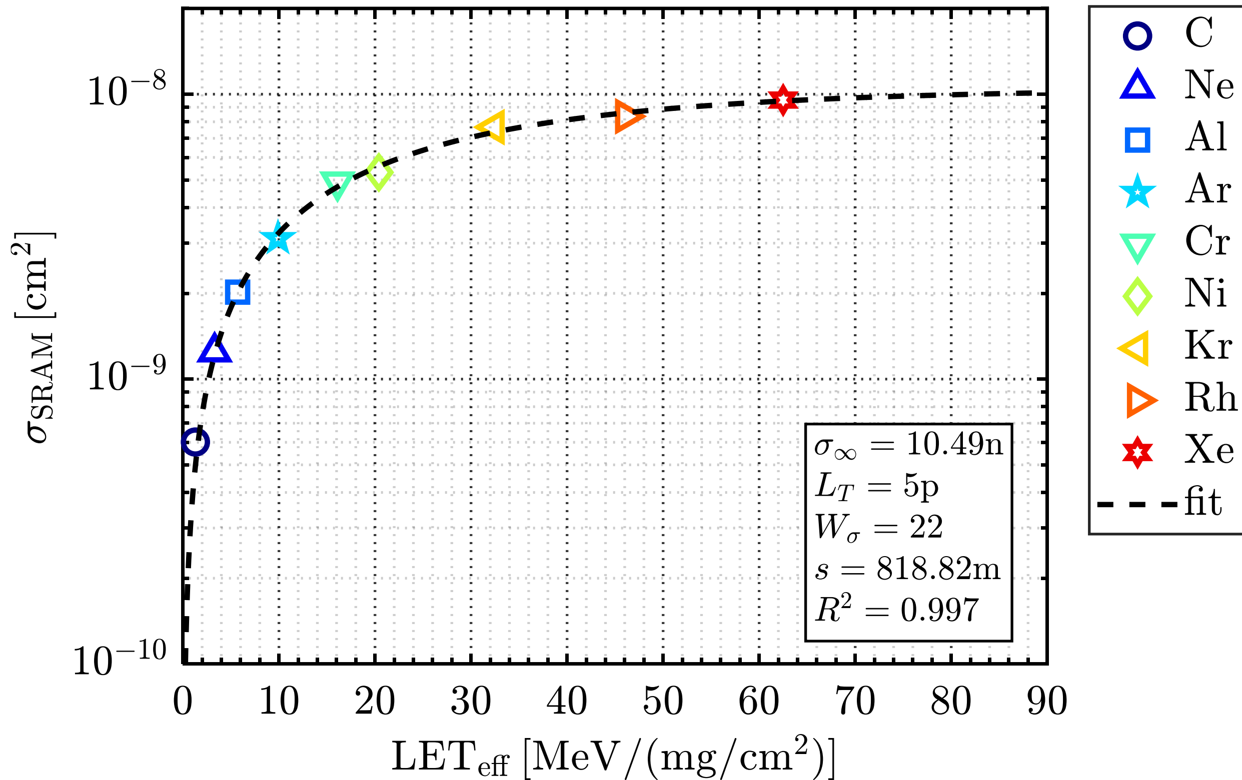
form HI to representative environment

↓

Weibull fit

↓

Huhtinen, M., and F. Faccio. "Computational method to estimate Single Event Upset rates in an accelerator environment." *NIMA* 450.1 (2000): 155-172.



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example:

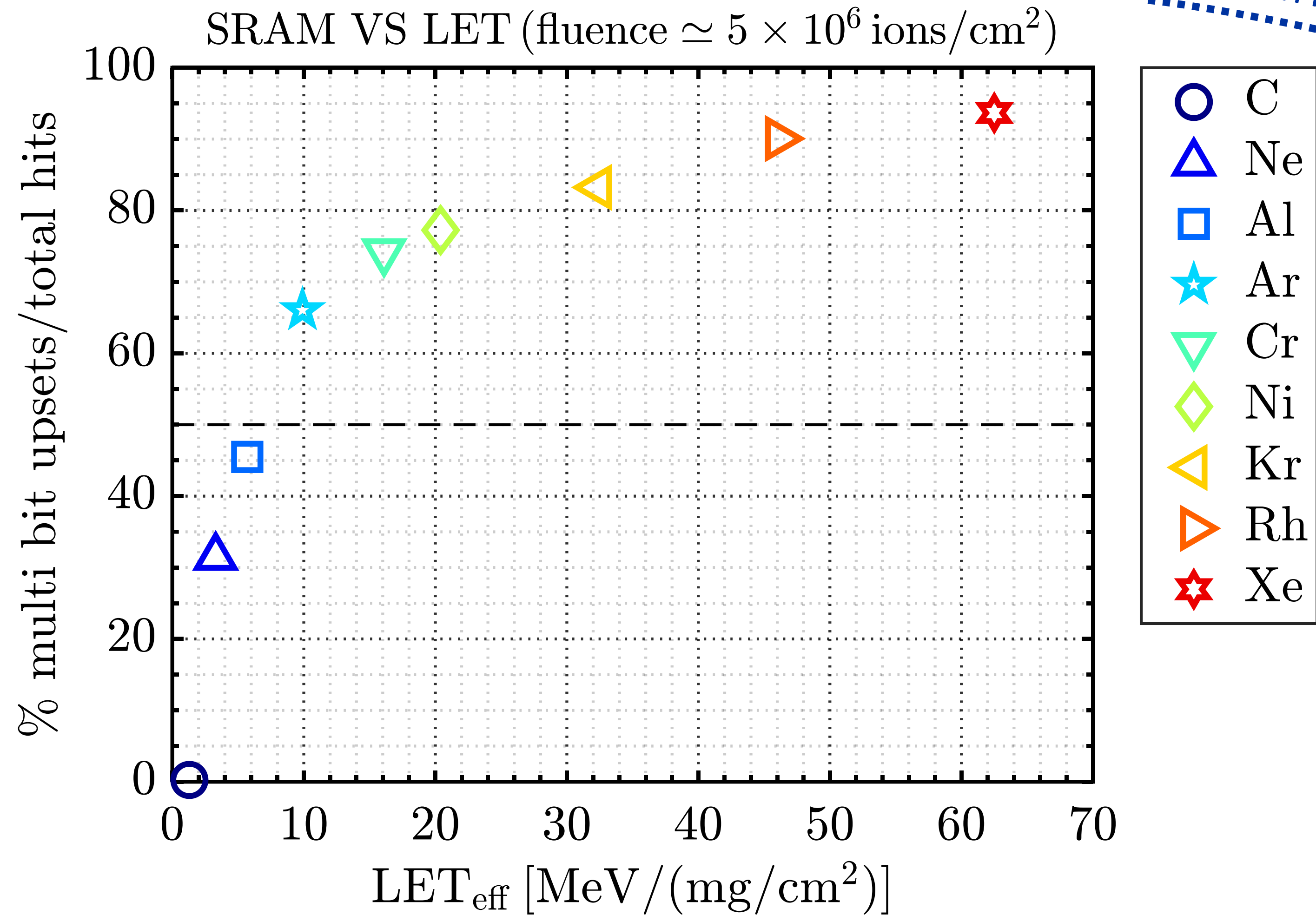
Caratelli, A., et al. "Low-power SEE hardening techniques and error rate evaluation in 65 nm readout ASICs". No. CMS-CR-2019-190. 2019.
https://cds.cern.ch/record/2724952/files/PoS(TWEPP2019)015.pdf

This analysis takes into consideration hadrons with energy higher than 20 MeV in the CMS tracker, for 13 TeV proton-proton collisions.

	SEU Counter	Stub data	L1 data (1 µs)	L1 data (12.6 µs)
MPA	$6.77 \cdot 10^{-11}\ \mathrm{cm}^2$	$7.92 \cdot 10^{-11}\ \mathrm{cm}^2$	$5.59 \cdot 10^{-11}\ \mathrm{cm}^2$	$9.55 \cdot 10^{-11}\ \mathrm{cm}^2$
SSA	-	$2.74 \cdot 10^{-11}\ \mathrm{cm}^2$	$0.82 \cdot 10^{-11}\ \mathrm{cm}^2$	$1.39 \cdot 10^{-11}\ \mathrm{cm}^2$

Table 1: MPA and SSA SEU cross section values for the CMS outer-tracker particle spectrum for 13 TeV proton-proton collisions.

in this example (28nm), MBUs dominate the response for LET > 10



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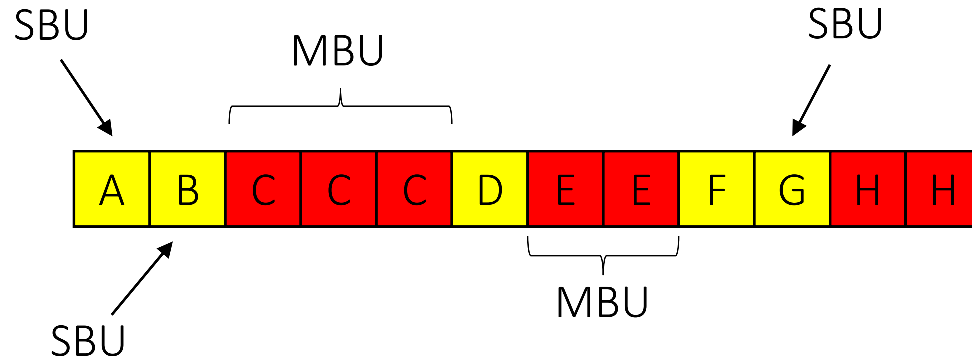
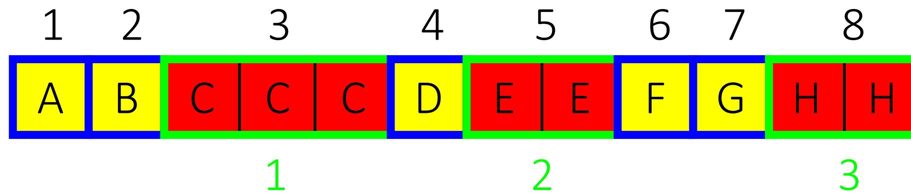
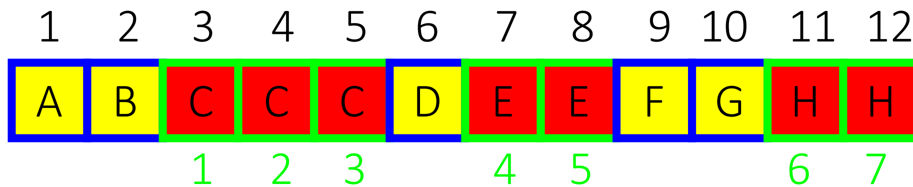




- 3 MBU/8 HITS = 37.5% : probability that a particle triggers an MBU (P_{MBU})



- 7 MBU/12 ERRORS = 58.3%: device sensitivity to MBU (S_{MBU})

giulio.borghello@cern.ch | CERN EP-ESE-ME