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GADEST 2026

Program and abstract booklet



21st International Conference on
Gettering and Defect Engineering
in Semiconductor Technology

San Servolo Island, Venice, Italy
27 September – 2 October 2026



**UNIVERSITÀ
DI PADOVA**

Dipartimento
di Fisica e Astronomia
"Galileo galilei" - DFA



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UNIVERSITÀ DI BOLOGNA

DEPARTMENT
OF PHYSICS AND ASTRONOMY
"AUGUSTO RIGHI"



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Preface

Welcome to the 21st International Conference on Gettering and Defect Engineering in Semiconductor Technology, held on the island of San Servolo, Venice, from 27 September to 2 October 2026.

GADEST was founded in 1985 by Hans Richter, at the Institute for Physics of Semiconductors of the Academy of Sciences of the former German Democratic Republic, as a meeting point for the semiconductor technology, device physics and defect physics communities, drawing on both academia and industry. It has been a biennial meeting ever since, interrupted only by the pandemic, and has traditionally been held at secluded venues, where participants stay together for the whole week and the discussion continues well past the end of the sessions. San Servolo follows that tradition closely: a small island in the Venetian lagoon, a short boat ride from San Marco, with the conference rooms, the residence and the dining hall all on the same island. Few places make it so easy to keep talking after a talk has ended.

This is the first edition without Hermann Grimmeiss and Vladimir Voronkov. Grimmeiss, who died in 2026, was a member of the Executive Committee and one of the pioneers of deep-level spectroscopy in semiconductors; his work on junction techniques for the characterization of deep centres remains a reference for this community. Voronkov died in 2025, shortly after attending the previous edition in Bad Schandau. His work at GlobalWafers-MEMC on point-defect behaviour during crystal growth gave the silicon industry the means to control vacancies and interstitials in the material it produces, and much of the work on silicon discussed at this conference builds on it. Two awards for young presenters, described below, have been established in his memory.

The continuity of the series rests with the Executive Committee, which oversees GADEST from one edition to the next, chooses its venues and chairs, and guides its scientific direction. It is largely thanks to its members that the scope of the conference has held steady while the technology around it has changed.

One question has held GADEST together for four decades: how defects govern the behaviour of semiconductor materials and devices, and how they can be suppressed, engineered, or put to work. The programme of this edition runs from the identification of point defects and their interaction with impurities to the processing of complete device structures, across silicon, silicon carbide, group-IV alloys, nitrides and halide perovskites. Microelectronics, power electronics and photovoltaics are joined by a growing body of work in which the defect is no longer only a limitation but a resource, as in single-photon emitters and spin qubits hosted by the crystal itself. The conference opens with a plenary lecture and continues with sixteen invited talks, fifty-two contributed oral presentations and sixty-two posters, from more than 140 submitted abstracts. The invited talks span the whole range, from atomic-scale dopant control to metrology and reliability in production environments.

A selection of the work presented here is collected in a Special Issue of *Materials Science in Semiconductor Processing* (Elsevier), dedicated to this edition, with the papers appearing around the time of the conference.

The two poster sessions, on Monday and Tuesday evening, take place in the dining hall itself and run alongside dinner. This is deliberate. In a meeting of this size the posters are where most of the real exchange happens, and giving them the evening, with food and without a competing parallel session, is the surest way to protect it.

On Wednesday the sessions end in mid-morning and the rest of the day is given to the social excursion, a boat trip through the lagoon, followed by the conference dinner. The break in the middle

of the week is part of the format rather than a concession to tourism: it is the point at which conversations begun on Sunday tend to turn into collaborations.

On the final day the conference presents the two Voronkov awards, each of €500, thanks to the generous support of GlobalWafers-MEMC Electronic Materials. The Young Student Award goes to the best student presentation, the Young Researcher Award to the best presentation by a researcher under the age of forty. The ceremony includes a memorial presentation by Robert Falster, member of the Executive Committee and for many years Voronkov's colleague and friend, on what Voronkov's work has meant for this community and for semiconductor science.

We thank the members of the Executive Committee and of the International Programme Committee for the review of the abstracts and for the shaping of the programme, our sponsors for their support, and the local organizing team, whose work over the past months made this week possible.

Enrico Napolitani, Università degli Studi di Padova, Italy
Michele Perego, IMM-CNR, Unit of Agrate Brianza, Italy
Daniela Cavalcoli, Università degli Studi di Bologna, Italy
Simona Binetti, Università degli Studi di Milano-Bicocca, Italy
Antonino La Magna, IMM-CNR, Catania, Italy

Conference Chairs

Committees

Conference Chairs

Enrico Napolitani — Università degli Studi di Padova, Italy
Michele Perego — IMM-CNR, Unit of Agrate Brianza, Italy
Daniela Cavalcoti — Università degli Studi di Bologna, Italy
Simona Binetti — Università degli Studi di Milano-Bicocca, Italy
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Conference Programme

Sunday, 27 September, 2026				Page
14:00-15:45	<i>Registration and Welcome coffee</i>			
15:45-16:15	<i>Opening — Welcome Speech</i>			
16:15-17:00	Plenary Session			
16:15-17:00	Su-PL1	Steven Schofield	Dopants at the Atomic Limit in Silicon and Germanium	1
17:00-18:20	Defect Engineering and Metrology			
17:00-17:40	Su-I1	Lennaert Wouters	Scanning Spreading Resistance Microscopy as a Key Nano-Metrology Technique for Semiconductor Technology Scaling – History and Future	2
17:40-18:20	Su-I2	Lachlan Black	Defect mitigation strategies for next-generation, high-efficiency silicon-based solar cells	3
19:00-22:00	<i>Dinner</i>			

Monday, 28 September, 2026				Page
08:30-10:10	Group IV: Hyperdoping and Defects			
08:30-09:10	Mo-I1	Francesca Chiodi	Tuning superconductivity in ultra-doped Si and SiGe epilayers with Nanosecond Laser Doping	4
09:10-09:30	Mo-O1	Enrico Di Russo	Combination of layer deposition and pulsed UV laser annealing for thin GeSn:Sb layers hyperdoping	5
09:30-09:50	Mo-O2	Afonso de Cerdeira Oliveira	Defect characterization in monolithic integrated Ge-on-Si layers grown by Low-Energy Plasma-Enhanced Chemical Vapour Deposition	7
09:50-10:10	Mo-O3	Francesco Sgarbossa	Hyperdoped and Highly Strained Ge:Sb layers by Pulsed Laser Melting for Next-Generation Germanium Crystalline Gamma-Ray Sources	10
10:10-10:40	<i>Coffee break</i>			
10:40-12:40	Group IV for Photonics			
10:40-11:20	Mo-I2	Yonder Berencén	All-silicon telecom photodetectors via ion-beam engineering for photonic integration	12
11:20-11:40	Mo-O4	Davide Impelluso	SiGe Forward-Reverse linearly graded buffers for mid-infrared photonics	13
11:40-12:00	Mo-O5	Guo-En Chang	GeSn Waveguide Photodetectors for Next-Generation Silicon Photonics	14
12:00-12:20	Mo-O6	Giulia Maria Spataro	Emergent optical and transport phenomena in hyperdoped n-type Ge	16
12:20-12:40	Mo-O7	Mariia Terletskaia	Controlled surface cleaning of MACE-nanotextured Ge for cost-efficient high-performance UV-SWIR photodetection	18
12:40-13:40	<i>Lunch break</i>			
13:40-15:40	Alternative Semiconductor Devices			
13:40-14:20	Mo-I3	Bruna Cardoso Paz	QSOI®: a platform for large scale quantum integrated circuits	20
14:20-14:40	Mo-O8	Maximilian Stipkovich	Cryogenic SiGe Transistors based on Modulation Acceptor Doping	21
14:40-15:00	Mo-O9	Daniele Nazzari	Non-volatile reconfigurable Al-Si transistors via ferroelectrically modulated Schottky barriers	23
15:00-15:20	Mo-O10	John Murphy	Photoexcited muon spin spectroscopy for studying bulk, surface, and temperature-dependent carrier recombination in silicon wafers and solar cells	25
15:20-15:40	Mo-O11	Yu-Chen Chang	Engineering UltrasMOOTH Sub-Nanometer Interlayers via Chemical Modulation for Suppression of Interface Defects in Advanced Si/HfO ₂ MOS Technology	27
15:40-16:10	<i>Coffee break</i>			
16:10-17:50	Defects for Advanced Semiconductor Applications			

Monday, 28 September, 2026				Page
16:10-16:50	Mo-I4	Felipe Murphy-Armando	From Defect-Induced Variability to Deterministic Control: Strain Gradients as a New Paradigm for Valley Engineering	29
16:50-17:10	Mo-O12	Andrea Besana	Low Temperature Epitaxy of Planar Hexagonal Germanium	31
17:10-17:30	Mo-O13	Andrea Pulici	Beyond Bulk: Interface-Driven Dopant Physics in Ultrathin Silicon-on-Insulator	33
17:30-17:50	Mo-O14	Kaynat Alvi	W-Center Defects in Crystalline Silicon: Electronic Structure and Optical Signatures	35
17:50-18:40	<i>Industrial session</i>			
19:00-22:00	<i>Dinner and Poster Session 1</i>			

Poster Session 1 - Monday 28 September, 19:00-22:00			Page
Mo-P1	Oleg Olikh	Admittance spectroscopy of organic-silicon heterojunction structures fabricated with ultrasound assistance	37
Mo-P2	Takuya Kusunoki	Comparative study of void defect annihilation in Si (100) and Si (110) wafers during high-temperature rapid thermal processing	39
Mo-P3	Shuai Yuan	Controlled Copper Precipitation for Rapid Point Defect Characterization in Near-Perfect Czochralski Silicon	41
Mo-P4	Iori Takeda	DFT Analysis of Gettering in Si Wafers for CMOS Image Sensors	42
Mo-P5	Shengqiang Zhou	Doping Engineering of Double-SOI Structures for Two-Channel Tunneling Transistors	44
Mo-P6	Oskari Leiviskä	Electric Field Distribution in Black Silicon Needles Under Reverse Bias: A TCAD Simulation Study	45
Mo-P7	Kaynat Alvi	Electrical and Optical Properties of Defect-Enhanced SiGe Heterostructures	47
Mo-P8	Henriette Tetzner	Electrical Properties of Dislocation-Related Defects in Ge/Si Virtual Substrates	48
Mo-P9	Alessandro Puddu	Electrically detected magnetic resonance of telecom-wavelength G and C centers in silicon	50
Mo-P10	Yilun Wang	Elimination of slip lines induced by the pins in rapid thermal processing for Czochralski silicon wafers	51
Mo-P12	Roberta Farina	Engineering Nanostructured Electrodes on Screen-Printed Carbon for Real-Time Monitoring of Nitrogen-Based Water Pollutants	53
Mo-P13	Matteo Pannocchia	Epi stacking fault defects in highly doped phosphorus 300 mm crystals	54
Mo-P14	Ignazio Vacante	Evaluation of impurity effects in magic-angle twisted bilayer graphene by machine learning interatomic potentials	56
Mo-P15	Dawid Kot	Experimental and simulated investigation of nitrogen shallow donors in Czochralski silicon wafers doped with nitrogen	57
Mo-P16	Mette Schouten	Experimental observation and analysis of gliding I3 basal stacking faults in hexagonal germanium	59
Mo-P17	Charlotte Weiss	Ge-on-Si Substrates with Porous Silicon buffer as Compliant Layer	61
Mo-P18	Matthias Müller	Impact of ion charge transport on perovskite solar cells simulated by TCAD Sentaurus	63
Mo-P19	Jinge Wang	Impact of Substrate Carbon Impurities on MOSFET Breakdown Voltage via Enhanced Phosphorus Out-Diffusion in n/n ⁺ Epitaxial Wafers	65
Mo-P20	Sergey Pavlov	Infrared properties of a perfectly compensated germanium doped with shallow donors and acceptors below the Mott transition	67
Mo-P21	Alexandra Abbadie	Mechanism of slip line propagation in advanced 300mm silicon substrates	69
Mo-P22	Sébastien Kerdilès	On the formation of local molten regions on Si surfaces by pulsed laser annealing at the melting threshold	71
Mo-P23	Mykola Kras'ko	On the gettering properties of isovalent tin and lead impurities in n-type Czochralski silicon	73

Poster Session 1 - Monday 28 September, 19:00-22:00			Page
Mo-P24	Shuyu Wen	Optically detected spin properties of the telecom L-band C center in silicon	75
Mo-P25	Yanan Xu	Origin of optically active Er ³⁺ sites in Silicon on Insulator-based photonic waveguides	76
Mo-P26	Kevin Lauer	Progress in understanding optically detected magnetic resonance (ODMR) spectra of ASi-Sii-defects	78
Mo-P27	Francesco Sgarbossa	Pulsed Laser Melting for TOPCon technology: new routes to higher efficiency	80
Mo-P28	Vladimir Markevich	Radiation-induced defect reactions in Silicon Junction Barrier Schottky Diodes upon irradiation with alpha particles in different regimes	81
Mo-P29	Koji Sueoka	Search for stable atomic configurations in SiGe, SiSn, and GeSn alloys using DFT and optimization algorithms	82
Mo-P30	Marisa Di Sabatino	Structure loss during the Czochralski silicon process: causes, remedies and ML aid	84
Mo-P31	Sophie Pain	Superacid-based diagnosis of damage in high-carrier-lifetime crystalline silicon	85
Mo-P32	John Murphy	Surface passivation of silicon by ZnO/Al ₂ O ₃ stacks with controlled SiO _x interlayers	87
Mo-P33	Koji Ozawa	Theoretical study on the stability of Sn atom in Ge thin film grown on GaSb substrates	89

Tuesday, 29 September, 2026				Page
08:30-10:10	Silicon Carbide			
08:30-09:10	Tu-I1	Salvatore Coffa	Defects identification, testing and screening for reliable SiC devices	91
09:10-09:30	Tu-O1	Giorgio Migliore	SiC color centers for quantum sensing: an Electro-Luminescence based approach for their investigation	92
09:30-09:50	Tu-O2	Alexey Lyasota	Benchmarking single Er ³⁺ coherence in Silicon Carbide on Insulator-based micropillars	94
09:50-10:10	Tu-O3	Alexey Lyasota	Exploring erbium quantum emission in CMOS compatible hexagonal Silicon Carbide on Insulator photonics	95
10:10-10:40	<i>Coffee break</i>			
10:40-12:40	Silicon, Germanium and their Alloys I			
10:40-11:20	Tu-I2	Dominique Bougeard	Gate-defined quantum circuits in silicon-germanium heterostructures	97
11:20-11:40	Tu-O4	Benedetta Scandolaro	UV-nanosecond laser hyperdoping of Ge/Si and SiGe/Si epilayers	98
11:40-12:00	Tu-O5	Lars Rebohle	Crystallization of Sn-rich Si and Ge thin films by flash lamp annealing	100
12:00-12:20	Tu-O6	Enrico Di Russo	Ex-situ incorporation of Al in Ge by sputter deposition and pulsed laser melting: a new approach to fabricate hyper-doped Ge:Al alloys.	101
12:20-12:40	Tu-O7	Pejk Amoroso	Positron trapping in highly p-type Ge	103
12:40-13:40	<i>Lunch break</i>			
13:40-15:40	GeSn Special Session (LASTSTEP Project) I			
13:40-14:20	Tu-I3	Oussama Moutanabbir	GeSn Semiconductors: A Tale of Defects and Devices	104
14:20-14:40	Tu-O8	Dan Buca	Material and Design Trade-offs in GeSn-Based MQW Lasers on Silicon	105
14:40-15:00	Tu-O9	Walid Belaid	Room-Temperature Optical Gain Analysis in Biaxially Strained Bulk GeSn for Mid-Infrared Silicon Photonics	106
15:00-15:20	Tu-O10	Michael Oehme	MBE Growth of Sn/Ge MQW Structures	108
15:20-15:40	Tu-O11	Moustapha EL Kurdi	Germanium tin on insulator, a suitable platform for electrically driven Mid-IR emitters and detectors	109
15:40-16:10	<i>Coffee break</i>			
16:10-18:10	GeSn Special Session (LASTSTEP Project) II			
16:10-16:50	Tu-I4	Wei Du	SiGeSn Technology for Monolithic Infrared Silicon Photonics	110
16:50-17:10	Tu-O12	Théophile Willoquet	Improving the performance of GeSn infrared photodetectors on Si through nanoscale engineering	111

Tuesday, 29 September, 2026				Page
17:10-17:30	Tu-O13	Paul Goulain	Influence of Electrode Geometry and Thermal Annealing on the Electroluminescence of GeSn LEDs	113
17:30-17:50	Tu-O14	Lorenzo Finazzi	High Sn content GeSn-based Avalanche PhotoDiode for Medium InfraRed detection	115
17:50-18:10	Tu-O15	Giovanni Capellini	Operando study of device heating using full-field x-ray diffraction microscopy	117
19:00-22:00	<i>Dinner and Poster Session 2</i>			

Poster Session 2 - Tuesday 29 September, 19:00-22:00			Page
Tu-P1	Ioannis Deretzis	Ab Initio Modeling of Surface-Induced Effects on Quantum Gate Fidelity in 3C-SiC Divacancy Qubits	118
Tu-P2	Deren Yang	Atomic-scale mechanism of step-edge-induced stacking fault evolution during HVPE growth of (100) β -Ga ₂ O ₃	120
Tu-P3	Enrico Di Russo	Atomic-scale microscopy insights into order and disorder phenomena in Al _x Ga _{1-x} N	122
Tu-P5	Vladimir Kolkovsky	Deep Level Defects in β -Ga ₂ O ₃ : Insights from Hydrogenation and Oxygen Annealing Studies	124
Tu-P6	Vladimir Kolkovsky	Magnetron-Sputtered HfO ₂ Thin Films for Microelectronic and Sensor Applications	125
Tu-P7	Vanira Trifiletti	Defect Engineering and Passivation at Halide Perovskite and Kesterite Nanoparticles Interface: A Combined Experimental and DFT Study	126
Tu-P8	Corrado Del Conte	Defect studies and down conversion strategies of double-cation mixed perovskite solar cells	127
Tu-P9	Pavel Hazdra	Defect Suppression in Boron-Doped MW-PECVD-Grown (113)-Oriented Diamond Substrates for Vertical Power Schottky Diodes	129
Tu-P10	Kaisla Sutinen	Detection of nuclei for oxidation induced stacking faults	131
Tu-P11	Jeremie Chretien	Elaboration of 200 mm GeSnOI via Bonded Etch-Back SOI process	133
Tu-P12	Oleg Olikh	Estimating recombination-active defect concentrations in silicon n ⁺ -p-p ⁺ structures via transfer learning from computer vision models	135
Tu-P13	Mahsa Masoud	Identification of the dominant trap states in mixed halide perovskite pellets	137
Tu-P14	Gaetano Calogero	Impact of Ionic Defects on Mesoporous Perovskite Solar Cells and X-Ray Detectors	138
Tu-P15	Francesco Sgarbossa	Lithium-free segmentable hyperpure germanium detector via Pulsed Laser Melting	140
Tu-P16	Vincent Reboud	Monolithic GeSn Photodetectors Integrated on Silicon for Mid-Infrared Applications	141
Tu-P17	Valentina Arena	Multiparametric Control of MAPbI ₃ Growth via Low-Vacuum Proximity-Space Effusion	143
Tu-P18	Szilard Pothorszky	Non-destructive light scattering-based bulk micro defect detection in silicon wafers	145
Tu-P19	Marisa Di Sabatino	Novel method to measure the temperature-dependent minority carrier lifetime of crystalline silicon wafers for solar cell applications	147
Tu-P20	Amy Albrecht	Optical Characterisation of Colour Centres in Nitride Layers	148
Tu-P21	Ulrich Bläß	Origin and evolution of basal dislocations in HVPE grown GaN	150
Tu-P22	Hartmut Bracht, Tröger-Neuhaus	Oxygen diffusion in Aluminium-Nitride	151
Tu-P23	Martin Herms	Photo-elastic Characterization of InP Wafers	152
Tu-P24	Gabriele Seguini	Photo electrical characterization of the interface states in dielectric/AlGaIn/GaN structures	153

Poster Session 2 - Tuesday 29 September, 19:00-22:00			Page
Tu-P25	Kuei-Shen Hsu	Photoluminescence spectroscopy study on hydride vapour phase epitaxy grown GaN:Mn using metal-organic precursor doping approach	154
Tu-P26	Jiri Tomkovic	Response Surface Modelling for a Vertical GaN HVPE Reactor within a Constrained Design Space	156
Tu-P27	Walid Belaid	Strain-controlled directness and confinement margins in CGeSn/(Si)GeSn MQW emitters on (001) Ge/Si	158
Tu-P28	Nishant Saini	Study of Defect Physics in Zirconia MIM Capacitors	159
Tu-P29	Anita Patelli	Synthesis of artificial graphene in the AlGa _N /Ga _N heterostructure through block copolymer self-assembly	161
Tu-P30	Enrico Di Russo	Synthesis of supersaturated GeSn alloys on Ge and Ge-on-Si by sputter deposition and nanosecond pulsed laser melting	162
Tu-P31	Simona Binetti	Towards Scalable Flexible Kesterite-based solar cells: Addressing Bulk and Interface Defects through Drop-on-Demand Inkjet Printing	164

Wednesday, 30 September, 2026				Page
08:30-10:30	Nitride Semiconductors			
08:30-09:10	We-I1	Rachel Oliver	Controlling formation of single photon emitting colour centres in MOVPE of gallium nitride	165
09:10-09:30	We-O1	Sébastien Pezzagna	Photo-induced emission hopping of bright and regularly occurring native quantum emitters in AlN grown by molecular beam epitaxy	166
09:30-09:50	We-O2	Leon Schiller	Non-destructive visualization of the threading dislocation content in PVT-grown bulk AlN on wafer scale	167
09:50-10:30	We-I2	Franziska C. Beyer	Plasma enhanced Atomic Layer Etching on Nitrides and SiC for high power and photonic application	169
10:30-11:00	<i>Coffee Break</i>			
11:00-18:00	<i>Social excursion</i>			
19:00-	<i>Social dinner</i>			

Thursday, 1 October, 2026				Page
08:30-10:10	Perovskites and their Applications			
08:30-09:10	Th-I1	Ivan Scheblykin	Metal-Halide Perovskites and Their “Magic” Defects	171
09:10-09:30	Th-O1	Andrea Ciavatti	Unravel the contribution of Bulk and Surface States in 2D-layered Perovskite by means of Photocurrent Spectroscopies	172
09:30-09:50	Th-O2	Giuseppe Fisicaro	Atomistic Engineering of Nucleation and Defect-Mediated Phase Stability in MAPI Perovskites: An AI-Driven Computational Framework	174
09:50-10:10	Th-O3	Vanira Trifiletti	Evaluating Structural Stability and Optoelectronic Properties of Lead-Free Metal Halide Perovskite Thin Films	176
10:10-10:40	<i>Coffee break</i>			
10:40-12:40	Silicon, Germanium and their Alloys II			
10:40-11:20	Th-I2	Hartmut Bracht	Diffusion and Defect Reactions in Semiconductors: Progress and Challenges	177
11:20-11:40	Th-O4	Lena-Maria Sinz	Diffusion of p-type dopants in Germanium	178
11:40-12:00	Th-O5	Gaetano Calogero	Shallow junction formation in silicon by laser annealing of phosphorus end-terminated polymers	179
12:00-12:20	Th-O6	Daniel Hiller	Modulation Acceptor Doping of Silicon: Induced defects in SiO ₂ for hole generation in impurity-free Si	181
12:20-12:40	Th-O7	Giuseppe D'Arrigo	Beyond the Statistical Indeterminism of Ion Implantation: Toward Deterministic Nanoscale Doping and Defect Engineering	183
12:40-13:40	<i>Lunch break</i>			
13:40-15:40	Low Dimensional Semiconductors			
13:40-14:20	Th-I3	Zahid Durrani	Dopant atom engineering quantum dot single-electron transistors and memory in silicon	185
14:20-14:40	Th-O8	Gabriele Seguni	Tuning Kondo effect via two-dimensional confinement in highly doped silicon-on-insulator	187
14:40-15:00	Th-O9	Teimuraz Mtchedlidze (Mchedlidze)	Engineering 1DEG system in pure silicon	189
15:00-15:20	Th-O10	Damiano Ricciarelli	Exploring quantum effects and structural interplays in graphene-derived functional materials for sensing and beyond	191
15:20-15:40	Th-O11	Daniele Demeneghi	Sputter deposition and pulsed laser crystallisation of MoS ₂ films	193
15:40-16:10	<i>Coffee break</i>			
16:10-18:10	Advanced Characterization Techniques			
16:10-16:50	Th-I4	Isabella Mica	Laboratory Photoluminescence imaging apparatus for identifying crystallographic defects in silicon	194

Thursday, 1 October, 2026				Page
16:50-17:10	Th-O12	Nicholas Grant	A charge decoupling method to infer bulk recombination in high quality silicon wafers	196
17:10-17:30	Th-O13	Vladimir Kolkovsky	Beyond Conventional DLTS: Direct Observation of Isotope Shifts in Deep-Level Emission Using Laplace DLTS	198
17:30-17:50	Th-O14	Paolo La Torraca	Defect Profiling in AlInGaP Alloys via MOS Impedance Spectroscopy	199
17:50-18:10	Th-O15	Maryna Dryhailo	3D chemical mapping of dopant distribution in epitaxially grown heavily doped Si:P and SiGe:B using atom probe tomography	201
19:00-	Dinner			

Friday, 2 October, 2026				Page
08:30-10:30	Silicon for Photovoltaics and Microelectronics			
08:30-08:50	Fr-O1	Sophie Pain	Hydrogen migration in ALD-grown dielectrics for silicon surface passivation	202
08:50-09:10	Fr-O2	Gianmarco Puggioni	Investigation of Pinholes Opening in Silicon Solar Cell Passivated Contacts Induced by Pulsed Laser Annealing	204
09:10-09:30	Fr-O3	Alexandra Abbadie	Impact of metallic contamination and gettering in bipolar technologies	206
09:30-09:50	Fr-O4	Koji Sueoka	Atomic structures and stability of large-sized vacancy clusters and finite-size extended interstitial defects in silicon: A neural-network potential and first-principles study	208
09:50-10:10	Fr-O5	Oceane Fevrier	Diffusion and gettering mechanism of critical metals in 300mm silicon substrates	210
10:10-10:30	Fr-O6	Antonio Massimiliano Mio	TEM analysis of Textured Silicon Polymorph Crystals obtained via Nanoindentation and Annealing	212
10:30-11:00	<i>Coffee break</i>			
11:00-12:00	<i>Announcements, YRA and YSA, Closing Remarks</i>			
12:00-	<i>Lunch & departure</i>			

Dopants at the Atomic Limit in Silicon and Germanium

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Controlling the placement and electronic character of dopant atoms in semiconductors lies at the heart of both classical device technology and the emerging field of semiconductor quantum computing. As device dimensions approach the single-atom limit, however, the discrete quantum-mechanical nature of individual dopants demands fundamentally new approaches to fabrication and characterisation. Understanding how a dopant wavefunction is shaped by its host crystal, and how quantum confinement evolves as doped layers approach atomic thickness, are central questions that bridge fundamental defect physics and device engineering.

In this talk, I will present an overview of our group's recent work on atomic-scale dopant systems in silicon and germanium, combining ultrahigh vacuum scanning tunnelling microscopy (STM), soft X-ray angle-resolved photoemission spectroscopy (SX-ARPES), and theoretical modelling. We explore how dopant species, host material, and fabrication pathways influence incorporation, electronic structure, and quantum confinement. These studies include the development of alternative dopant chemistries enabling high-yield incorporation, the realisation of ultra-confined electronic systems in atomically thin doped layers, and the direct imaging of anisotropic dopant wavefunctions in silicon arising from the interplay of crystal symmetry and quantum confinement [1–5].

Taken together, this work advances atomic-scale control of dopant placement in silicon and germanium, and provides new insight into how atomic-scale structure and chemistry govern the electronic states of dopants and dopant structures in semiconductors.

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Scanning Spreading Resistance Microscopy as a Key Nano-Metrology Technique for Semiconductor Technology Scaling – History and Future

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The continued downscaling of nanoelectronic devices, where performance is governed by nanometer-accurate doping distributions, demands metrology solutions with matching spatial resolution. Scanning Spreading Resistance Microscopy (SSRM), an AFM-based technique that measures the resistance as current spreads from a high-pressure-induced β -tin phase of silicon beneath a conductive diamond tip, has met this need for over three decades [1]. The resulting spreading resistance is directly related to local resistivity, enabling reliable electrical characterization from lightly doped channel regions to heavily doped source/drain contacts. With calibration measurements on reference samples containing layers of known carrier concentration, spreading resistance maps can be converted into quantitative active carrier profiles, establishing SSRM as a key technique for carrier metrology.

In my talk, I will overview how SSRM has evolved from a two-dimensional mapping method suitable for early planar transistors into a tomographic nanoscale sensing method, known as scalpel-SSRM, capable of true 3D carrier mapping in state-of-the-art device architectures such as FinFETs, nanosheet FETs, and complementary FETs. I will also discuss force-modulated FFT-SSRM, which addresses parasitic resistances inherent to confined device volumes and thereby significantly improves spreading resistance sensitivity. Beyond silicon CMOS, I will show how SSRM has been applied extensively to solar cell and III–V semiconductor characterization. The implementation of artificial intelligence for automated quantitative SSRM processing will be presented as an example case to demonstrate how AI can accelerate SSRM data analysis. Finally, I will highlight essential diamond probe technology advances for improvements in spatial resolution.

Looking ahead, I will introduce emerging concepts such as in-situ SSRM integrated with FIB-SEM-TEM to facilitate site-specific analysis, and multi-probe approaches that bridge the low-pressure regime used for high-resolution mapping with the high-pressure regime required for tomographic imaging. Together, these developments sustain SSRM's position as a powerful and versatile tool for probing nanoscale electrical information in future semiconductor technologies.

[1] M. A. R. Laskar, L. Wouters, P. Lagrain, J. Serron, N. Peric, A. Pondini, P. Eyben, T. Hantschel and U. Celano, *Appl. Phys. Rev.* **2025**, 12, 041305.

Defect mitigation strategies for next-generation, high-efficiency silicon-based solar cells

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Crystalline silicon (c-Si) solar cells are now approaching their fundamental performance limits, with voltages now limited primarily by intrinsic recombination processes. We discuss the key remaining bulk and surface defects relevant for high-efficiency commercial c-Si solar cells, as well as strategies for mitigating these defects in next-generation devices, focusing particularly on work at ANU.

Remaining bulk defects include various defects related to oxygen complexes in Czochralski-grown silicon, including thermal donors and oxygen precipitates, as well as residual levels of metallic contamination (especially Fe). The former manifest for example in so-called “ring” defects, and can be mitigated by high-temperature treatments, while the latter can be reduced to trace levels via gettering by heavily doped regions, dielectric passivation layers, or polysilicon contacts. We show that with the aid of such treatments, the bulk lifetime in commercial c-Si wafers now closely approaches the intrinsic Auger limit.

Surface passivation in recent high-efficiency devices has also improved to the point that surface defects no longer significantly limit the cell voltage. Therefore, future innovation in surface and contact passivation for c-Si devices need not improve on current state-of-the-art levels of passivation, but only maintain these while reducing other losses (i.e. transport and optical losses) or realising other advantages such as reduced process cost or improved stability. In particular, degradation of surface passivation due to defect generation under ultraviolet light has re-emerged as a key concern for device stability in the field. We discuss the potential role of alternative passivation species such as chlorine in place of or in addition to hydrogen, and their potentially beneficial properties for stability. We also highlight some emerging potential alternatives to conventional passivation and contact layers that may offer benefits such as improved optical transparency, contact properties or stability.

Tuning superconductivity in ultra-doped Si and SiGe epilayers with Nanosecond Laser Doping

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Since the discovery of BCS superconductivity in silicon by nanosecond laser ultra-doping with boron, theoretical and experimental works have endeavored to understand what triggers and controls the superconducting phase. Indeed, superconducting Si has great potential to develop a cryogenic electronics with the advantages of large scale integration and high reproducibility [1,2]. Through the optimization of the nanosecond laser temporal profile, we achieved an excellent control of both the electrical and structural properties of ultra-doped Si thin layers, with a maximum carrier concentration of 8 at.%, the state of the art, in monocrystalline epilayers with few defects, 100% dopant activation up to and above the solubility limit, and a vertically homogeneous doping profile [1-3].

The control and improvement of the active doping is directly reflected in the control of the superconducting critical temperature T_c of such disordered superconductor, increased by 30% in this optimized setup, in agreement with theory and opposite to previous results (Fig.1) [4].

Furthermore, we demonstrated that superconductivity is not only controlled by doping, but also by the lattice deformation. Thus, it is possible to tune up to 50% T_c by modifying by 1% the lattice parameter, as shown through nanosecond laser incorporation of Ge up to 20 at.% [5].

Mastering and understanding the materials properties has brought to the development of all-silicon devices, such as Josephson junctions and superconducting microwave resonators [6]. Indeed, SQUIDS and Josephson junctions were developed [7], thanks to the excellent, epitaxial, transparent interface between superconducting Si and semiconducting Si, that we have characterized both at room temperature and at sub-K temperatures as a function of the semiconductor doping.

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[3] G. Hallais, et al., *Semicond. Sci. Tech.* 38, 034003 (2023)

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[7] F. Chiodi, et al., *Phys. Rev. B* 96, 024503 (2017)

Combination of layer deposition and pulsed UV laser annealing for thin GeSn:Sb layers hyperdoping

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GeSn has been attracting a lot of attention lately due to its potential uses in SWIR and MWIR photonics. Adding Sn to Ge at high substitutional concentrations (6–8% Sn) reduces the energy bandgap and changes its type from indirect to direct [1,2]. However, the low equilibrium solubility of Sn in Ge (<1 at.%) makes producing thick (~ 1 μm) GeSn layers with high Sn concentrations difficult. Recent research has shown that, by coupling Sn deposition on Ge substrates with pulsed UV laser annealing in the melt regime, it is possible to exceed this solid solubility and fabricate 200 nm-thick GeSn layers with Sn% > 6 at.% [3–5]. To facilitate the current flow across the final structure, GeSn integration requires the introduction of high dopant concentrations (>1020 cm^{-3}) within a shallow junction (<100 nm) close to the surface.

In this study, we describe a process that combines an ultra-thin (< 2 nm) Sb layer deposition on previously fabricated GeSn and a laser annealing to achieve surface melting (< 200 nm). This allows for the incorporation of high levels of antimony concentration (n-type doping). After fabricating a GeSn layer as previously describes, a 2-nm-thick Sb layer was deposited and the Sb/GeSn stack is then laser-annealed under various conditions to finally obtain a 100 nm-thick hyperdoped GeSn:Sb layer with an active Sb concentration around $3 \times 10^{20} \text{ cm}^{-3}$. Different investigations were also conducted on the melt depth evolution as a function of energy density for GeSn layers and on the impact of HF cleaning prior to the Sb layer deposition. Morphological and structural characterizations were performed to study the impact of Sb inclusion in GeSn by AFM (Fig. 1.a) and Raman spectroscopy (Fig. 1.b). Hall effect measurements (Fig. 1.c) and SIMS (Fig. 1.d) were used to analyze the electrical activation.

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[4] E. Di Russo *et al.*, “Synthesis of relaxed $\text{Ge}_{0.9}\text{Sn}_{0.1}/\text{Ge}$ by nanosecond pulsed laser melting,” *Applied Surface Science*, **2023**, vol. 612, p. 155817.

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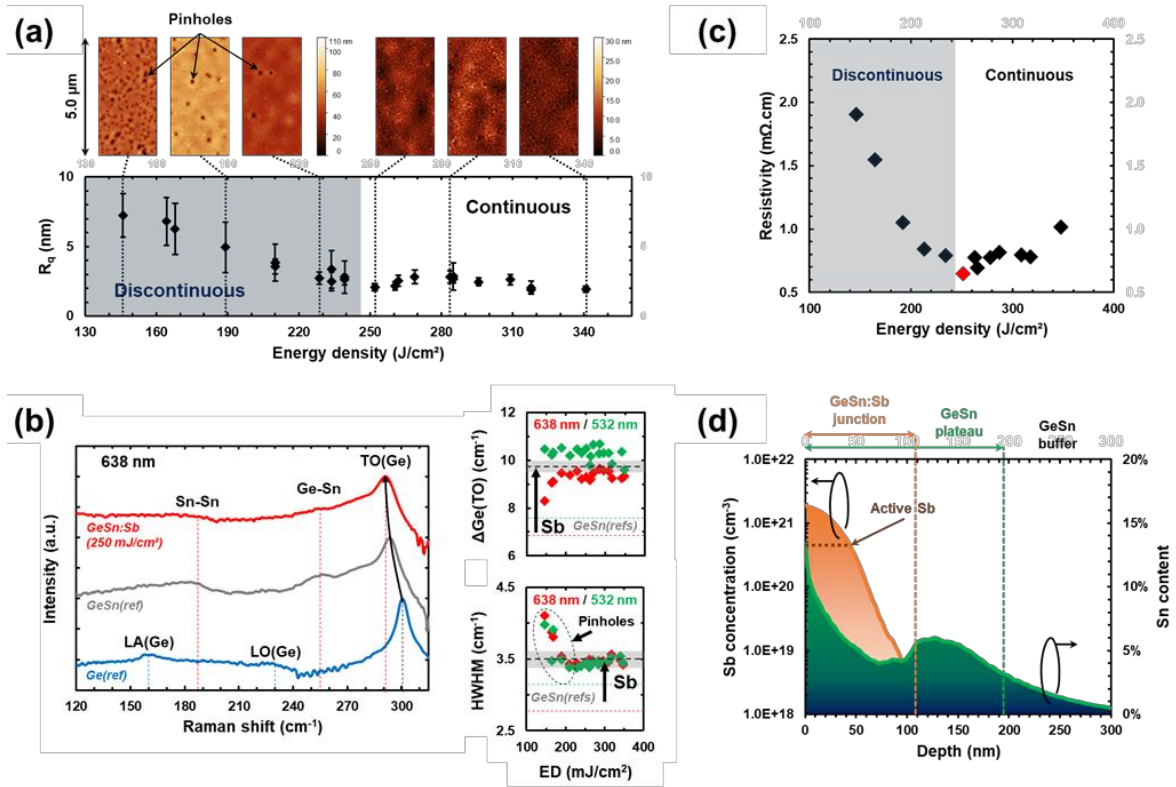


Fig. 1. (a) AFM measurements on GeSn:Sb samples after different laser annealing processes conditions on Sb-on-GeSn layers. The results exhibit two regimes in melting conditions: a first “discontinuous” regime showing pinholes (decreasing roughness values when increasing energy densities) and a “continuous” regime displaying a flat surface (constant roughness values). (b) Raman spectroscopy spectra for Ge, GeSn and GeSn:Sb samples. We observe a drastic shift of the TO(Ge) mode to lower frequencies. (Insets) Raman shift of the TO(Ge) mode and Half Width at Half Maximum (HWHM) as function of the energy density depicting the significant impact of the Sb incorporation. (c) Resistivity as function of the energy density (red point: best condition). (d) Sb chemical concentration and Sn content as function of depth for our best condition. Brown dotted line indicates the active Sb concentration.

Defect characterization in monolithic integrated Ge-on-Si layers grown by Low-Energy Plasma-Enhanced Chemical Vapour Deposition

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Silicon is the bedrock of modern microelectronics however its intrinsic limitations have driven the search for complementary materials compatible with silicon-technology.

In this context, Ge-on-Si structures have emerged as a compelling solution, combining germanium's superior optoelectronic properties with the scalability and CMOS compatibility of silicon, making them attractive for photonic integrated circuits and infrared imaging.

Nevertheless, the 4.2% lattice mismatch between Ge and Si leads to the formation of defects that degrade device performance by acting as non-radiative recombination centers. Consequently, effective defect reduction and comprehensive characterization are essential for the development of high-performance Ge-on-Si technologies.

Here we report in-depth characterization of dislocation evolution in 1500 nm-thick Ge-on-Si epilayers grown by low-energy plasma-enhanced chemical vapor deposition and subsequently cycled annealed from 600 °C to different maximum temperatures ranging from 650 to 760 °C, retaining an as-grown sample as reference. Through optimized thermal treatment, the threading dislocation density was reduced from $2 \times 10^9 \text{ cm}^{-2}$ to below $1 \times 10^7 \text{ cm}^{-2}$.

By combining X-ray diffraction (XRD), transmission electron microscopy, photoluminescence, atomic force microscopy and defect etch characterization, insight into the trade-off between surface roughness, and Si–Ge interdiffusion and threading dislocation density after high thermal budgets was achieved.

Furthermore, as-grown samples are dominated by 60° misfit dislocation and exhibit limited photoluminescence emission. After annealing at relatively low temperatures, XRD spectra suggests the presence of 90° dislocations, whereas photoluminescence suggests the presence of gliding 60° dislocation. This discrepancy is tentatively attributed to the pairing of isolated 60° dislocations upon annealing, resulting in an effective Burgers vector equivalent to that of 90° dislocations.

While high-temperature treatments promote defect annihilation, careful optimization is required to avoid detrimental effects. The structural and optical characterization presented here provides critical insight into managing the trade-off between defect mitigation and material preservation, advancing monolithically integrated Ge-on-Si platforms.

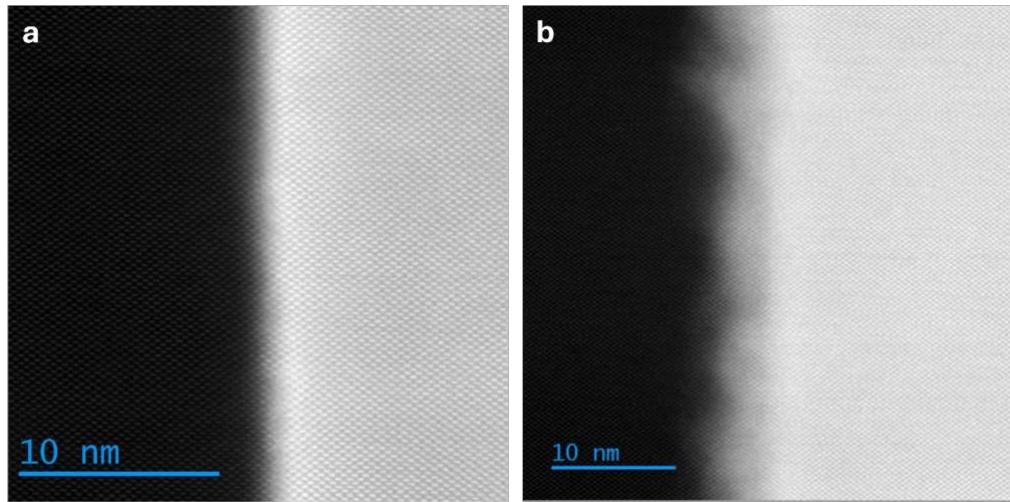


Fig. 1- Cross-sectional STEM–HAADF (Z-contrast) images of Ge-on-Si layers (a) in the as-grown condition and (b) after thermal cycling annealing treatment. The post-annealed sample exhibits an approximately 10 nm-thick interfacial region, in which a $\text{Si}_{1-x}\text{Ge}_x$ alloy has formed between the silicon substrate and the germanium layer, consistent with silicon interdiffusion during high-temperature processing.

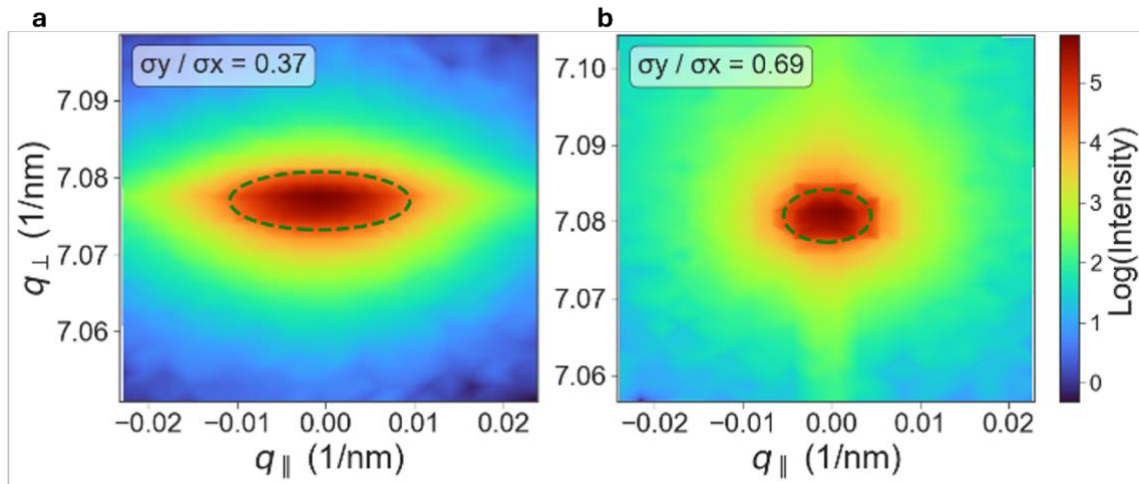


Fig. 2- Reciprocal space mapping around (004) Ge reflection for Ge-on-Si layers: (a) as-grown showing broadening consistent with uncorrelated 60° dislocations; (b) after cyclic thermal annealing, indicating the transition toward 90° dislocations.

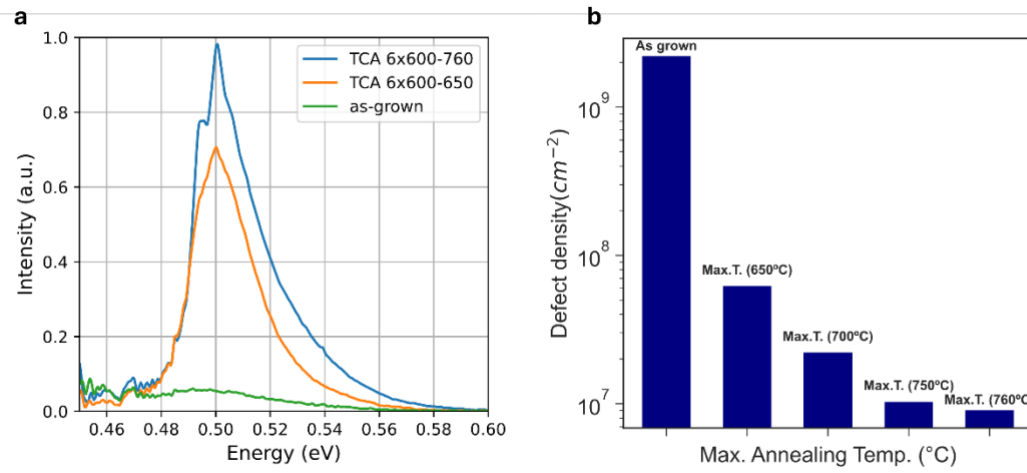


Fig. 3- Effect of thermal cycling annealing at different maximum temperatures on defect-related properties in Ge-on-Si layers: (a) Photoluminescence spectra of Ge-on-Si layers highlighting radiative recombination associated with defect-related energy levels (b) threading dislocation density determined after selective etching of defective regions and subsequent etch-pit counting by scanning electron microscopy.

Hyperdoped and Highly Strained Ge:Sb layers by Pulsed Laser Melting for Next-Generation Germanium Crystalline Gamma-Ray Sources

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The requirement of induced highly controlled deformation in germanium has become prominent in various research areas, including nanoelectronics, photonics, photovoltaics, and gamma ray production [1,2,3]. Pulsed laser melting (PLM) techniques have recently been shown to be a successful strategy for achieving such highly strained states. This effectiveness is primarily due to the ability to introduce a high concentration of impurity atoms within the first few hundred nanometres of silicon and germanium. Remarkably, successful experiments have been conducted with antimony and tin atoms, demonstrating incorporation levels significantly exceeding their equilibrium solid solubilities [3,4].

The resulting layer exhibits excellent crystalline quality, attributed to the epitaxial regrowth that occurs during the extremely fast post-laser material cooling. Moreover, by exploring various laser parameters, it is possible to produce either pseudomorphic or relaxed surface layers, each serving different technological purposes [1].

In this study, different germanium crystal orientations $\langle 001 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ were investigated to determine the maximum incorporation limits. The results highlight the remarkable versatility and strong potential of this technique in the advancement of strain engineering in germanium. Various applications of strain engineering using pulsed laser melting (PLM) will be discussed, with a primary focus on the fabrication of germanium crystalline undulators. Through the heavy antimony doping of germanium, the first crystalline undulators produced by this technique have been fabricated and characterised. Their key properties will be reviewed, demonstrating significant promise for gamma-ray generation.

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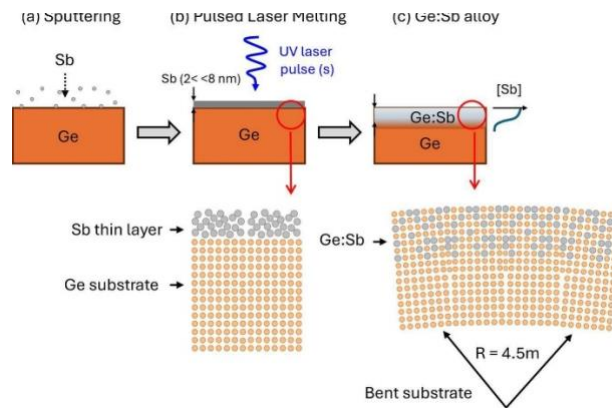


Fig. Process scheme

All-silicon telecom photodetectors via ion-beam engineering for photonic integration

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Silicon's transparency in the telecommunication bands (1260–1625 nm) has traditionally required hybrid integration of materials such as germanium for photodetection, limiting scalability and CMOS compatibility [1-3]. Here, we present a strategy based on **ion-beam engineering of deep-level dopants in silicon** to realize all-silicon, waveguide-coupled photodetectors operating at room temperature in the telecom C band. By implanting deep-level dopants near the solid-solubility limit, **sub-bandgap absorption is enhanced via defect-mediated states**, while preserving electronic transport [4].

The resulting devices achieve a responsivity of 0.56 A/W, external quantum efficiency of 44.8%, a 2 GHz bandwidth, and a noise-equivalent power of 4.2×10^{-10} W/Hz^{1/2} at 1550 nm. These results demonstrate that **ion implantation can create optically active defect states in silicon with practical photodetection performance**, enabling monolithic integration into photonic circuits. Beyond device operation, this approach provides insight into the **formation, energy levels, and transport properties of deep-level centers in silicon**, highlighting the potential of ion-beam techniques for **defect engineering and functionalization of silicon for advanced optoelectronic and quantum photonic applications**.

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- [4] Shaikh, S. M. *et al.* A high-performance all-silicon photodetector enabling telecom-wavelength detection at room temperature. arXiv:2412.05872 (2025).

SiGe Forward-Reverse linearly graded buffers for mid-infrared photonics

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Mid-infrared (MIR) photonics has attracted increasing interest due to its relevance for spectroscopic applications in the 3–15 μm spectral range, where many molecules exhibit strong and distinctive absorption fingerprints [1]. SiGe alloys represent a particularly promising platform for this purpose, as they combine compatibility with mature silicon technology, extended transparency beyond 8 μm , and composition-dependent optical properties. However, integrating high-performance electro-optical modulators (EOMs) into Ge-rich platforms remains challenging. The key difficulty in EOM design lies in achieving an optimal trade-off between propagation losses and extinction ratio: increasing the device length generally improves modulation efficiency, but at the expense of higher optical losses. In Schottky-based EOMs, these losses mainly arise from the modal overlap with the top metal layer, which is necessary to electrically bias the diode [2].

In order to address this challenge, we designed and realized forward-reverse SiGe graded buffers, where the vertical refractive index profile has been engineered to control the optical field distribution within the waveguide and push the mode away from the top metal layer. The samples were grown on Si(001) substrates by low-energy plasma-enhanced chemical vapor deposition and consist of two sections. The first is a forward-graded SiGe buffer, where the Ge content is linearly increased at 16.7%/ μm up to pure Ge. The second is a reverse-graded SiGe buffer, in which the Ge concentration is gradually reduced down to 80%. This second section required careful optimization of the growth parameters to prevent cracking caused by residual tensile strain. Selected samples were further analysed by scanning transmission electron microscopy (STEM), showing that the reverse-graded layers feature high crystalline quality. Waveguides fabricated from the optimized samples demonstrated propagation losses below 2 dB/cm in the 5–8.5 μm range.

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[2] T.H.N. Nguyen et al, Opt. Expr. **2022**, 30 47093

GeSn Waveguide Photodetectors for Next-Generation Silicon Photonics

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Group-IV GeSn alloys have been considered as a promising photodetector (PD) material for next-generation photonics [1]. Pure Ge has a direct bandgap of 0.8 eV, corresponding to a direct-gap absorption edge of 1550 nm. As a result, Ge photodetectors (PDs) are well suited for photodetection in the telecommunication O-band (1260–1360 nm), where chromatic dispersion is minimal and beneficial for short-reach applications. However, the limited direct-bandgap absorption range restricts Ge PDs from efficient operation in the more critical C+L bands (1530–1625 nm) [2], which are essential for low-loss, long-haul, high-capacity data transmission in silicon photonic optical receivers operating at 800 Gb/s, 1.6 Tb/s, and beyond. This problem can be effectively addressed by employing GeSn as the active material. Adding Sn into Ge can effectively reduce the bandgap energy, thereby extending the photodetection range to cover not only the entire telecommunication bands (1260–1675 nm), but also the emerging 2 μ m band (1800–2100 nm) for next-generation silicon photonic optical receivers.

Here, we present GeSn waveguide PDs (WGPDs) monolithically integrated on Ge-buffered (100) silicon wafers for wideband photodetection. GeSn/Ge heterostructures were grown on Si wafers using low-temperature molecular beam epitaxy for fabricating *p-i-n* WGPDs, as shown in Fig. 1(a). With a Sn content of 5.28%, the direct bandgap energy is reduced to 629 meV. As a result, from the measured optical responsivity, the cutoff wavelength photodetection is extended from 1550 nm to 2080 nm, covering the entire telecommunication bands. In addition, the long photon absorbing length can enhance the responsibility. The waveguide geometry allows for easy communication with other photonic devices to construct dense electronic-photonic integrated circuits. These results indicate that GeSn WGPDs are a promising candidate for next-generation optical receivers in silicon photonics.

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[2] C. H. Liu, R. Bansal, C. W. Wu, Y. T. Jheng, and G. E. Chang, *Adv. Photon. Res.* **2022**, 2100330 (2022).

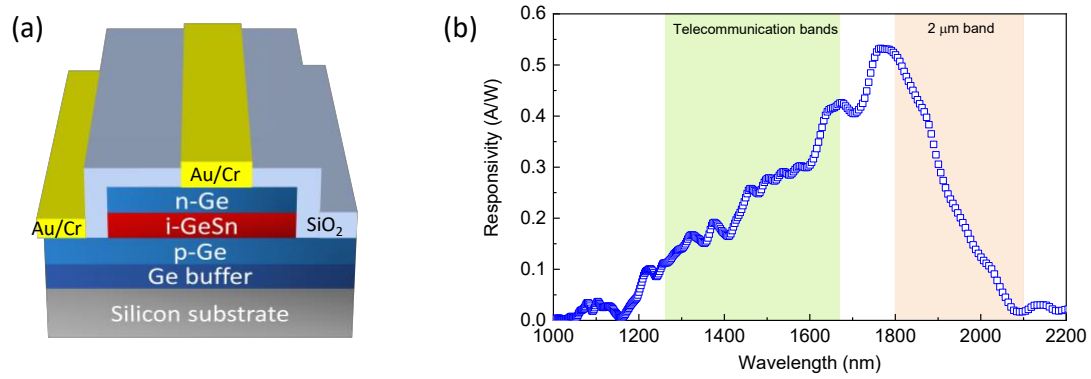


Fig. 1. (a) Schematics of GeSn waveguide $p-i-n$ photodetectors on silicon. (b) Optical responsivity measured at room temperature.

Emergent optical and transport phenomena in hyperdoped n-type Ge

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Hyperdoping group-IV semiconductors beyond equilibrium solubilities is crucial for advanced applications including nano- and quantum-electronics, photonics, and plasmonics. However, this process presents significant challenges due to solubility limits and dopant-defect interactions. In this study, we investigate the optical and electrical transport properties of hyperdoped Ge-on-Si epitaxial layers with a flat electron concentration profile reaching a record value of $2.7 \times 10^{20} \text{ cm}^{-3}$ over 300 nm. Hyperdoping was reached by in-situ phosphorous (P) doping followed by UV-nanosecond laser melting [1,2]. The resulting material exhibits a plasma wavelength of 3 μm , as determined by infrared reflectivity measurements. The flatness of the P activation profile is quantitatively demonstrated by differential van der Pauw-Hall measurements and confirmed through conductive atomic force microscopy.

Notably, in the hyperdoped regime, electron mobility deviates from previously reported trends (Fig. 1), and an additional term to the empirical model proposed by Menéndez et al. [3] is introduced [1]. For high-temperature annealed samples, mobility further decreases when the active P fraction drops below 30%, due to carrier scattering from inactive P clusters. Furthermore, ultrafast epitaxial regrowth induced by the laser process results in high biaxial tensile strain, measured by high-resolution X-ray diffraction, providing a valuable platform for bandgap engineering. This observation is supported by micro-Raman spectroscopy, which confirms strain and, once its contribution is removed, reveals a pronounced doping-induced Raman shift, enabling the establishment of an empirical relationship linking Stokes peak parameters to free-carrier concentration. Consistently, from temperature-dependent photoluminescence it is possible to reveal pronounced band filling and hot-carrier effects at extreme doping levels, reflecting strong many-body interactions and electron degeneracy at high carrier densities, along with a non-trivial temperature evolution of the bandgap (Fig. 2). These results provide new insight into the electrical and optical properties of n-type hyperdoped Ge-on-Si heterostructures, highlighting their potential for silicon-integrated midinfrared photonic and quantum devices.

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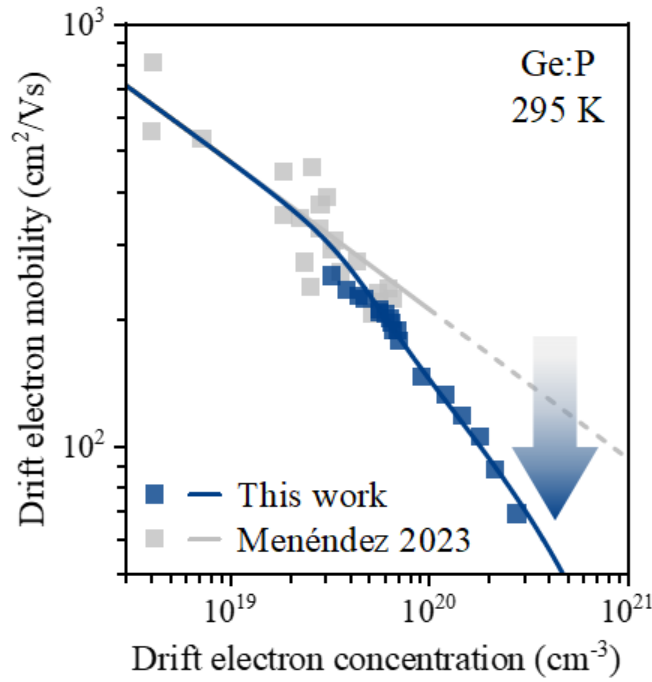


Fig. 1. Drift electron mobility as a function of carrier concentration at 295 K for Ge:P epilayers. Gray squares represent literature data, and the solid curve shows the empirical model proposed in [2], with the dashed extension obtained by extrapolation. Blue squares correspond to hyperdoped Ge:P, while the solid curve represents the modified empirical model introduced in this work, capturing the mobility drop at high carrier concentrations in the hyperdoped regime.

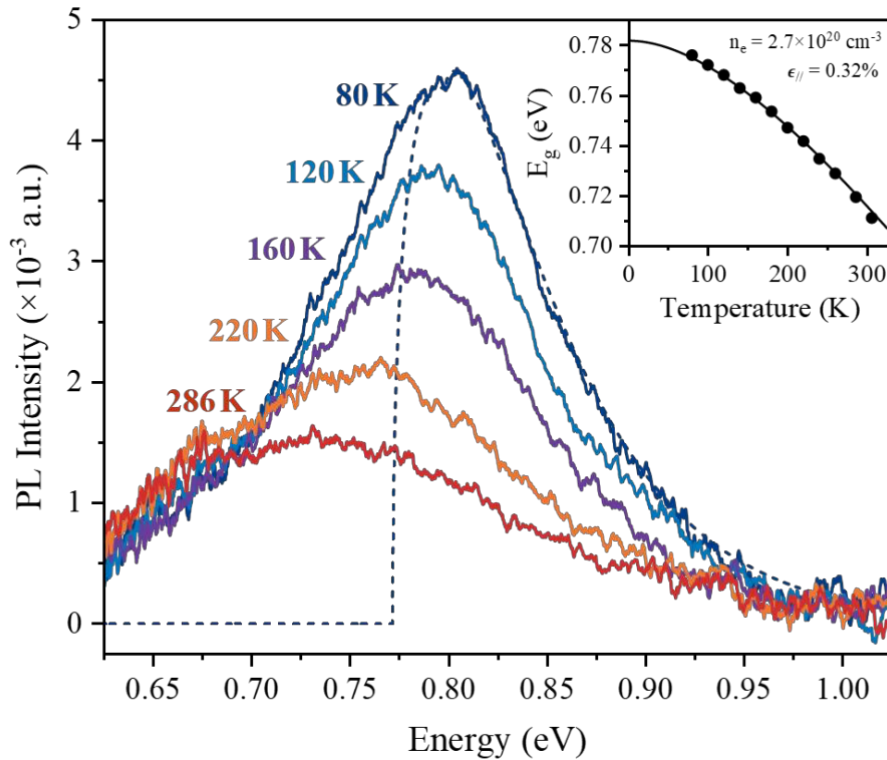


Fig. 2. Temperature-dependent photoluminescence of a hyperdoped Ge:P epitaxial layer with an electron concentration of $2.7 \times 10^{20} \text{ cm}^{-3}$ and a biaxial tensile strain of 0.32%. The inset shows the bandgap energy extracted from the PL peak fitting (illustrated by the dashed line in the main panel for the 80 K measurement) as a function of temperature; the solid curve represents the Varshni fit to the bandgap temperature dependence.

Controlled surface cleaning of MACE-nanotextured Ge for cost-efficient high-performance UV-SWIR photodetection

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Efficient photodetection in the near-infrared (NIR) and short-wave infrared (SWIR) ranges with wavelengths up to 1800 nm is in the core of multiple cutting-edge and high-societal-impact photonic technologies (e.g., telecommunications, autonomous driving, medical diagnostics, etc.). [1-3] While state-of-the-art solutions based on III-Vs [4] and plasma-nanotextured Ge [5] deliver high sensitivity, their implementation is often hindered by high material expenses and/or fabrication costs.

Nanotextured Ge by metal-assisted chemical etching (MACE, or MacEtch) [6] might serve as a cost-efficient and scalable alternative. MACE-nanotexturing has proved its competitiveness in Si-based devices [7], but no comparable performance has been shown for Ge. This is likely due to the need for high-quality surface passivation required for high-performance devices. Indeed, residual Ag nanoparticles (NPs), characteristic for anti-reflective MACE-nanotexturing [6, 7], act as surface generation/recombination sites. For Ge, removal of the NPs by conventional nitric-based solutions is limited by rapid wet oxidation and uncontrolled etching capable of degrading the surface nanotexture.

In this work we introduce a multistep wet chemical surface cleaning procedure and demonstrate its impact on the performance of fabricated Ge photodiodes [5]. Controlled sequential oxidation-dissolution process (HCl-H₂O₂-HCl) was employed to gently remove Ag NPs together with other chemical residues while preserving the surface nanotexture with its anti-reflective properties (Figure 1). Electrical characterization of passivated nanotextured Ge surfaces (Figure 2) confirms that the multistep cleaning significantly enhances interface quality resulting in effective lifetimes of ~650 μs, which is 10 and 3 times higher than those for no cleaning or conventional HCl cleaning, respectively. Finally, introduction of the cleaning in the actual device fabrication yields superior performance of the photodiodes with near-unity internal quantum efficiency (IQE) at only -0.5V bias for the wavelengths up to 1700 nm (Figure 2). These results demonstrate that efficient Ag removal in MACE-nanotextured Ge paves the road towards cost-efficient high-performance SWIR optoelectronics.

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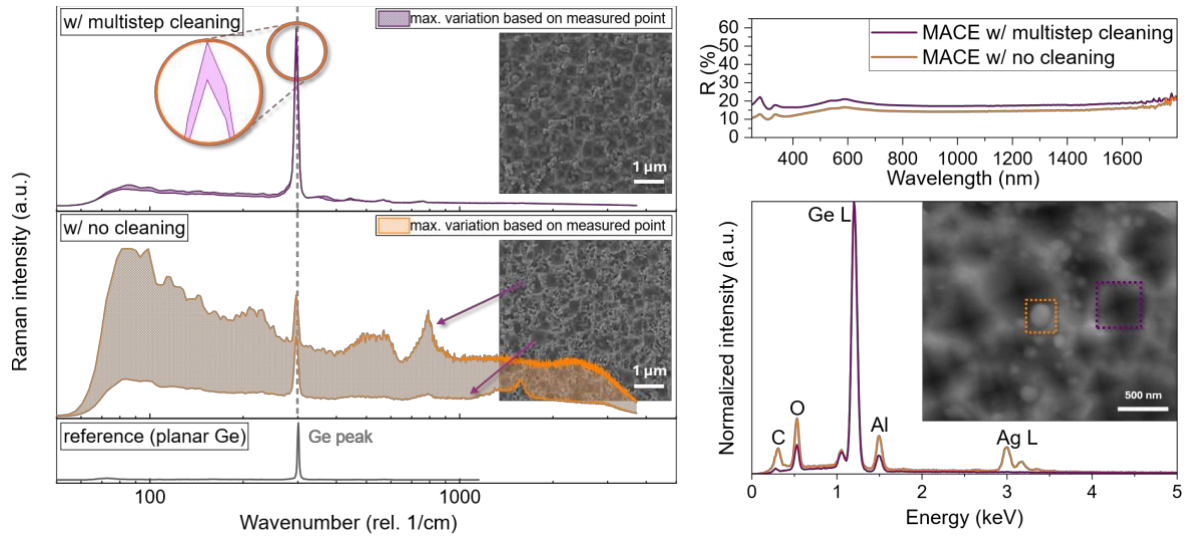


Fig. 1. (left) Raman spectra obtained from MACE-nanotextured Ge samples with multistep cleaning and no cleaning in comparison with planar bulk Ge reference. The filled areas show variation in the spectra collected from different locations on the samples; (top-right) Spectral reflectance measured from MACE-nanotextured Ge samples with multistep cleaning and with no cleaning; (bottom-right) EDX spectra obtained from particle-covered and particle-free areas of the Al_2O_3 passivated MACE-nanotextured Ge sample with multistep cleaning. The investigated areas are marked on the inset SEM image

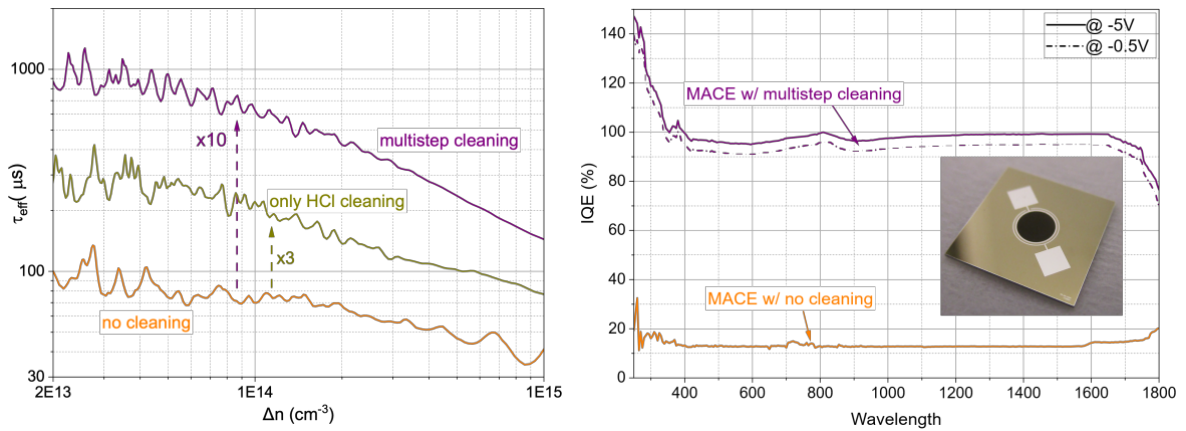


Fig. 2. (left) Assessment of ALD Al_2O_3 passivation quality of MACE-nanotextured Ge samples with multistep, conventional HCl and no cleaning prior ALD via injection level dependent effective lifetime measurement; (right) Internal quantum efficiency (IQE) of the MACE-nanotextured photodiodes with multistep and no cleaning prior ALD Al_2O_3 passivation. The IQE data is obtained at 0.5V (dash-dot lines) and 5V (solid lines) reverse biases. The inset demonstrates the real picture of the fabricated MACE-nanotextured Ge photodiode with multistep cleaning

QSOI®: a platform for large scale quantum integrated circuits

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Spin qubits implemented in silicon quantum dots (QDs) are among the most promising candidates for large-scale quantum computing due to their compatibility with CMOS technology and their strong potential for monolithic co-integration with control and readout electronics [1]–[3]. In this context, fully depleted silicon-on-insulator (FDSOI) technology offers unique advantages for quantum–classical integration. Its intrinsic electrostatic control, reduced variability, and the availability of a global back gate enable dynamic tuning of device characteristics [4], providing a powerful knob to optimize both performance and power consumption at cryogenic temperatures [5, 6].

In this work, we present our results on the quantum silicon-on-insulator (QSOI®) technology, inspired by the commercial 28 nm FDSOI process, and modified to address the specific requirements of spin qubit fabrication within a CMOS-compatible platform. Leveraging the industrial maturity of a commercial foundry process, we designed, fabricated and tested both quantum and classical devices on the same wafer. We will focus on the performance of the devices, with two objectives in mind: on the one hand, the development of a cryogenic Process Design Kit (PDK) suitable for quantum integrated circuit design. On the other hand, achieving the quantum regimes in arrays of quantum dots.

This work demonstrates that advanced FDSOI technology has the potential to support both high-quality silicon spin qubits and cryogenic CMOS electronics on the same wafer, establishing a scalable and manufacturable path toward large-scale quantum processors within a standard CMOS ecosystem.

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Cryogenic SiGe Transistors based on Modulation Acceptor Doping

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Doping at the nanoscale is becoming increasingly challenging for upcoming ultra-scaled technology nodes. This is related to abrupt doping profiles, random dopant fluctuations, and mobility degradation caused by channel-doping impurities, leading to increased dissipative losses and, consequently, lower energy efficiency. Thus, alternative approaches that circumvent these issues while offering the advantages of higher driving currents could facilitate the development of enhanced low-power devices. As an alternative approach, modulation acceptor doping (MAD), enables charge-carrier accumulation in the channel by embedding acceptor states in the surrounding gate oxide, resulting in improved on-state performance while maintaining an undisturbed lattice structure. [1]

Here, we demonstrate the first experimental vehicle to validate the MAD concept on SiGe semiconductors, which is highly important for enhancing device conductivity, especially in cryo-CMOS and quantum applications, where conventional impurity doping is detrimental because an undisturbed lattice structure is required. MAD is demonstrated via Al-induced acceptor states in a SiO₂ gate dielectric, using SiGe-based Schottky barrier field-effect transistors (SBFET) as a test vehicle. The proposed devices are based on abrupt Al-Si-SiGe multi-heterojunction contacts, enabling hysteresis-free, stable device operation over the temperature range from 4.5 to 373 K. The statistical evaluation of key parameters relative to a reference sample without MAD, using pulsed and temperature-dependent electrical measurements, revealed a 4170-fold increase in the conductivity of the ungated SiGe channel and a 3-fold increase in the p-type on-state current when the device is operated as a transistor at room temperature. [2] Moreover, we demonstrate a 100-fold improvement in the I_{ON}/I_{OFF} ratio by embedding the proposed MAD SiGe channels into multi-gate transistors (see Fig. 1a) that suppress reverse junction leakage current. Providing temperature-dependent electronic transport data down to $T = 4.5$ K (see Fig. 1b), we discuss the electronic transport and have extracted key metrics for the proposed transistors, which exceed those of similar impurity-doped counterparts suffering from dopant freeze-out. Most notably, the application of MAD to Ge-rich SBFETs may pave the way for nanoscale devices that harness both the advantages of MAD and Ge, enabling ultra-scaled transistors with lower supply voltages and faster switching speeds, which are highly interesting for cryogenic electronics.

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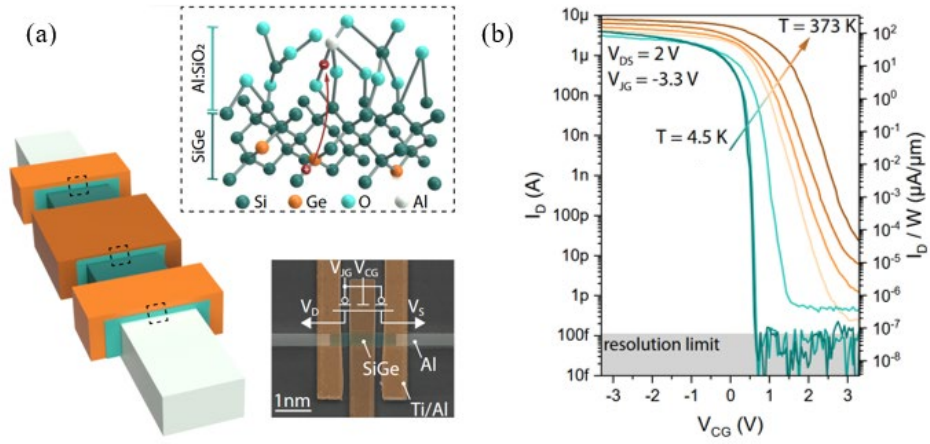


Fig. 1. (a) 3-D sketch of the fabricated multi-gate SiGe MAD transistor, including the respective schematic illustration of the MAD oxide stack and a false-color SEM image with device symbol. (b) Temperature-dependent transfer characteristic recorded from 4.5 K to 373 K.

Non-volatile reconfigurable Al-Si transistors via ferroelectrically modulated Schottky barriers

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Deep learning algorithms have recently achieved remarkable performance and are now pervasive across many different technological domains. Training and inference of artificial neural networks (ANN) are two operations that give rise to a high energy consumption on conventional von Neumann hardware, as substantial power and latency resources are spent shuffling data between processing units and memory. For this reason, there is a mounting need for versatile semiconductor device platforms that can merge logic and memory functionalities into a single device.

Reconfigurable field effect transistors based on ultrathin-body channels and electrostatically tuned Schottky junctions are able to be programmed at run-time between n- and p-FET conductance. Distinct to MOSFETs, there is no need of conventional impurity doping, as these devices exploit the electrostatic modulation of the Schottky barrier shape and thus the selective charge carrier injection capabilities for electrons and holes, ensuring an extreme flexibility of the device, even after fabrication. [1]

Here we present Al-Si-based reconfigurable transistors, fabricated from a silicon-on-insulator (SOI) substrate with a device layer of 20 nm. We show that with the addition of a ferroelectric layer in the gate stack, the Schottky junction transmissibility can be tuned in a non-volatile manner, effectively realizing logic devices whose behaviour can be permanently influenced by the ferroelectric remnant polarization, merging logic and memory functionalities into a single semiconductor device. [2] The multi-domain nature of HZO allows for the selection of different current levels, depending on the chosen programming pulse. All the achievable states show a retention over time, owing to the stability of the HZO polarization.

These devices pave the way for the future realization of a fully optimized non-volatile reconfigurable transistor, an ideal building block for novel hardware, enabling low-power circuits for ANN execution.

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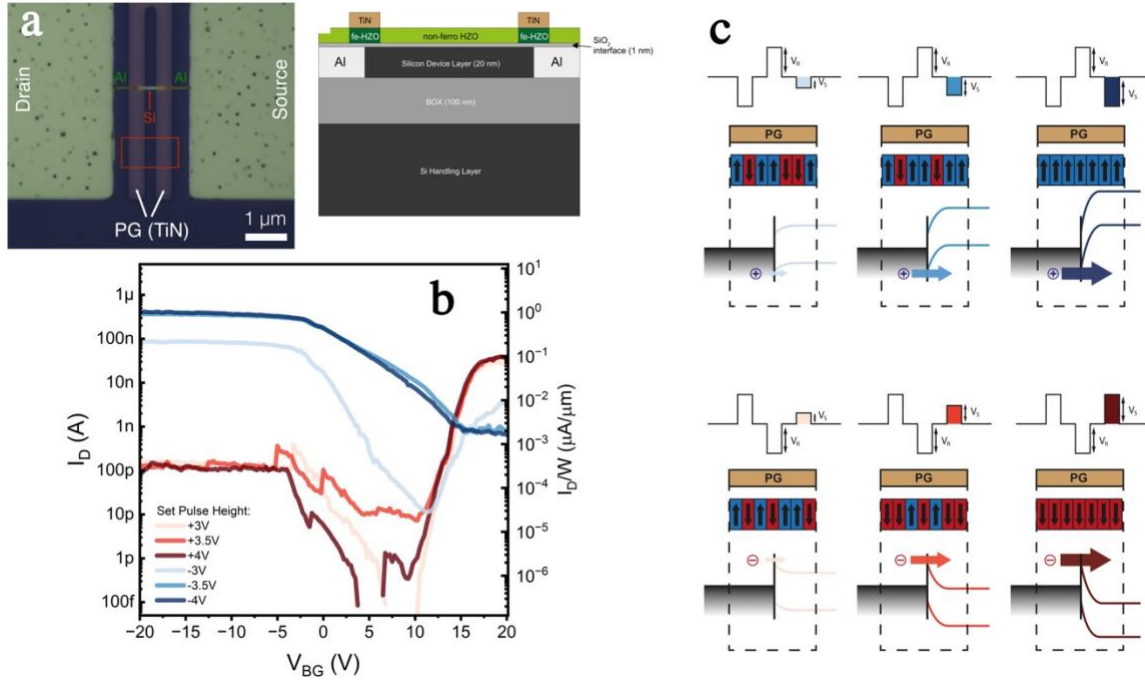


Fig. 1. a) Left: Optical microscope image of a fabricated device, showing the program gate (PG) covering the Al-Si Schottky junctions. Right: The stack scheme of the fabricated device. The ferroelectric HZO is positioned exclusively above the Schottky junctions. b) Transfer characteristics of the fabricated device, showing progressive adjustment of electron and hole injection as HZO domains are polarized as steered by the program pulse height and sign. Importantly, non-volatile p-/n-type programming of the device is demonstrated. c) The diagram shows the effect of a negative program pulse over the domain orientation of the ferroelectric layer. The Schottky barrier is modulated accordingly by the remnant polarization of the domains. In the lower part of the panel, the effect of a positive program pulse is shown.

Photoexcited muon spin spectroscopy for studying bulk, surface, and temperature-dependent carrier recombination in silicon wafers and solar cells

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Understanding charge carrier recombination kinetics is critical in optimizing photovoltaic materials and devices. Photoexcited muon spin spectroscopy (photo- μ SR) is a novel method for probing carrier dynamics in semiconductors [1]. This pump-probe technique – available at the UK's ISIS Neutron and Muon Source – involves generation of excess charge carriers by laser excitation followed by implantation of positive muons into a sample. Muon spin relaxation, induced by the interaction between muons and excess carriers, is directly related to the excess carrier density, enabling depth-resolved lifetime measurements of silicon wafers [2] and partially processed or even finished solar cells and other devices [3].

The presentation will provide an overview of photo- μ SR and highlight its potential for characterising semiconductor materials and devices. We will present new data for the temperature-dependence of carrier lifetime in completed 26% efficient silicon heterojunction (SHJ) solar cells (Fig. 1). Such data are important because these cells are starting to be used in extreme environments, such as space, where temperature varies substantially during operation. We also show depth-dependent data which show that photo- μ SR can be used to resolve differences in surface passivation quality in silicon wafers (Fig. 2). We find the technique can successfully be used over a wide range of surface recombination velocities (~ 10 –5000 cm/s) [4].

When interpreting photo- μ SR data for high-lifetime wafers or devices, it is important to understand that recombination-active defects can form upon exposure to the muon beam. For example, the state-of-the-art SHJ solar cell in Fig. 3 has photo- μ SR differential lifetimes lower than those from Suns- V_{oc} measurements. The photoluminescence (PL) imaging results confirm a reduction in lifetime coincident with the muon beam location, and the defects formed have been characterised by deep-level transient spectroscopy previously [3]. It has also been established that the damage formed can be partially recovered by subsequent annealing [5]. Thus, while photo- μ SR can provide information on bulk and surface recombination in completed semiconductor devices, any change in recombination associated with the measurement itself must be accounted for in the interpretation of the results.

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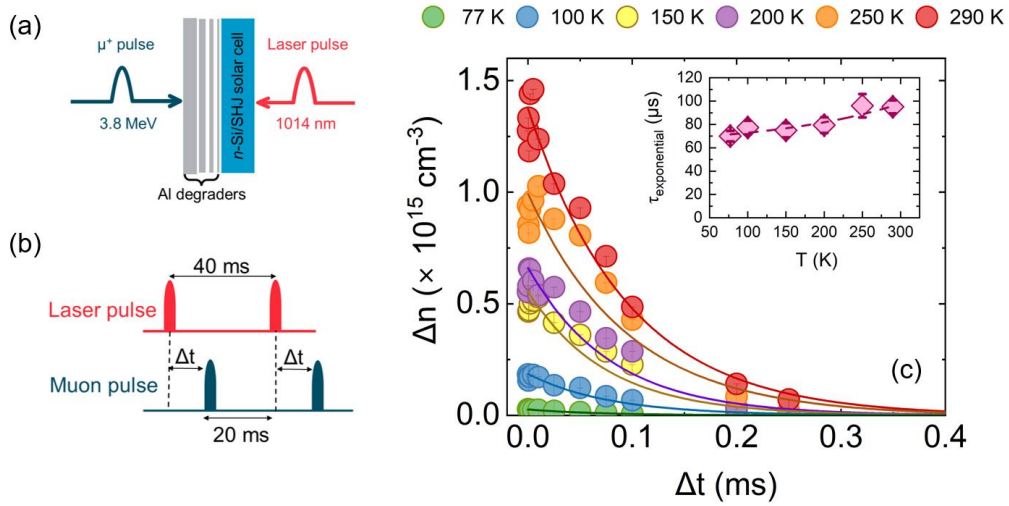


Fig. 1. (a) Schematic of experimental set-up showing front surface muon implantation and rear surface laser excitation. (b) Timing diagram of laser and muon pulse. (c) Photo- μ SR carrier lifetime spectrum measured at increasing temperatures (77 to 290 K) for a 26% efficient SHJ cell. The lifetimes from the exponential fits are plotted as a function of temperature in the inset graph.

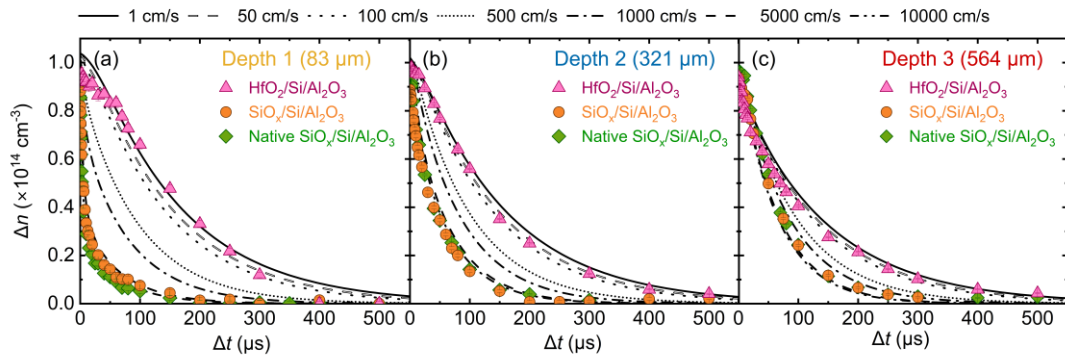


Fig. 2. Photo- μ SR carrier lifetime spectra measured from silicon samples with varying surface passivation quality with muons implanted at different depths from the muon-incident surface. The plotted curves are obtained from a 1D diffusion model with surface recombination velocities on the muon-incident surface varied from 1–10,000 cm/s and fixed to 1 cm/s on the Al_2O_3 passivated laser-incident surface (reproduced from [4]).

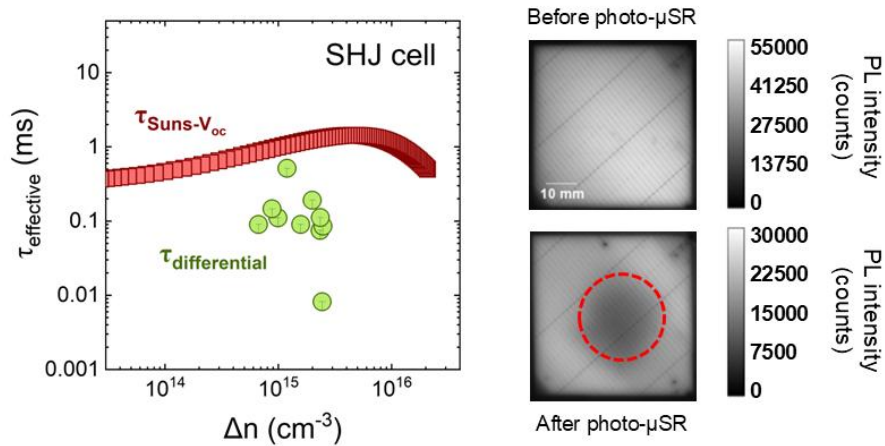


Fig. 3. Results for a 26% efficient silicon heterojunction (SHJ) solar cell. The differential lifetimes from photo- μ SR ($\tau_{\text{differential}}$) are lower than those from Suns- V_{oc} . PL images demonstrate reduced carrier lifetime in the location of the muon beam, showing the measurement creates defects in the sample being measured.

Engineering Ultrasmooth Sub-Nanometer Interlayers via Chemical Modulation for Suppression of Interface Defects in Advanced Si/HfO₂ MOS Technology

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Interfacial quality between the silicon substrate and high- κ dielectrics remains a pivotal challenge for optimizing the electrical performance of advanced CMOS gate stacks. [2] Conventional HF-last processes often trigger complex interfacial reactions during ALD growth and post-metallization annealing, leading to unwanted silicide/silicate formation and a high density of oxygen vacancies. [3,4] In this study, we present a defect-engineering strategy to suppress these deleterious effects by employing a tailored high-pH fluoride-based chemical modulation (NH₄F/(NH₄)₂SO₃/NH₄OH). This treatment facilitates the formation of an ultrasmooth, sub-nanometer (2~3 monolayers) SiO₂ interlayer with record-low surface roughness ($R_q = 0.06$ nm). By eliminating hillock-like surface features on SC-2 SiO₂ and providing a self-limiting etching characteristic, this chemical oxide layer serves as a robust template for subsequent HfO₂ deposition.

Electrical characterization reveals a significant ~80% reduction in interface trap density (D_{it}) and a ~60% decrease in fixed oxide charges, effectively minimizing charge-trapping centers. Furthermore, the transition from trap-controlled space-charge-limited conduction to tunneling-dominant transport confirms the superior integrity of the interface. Cross-sectional high-resolution scanning transmission electron microscopy (HRSTEM) and energy-dispersive X-ray spectroscopy (EDS) analysis verify an atomically abrupt Si/SiO₂/HfO₂ boundary without elemental intermixing, even after post-metallization annealing at 400°C. This work demonstrates that precise chemical modulation of the interlayer is a scalable pathway to achieve near-ideal interface characteristics and enhanced dielectric properties in advanced Si/high- κ MOS technology.

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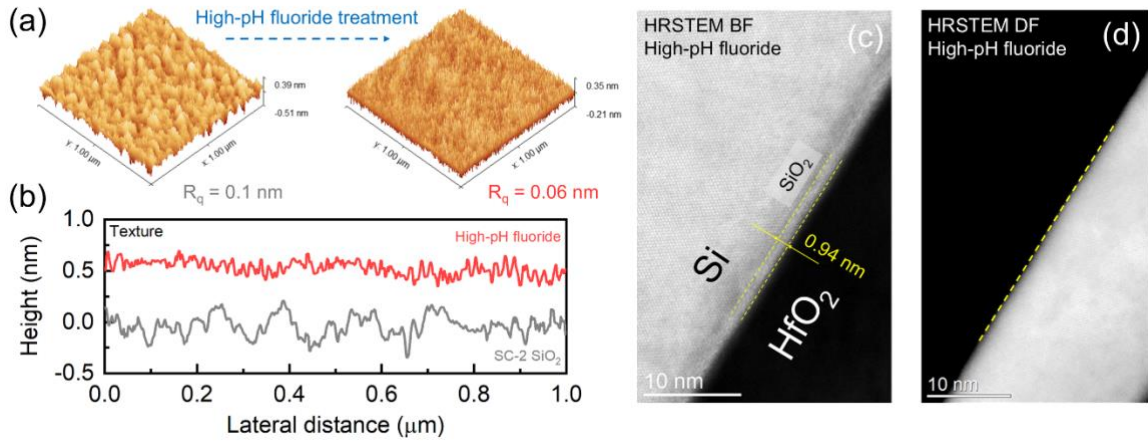


Fig. 1. Ultrasmooth sub-nanometer chemical SiO₂ surface via high-pH fluoride solution treatment. (a) The 1×1 μm² AFM 3D images of SC-2 SiO₂ after RCA cleaning and after 2-minute treatment. (b) The one-dimensional surface textures. (c) Bright-field HRSTEM image of the treated Si device (Si/SiO₂/HfO₂/TiN/Al) and its (d) corresponding dark-field image.

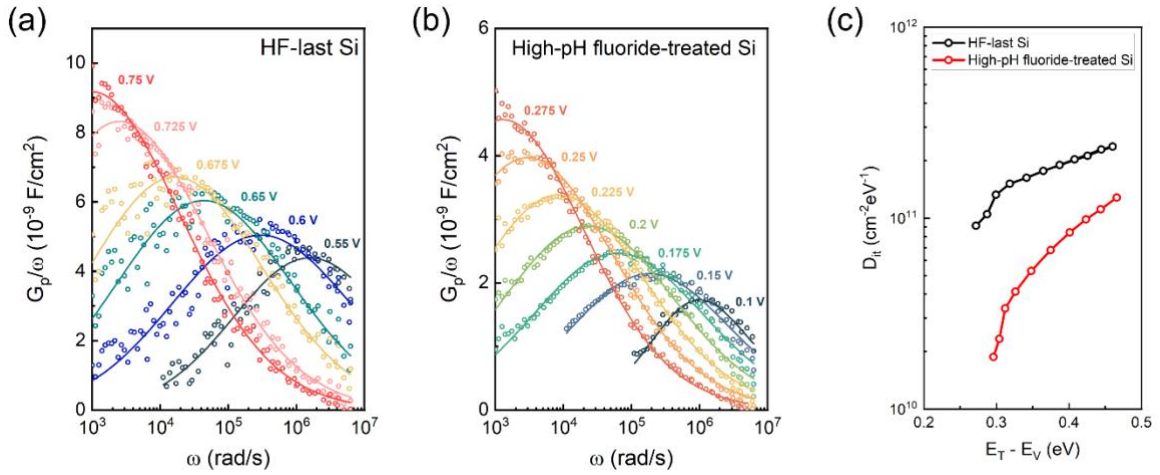


Fig. 2. The interface trap density (D_{it}) analysis through the conductance method. The G_p/ω - ω plots and corresponding fitting curves at different bias voltages for (a) HF-last and (b) high-pH fluoride-treated Si devices. (c) The extracted D_{it} values at different energy positions for both devices. The high-pH fluoride-treated Si device exhibits an 80% reduction in near-valence band edge D_{it} compared with the HF-last Si device, decreasing from 9.1×10^{10} to 1.8×10^{10} cm⁻²eV⁻¹.

From Defect-Induced Variability to Deterministic Control: Strain Gradients as a New Paradigm for Valley Engineering

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The Si/SiGe semiconductor platform is a leading architecture for spin-based quantum computing, offering single- and two-qubit gate fidelities above 99% and supporting linear arrays with more than ten quantum dots [1]. Its performance derives from the pristine Si quantum well—isolated from disorder by a SiGe barrier—and from the suppression of hyperfine interactions using isotopically enriched ²⁸Si. Despite this remarkable progress, the reliable control of valley states remains a central challenge for scalable silicon quantum processors. Valley splitting E_{vs} (<300 μ eV), which must be sufficiently large to ensure robust spin-qubit operation, is notoriously sensitive to structural imperfections including alloy disorder, interface roughness, atomic-scale intermixing, and strain inhomogeneities. As a result, valley physics lies at the intersection of quantum-device design and defect engineering. [2]

Historically, efforts to enhance valley splitting have focused on improving interface quality and modifying heterostructure design through approaches such as narrow quantum wells, Ge-alloyed or graded wells, Ge spikes, and wigggle-well architectures. [2,3] While these strategies can increase E_{vs} , they remain intrinsically linked to microscopic disorder, resulting in significant device-to-device variability. Achieving reproducible valley control therefore requires new design principles that move beyond defect mitigation towards deterministic engineering of the electronic landscape.[4]

In this presentation, I discuss the emerging role of mechanical and structural inhomogeneities in shaping valley physics in silicon quantum devices and highlight strain gradients as a previously underexplored yet highly effective tuning parameter. Unlike uniform strain, which has been extensively investigated, strain gradients arise naturally in realistic device architectures from process-induced stress, heterostructure design, thermal mismatch, and electrostatic gate layouts. Their influence on valley splitting, however, has remained largely unexplored.

To address this challenge, we combine finite-element modelling (FEM) of realistic SiGe/Si/SiGe device geometries with density-functional theory (DFT) calculations, establishing a multiscale framework that directly connects nanoscale strain distributions to quantum electronic properties. Full strain-tensor maps are obtained from three-dimensional device simulations and used to investigate the influence of spatially varying strain on valley states in silicon quantum wells.

Our calculations reveal that strain gradients provide a deterministic mechanism for modifying valley splitting. For an 8 nm Si quantum well, an intrinsic valley splitting of approximately 200 μ eV remains stable up to a critical strain-gradient threshold, beyond which E_{vs} increases systematically with increasing gradient magnitude (see fig. 1). These

results demonstrate that valley splitting can be engineered not only through confinement and interface design, but also through controlled spatial variations in strain.

The broader implication is that strain gradients represent a new design paradigm for quantum-device engineering. Rather than viewing structural inhomogeneities solely as sources of variability, certain forms of non-uniform strain may be harnessed to achieve robust and reproducible control of quantum states. This perspective opens new opportunities for defect-aware design strategies in silicon quantum technologies and illustrates how multiscale modelling can guide the development of future semiconductor quantum processors.

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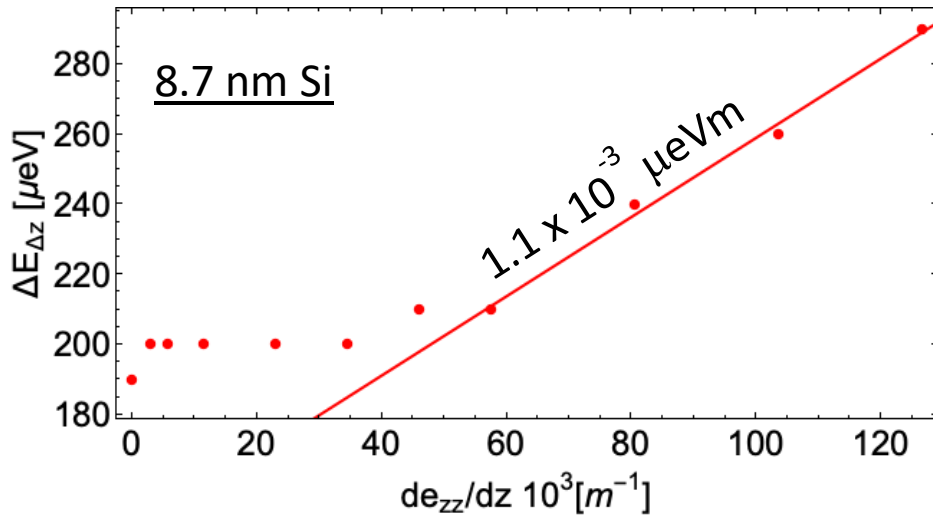


Fig. 1. Energy splitting of the Δ_z valleys as a function of strain gradient.

Low Temperature Epitaxy of Planar Hexagonal Germanium

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Germanium (Ge) is a material of significant interest in the field of semiconductor technology due to its electronic properties. The scientific community has recently intensified research efforts to obtain hexagonal Ge (Ge-2H), which has been shown to exhibit a direct bandgap. Ge-2H has thus far been mainly grown via core/shell nanowires [1], which inherently restrict the active volume. This hinders fundamental property investigation and device fabrication. To overcome this constraint, it is therefore essential to synthesize high-quality planar Ge-2H crystals.

In this context, we have grown Ge-2H layers on wurtzite m-plane cadmium sulfide (CdS) substrates. The Ge deposition was performed by low-energy plasma-enhanced CVD at low temperature (low-T) (200 – 300°C) to prevent Cd desorption from the substrate, which would lead to a substoichiometric surface and possibly result in the loss of the substrate's template effect on germanium growth. Prior to the low-T growths on CdS substrates, a preliminary study on low-T epitaxy on silicon substrates was conducted, yielding crystalline thin Ge epilayers even at ultra-low-T (250°C).

The Ge/CdS samples were structurally characterized by high-resolution X-ray diffraction (HR-XRD), energy-dispersive X-ray spectroscopy, transmission electron microscopy (TEM), and Raman spectroscopy.

Fig.1(a) and (b) show polarized Raman spectra of the 10 and 50 nm-thick Ge/CdS samples, respectively: in the $x(y,y)x$ configuration, according to Porto notation, the transverse optical E_{2g} mode of Ge-2H ($\sim 288\text{ cm}^{-1}$ [2]) is observed, indicating the presence of the epitaxial crystalline Ge-2H phase. This is directly confirmed by the TEM image (Fig.1(c)), which also shows that part of the Ge film eventually relaxes to the cubic phase (Ge-3C). Indeed, HR-XRD measurements show that Bragg peaks corresponding to both hexagonal and cubic phases are present (Fig.1(d)), indicating a roughly 2:1 ratio between Ge-2H and Ge-3C. Further investigations, including photoluminescence, will be carried out to assess the possible direct bandgap emission from planar Ge-2H.

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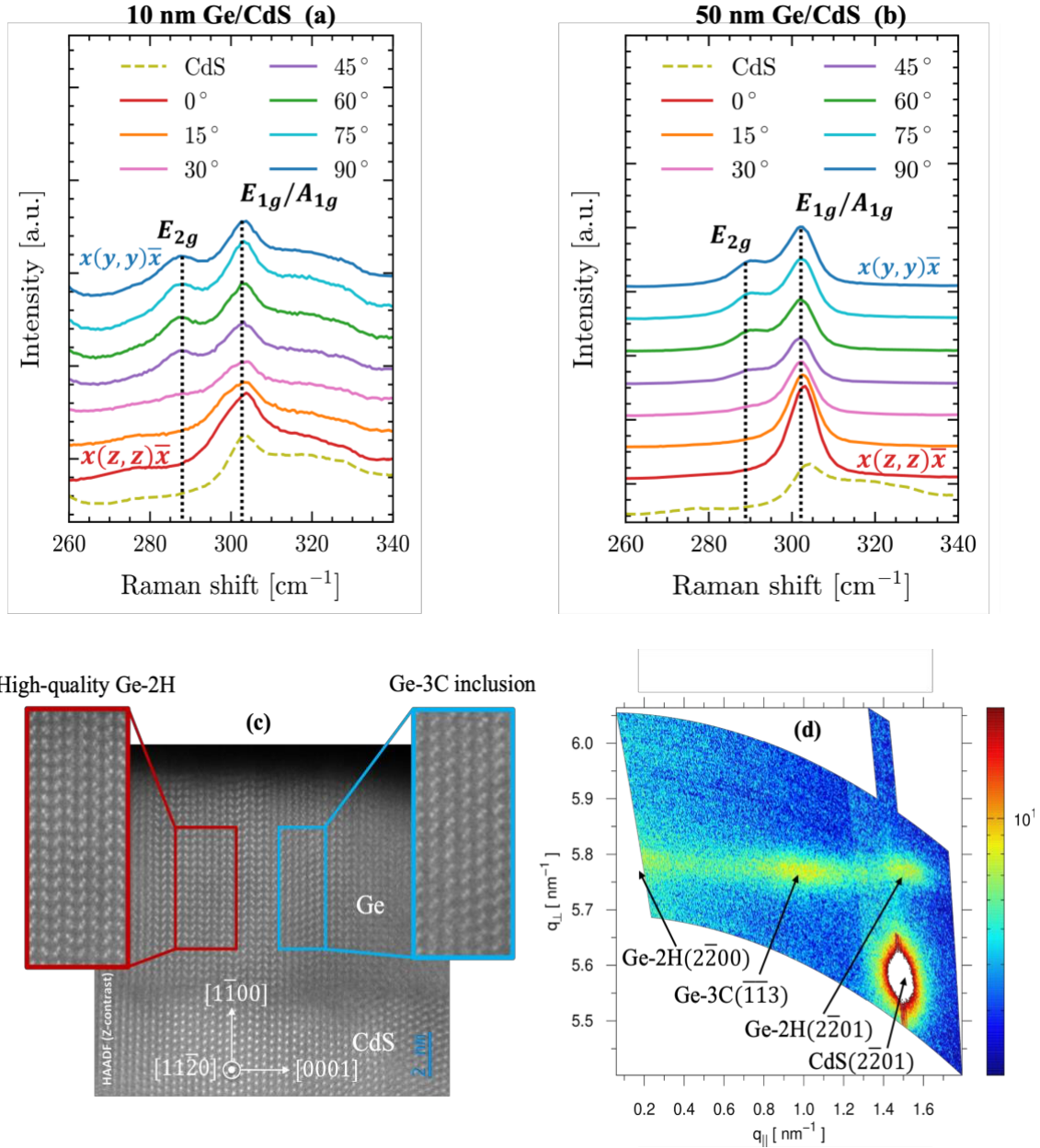


Fig.1 (a) – (b) Polarized Raman spectra of the 10 and 50 nm-thick Ge/CdS samples (grown at 250°C), acquired in different configurations ($x(y,y)\bar{x}$ and $x(z,z)\bar{x}$ corresponding to 90° and 0°, respectively). The E_{1g}/A_{1g} mode arises from the combined contributions of Ge-2H, Ge-3C, and the CdS substrate, whereas the E_{2g} mode is attributed exclusively to Ge-2H, therefore representing a Ge-2H *fingerprint*. **(c)** High-angle annular dark-field scanning TEM cross-section of the 10 nm-thick Ge/CdS sample, showing the epitaxial relationship between Ge-2H and the CdS substrate. Inclusions of Ge-3C are also visible at this scale. **(d)** HR-XRD reciprocal space map of the 50 nm-thick Ge/CdS sample around the CdS and Ge-2H($2\bar{2}01$) Bragg peaks, showing also the presence of the Ge-3C ($\bar{1}13$) Bragg peak at comparable intensity. Towards $q_{\parallel} \sim 0$ some intensity from Ge-2H ($2\bar{2}00$) can be observed.

Beyond Bulk: Interface-Driven Dopant Physics in Ultrathin Silicon-on-Insulator

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Silicon-on-insulator (SOI) offers a CMOS-compatible platform for advanced nanoelectronic devices, from ultra-low-power to unconventional applications.[1] While bulk Si doping is well established, dopant incorporation and ionization in Si nanostructures remains widely unexplored. Beyond device integration, SOI provides a controllable platform to probe 2D-confined Si films.

This work investigates ex-situ doping of ultrathin SOI films with thickness (H_{SOI}) ranging from 8 to 30 nm, using a mild bottom-up approach based on P-terminated polymers (**Fig.1**).[2,3] For $H_{SOI} \sim 30$ nm, dopant ionization and transport properties closely match those of bulk Si,[4,5] indicating nearly complete dopant activation. At room temperature, for $H_{SOI} < 30$ nm, carrier concentration and mobility is significantly reduced and progressively deviate from bulk values, revealing an increasing interface-driven dopant behavior (**Fig.2**).[6]

Electron paramagnetic resonance (EPR) and capacitance-voltage (CV) measurements identify non-passivated interfaces states at the SiO₂/Si interface. These traps create depletion regions in the device layer, reducing the effective conductive thickness (H_{eff}) and enhancing Coulomb scattering. Even at high P concentration ($n_D \sim 6 \times 10^{18} \text{ cm}^{-3}$), an unexpected semiconductor behavior emerges at low temperature, associated with a significant increase in activation energy (E_a) of the dopant due to the dielectric mismatch between Si and SiO₂. [7] At lower n_D and H_{SOI} , the reduction of H_{eff} is more pronounced, hence inducing significant quantum confinement effects. The combined effect of electrostatic-induced confinement and dielectric mismatch lead to an increase of E_a to 175 meV (**Fig.3**). By engineering the SiO₂/Si interface through thermal oxidation (RTO) and chemically grown SC2-SiO₂ capping, we demonstrate that interface quality control dopant ionization rather than bulk statistics and achieve controlled tuning of electrostatic confinement and dopant activation.

These results demonstrate that in ultrathin SOI, dopant physics transition from bulk to interface-limited, providing new routes to engineer carrier transport and controllable metal-insulator transition regimes in 2D Si nanostructures.

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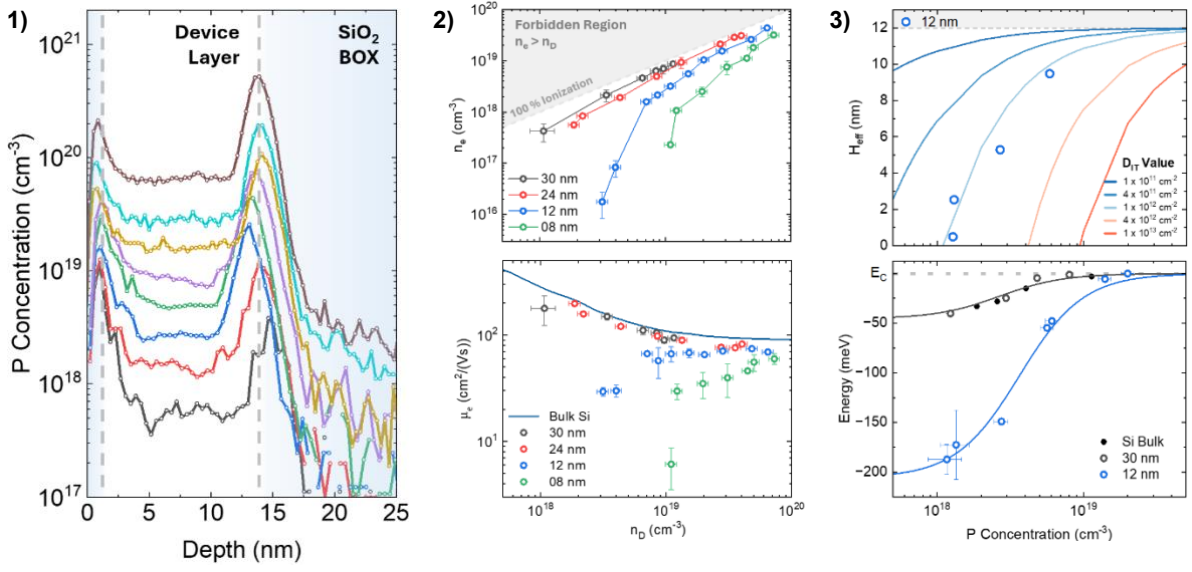


Fig. 1. ToF-SIMS P depth profiles of ultrathin SOI samples with $H_{SOI} = 12 \pm 1$ nm.

Fig. 2. Carrier concentration (n_e , top) and mobility (μ_e , bottom) vs the total dopant concentration (n_D) for SOI samples with different H_{SOI} .

Fig. 3. Effective conductive thickness (H_{eff} , top) and activation energy (E_a , bottom) obtained in the SOI samples with $H_{SOI} = 12 \pm 1$ nm.

W-Center Defects in Crystalline Silicon: Electronic Structure and Optical Signatures

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Controlling the quantum properties of individual fluorescent defects in silicon is a central challenge for the development of scalable quantum photonic technologies. To date, research has predominantly focused on extrinsic impurity-based colour centres incorporated into the silicon lattice. In this work, we investigate the electro-optical properties of intrinsic luminescent defects in crystalline silicon associated with the tri-interstitial W-center. Using first-principles density functional theory, the microscopic configuration of the W-center, a trigonal tri-interstitial vacancy complex (I_3-V), reproduces all key experimental signatures, including emission energy, donor levels, symmetry, vibrational characteristics, and thermal stability, while exhibiting lower formation energy and enhanced optical transition strengths compared to previously proposed structures [1,2]. Advanced TB-mBJ electronic structure calculations reveal defect-induced states within the silicon bandgap for the first time, enabling Coulomb-mediated excitonic radiative recombination below the band edge. We further examine the influence of disorder on W-center formation and optical response, providing a comparative analysis of defect generation mechanisms. These results establish intrinsic silicon defect centers as efficient quantum emitters compatible with integrated photonic platforms, highlighting their potential for waveguide-coupled light sources and scalable silicon-based quantum communication and photonic technologies.

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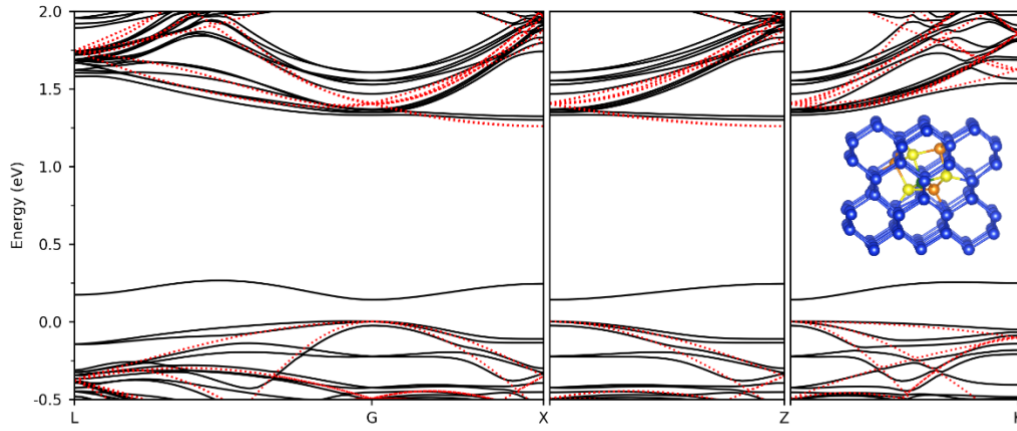


Fig. 1. Electronic band structure of the W-center defect in a $3 \times 3 \times 3$ Si supercell (216 atoms). Black solid lines represent the neutral defect configuration, while red dotted lines correspond to pristine bulk Si for comparison. All energies are referenced to the valence band maximum (VBM). In the structural inset, yellow spheres denote the defect atoms, whereas the orange and green spheres indicate the surrounding Si atoms displaced due to the I_3-V defect configuration.

Admittance spectroscopy of organic-silicon heterojunction structures fabricated with ultrasound assistance

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Organic–silicon hybrid structures are promising for next-generation photovoltaics due to high carrier mobility and scalable fabrication. PEDOT:PSS/Si heterojunctions enable low-temperature processing and tunable interfacial energetics [1]. Because defects govern their electronic properties, their characterization and control are essential. Here, admittance spectroscopy [2] is employed to probe defect states, and acoustic waves are used for defect engineering.

The n-Si/PEDOT:PSS structures were fabricated by silicon substrate cleaning, spin-coating of the organic layer, room-temperature relaxation, annealing at 140 °C, and contact evaporation. Film thickness and interfacial quality were tuned by varying the spin-coating speed and relaxation time. Ultrasound treatment (UST) was applied during relaxation of some samples, using primary waves at 2.5 MHz or radial waves at 500 kHz.

The interfacial trap density of states (tDOS) was evaluated using the Walter formalism [2] based on capacitance–frequency measurements (100 Hz–1 MHz) at bias voltages of 0 and 0.4 V. The trap emission prefactor ($4.3 \pm 0.2 \cdot 10^4 \text{ s}^{-1} \text{ K}^{-2}$) was extracted from temperature-dependent data in the range of 220–300 K (Fig. 1a). Defect states were resolved by Gaussian decomposition of the defect-related signal, with energy levels determined from peak positions and relative contributions quantified from area fractions (Fig. 1b).

Reducing the organic layer thickness by increasing the spin-coating speed slightly decreases the total defect density (Fig. 2). Forward bias increases the detected defect population due to enhanced contributions from deeper trap states (Figs. 2 and 3). UST has little effect on the absolute defect density but significantly reshapes the energy distribution by promoting deeper trap states, particularly under radial-wave excitation (Fig. 3). Although prolonged relaxation favors deeper levels, UST narrows the defect energy distribution. Overall, acoustic-wave-assisted fabrication enables effective defect engineering in organic–silicon hybrid structures.

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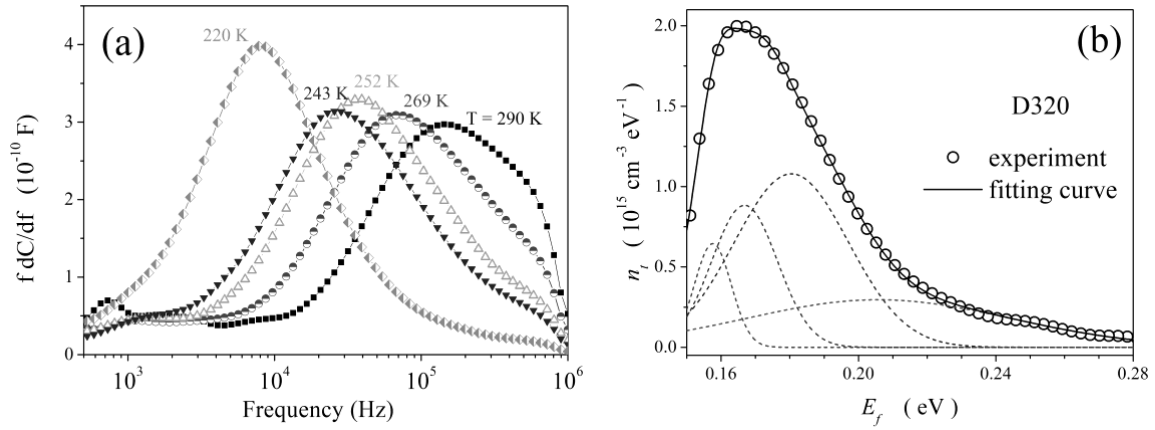


Fig. 1. (a) Frequency dependence of the capacitance derivative of the PEDOT:PSS/Si structure at different temperatures. (b) Representative Gaussian decomposition of the tDOS energy spectrum. Symbols denote experimental data, dashed lines correspond to individual defect contributions, and the solid line represents the cumulative fit.

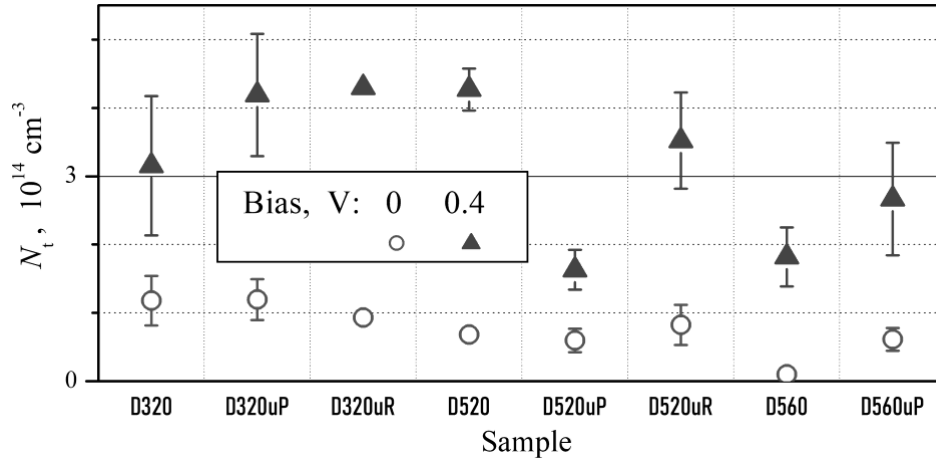


Fig. 2. Total tDOS determined at different bias voltages for samples fabricated under various processing conditions. In the sample notation, the first digit denotes the spin-coating speed, where 3 and 5 correspond to 3000 and 5000 rpm, respectively, and the following two digits indicate the room-temperature relaxation time in minutes. Suffixes specify ultrasonic treatment, with “uP” denoting primary waves and “uR” denoting radial waves.

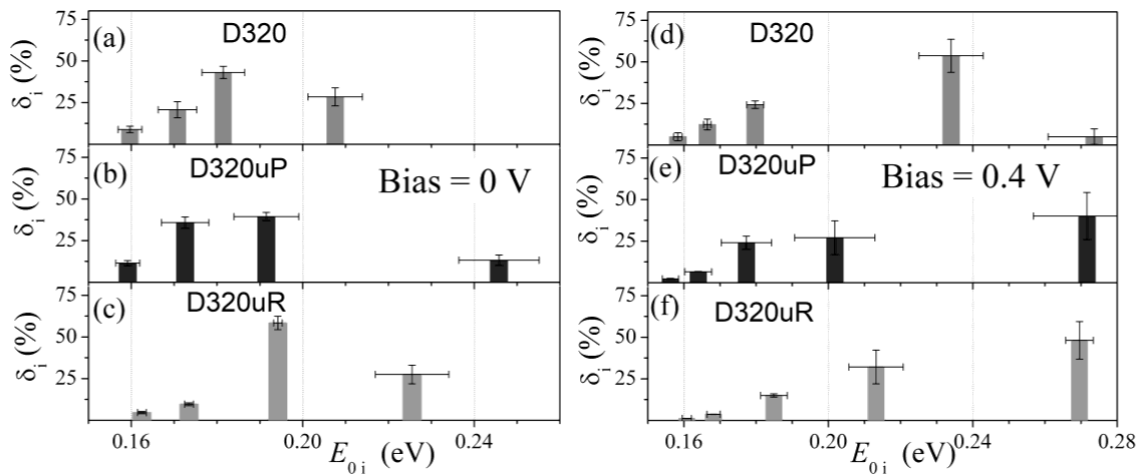


Fig. 3. Contributions of different defect types as a function of energy at bias voltages of 0 V (a–c) and 0.4 V (d–f). Data are shown for samples fabricated at a spin-coating speed of 3000 rpm with a 20 min room-temperature relaxation time: (a, d) without ultrasound treatment; (b, e) under primary-wave excitation; and (c, f) under radial-wave excitation.

Comparative study of void defect annihilation in Si (100) and Si (110) wafers during high-temperature rapid thermal processing

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(100)-oriented Si wafers are widely used as semiconductor substrates, while (110)-oriented wafers are attracting attention for manufacturing advanced logic devices because of their potential to enhance carrier mobility [1]. We previously established a rapid thermal process (RTP) in an oxidizing ambient above 1300 °C to improve the quality of Czochralski Si wafers [2], in which oxidation-induced self-interstitial injection from the SiO₂/Si interface promotes void annihilation. Although these point-defect behaviors have been discussed for Si (100), these behaviors remain unclear in other orientations; therefore, we investigate void annihilation in Si (110) during an oxidizing RTP. P-type (B-doped) Si wafers with (100) and (110) orientations, 300 mm in diameter, were prepared. The oxygen concentrations (old ASTM standard) were $9.3 \times 10^{17} \text{ cm}^{-3}$ and $9.1 \times 10^{17} \text{ cm}^{-3}$ for Si (100) and Si (110), respectively, while the corresponding nitrogen concentrations were $3.5 \times 10^{14} \text{ cm}^{-3}$ and $3.1 \times 10^{14} \text{ cm}^{-3}$. The RTP was conducted at 1350 °C for 10 s with O₂ partial pressures (Ar dilution) of 1%, 25%, and 100%. After conducting the RTP and repolishing, surface crystal void densities were measured using a KLA-Tencor Surfscan system, as shown in Figure 1 [3]. Without the RTP, void densities of both Si (100) and Si (110) wafers exceeded 100 cm⁻². For Si (100), the void density decreased as the O₂ partial pressure increased, consistent with higher oxidation rates enhancing self-interstitial injection and accelerating void annihilation. In contrast, for Si (110), the void density showed no clear dependence on O₂ partial pressure. Nevertheless, under 1% O₂, Si (110) exhibited a lower void density than Si (100), indicating more effective void annihilation in the former under low-oxygen conditions. These results demonstrate that the oxidation-induced point-defect behavior depends strongly on the orientation.

Acknowledgement:

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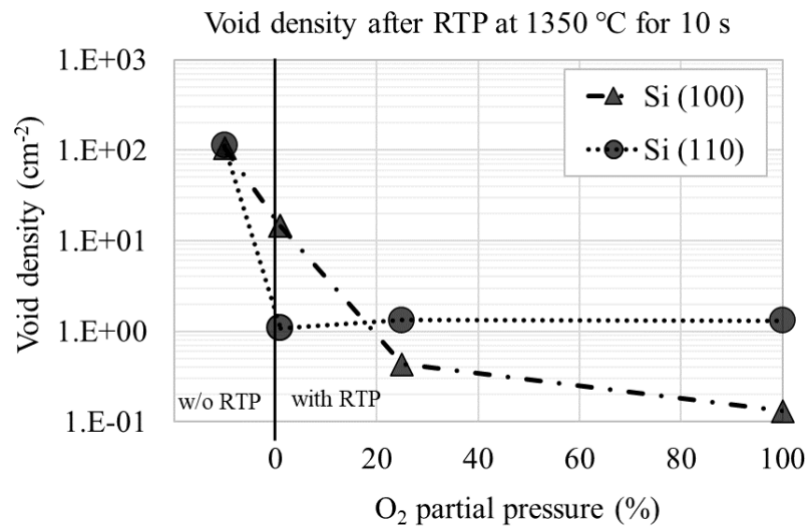


Fig. 1. Impact of O₂ partial pressure during RTP on void density.

Controlled Copper Precipitation for Rapid Point Defect Characterization in Near-Perfect Czochralski Silicon

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High-quality 300 mm near-perfect Czochralski (CZ) silicon wafers are crucial for advanced semiconductor devices, yet characterizing their residual nanoscale point defects—such as vacancies, self-interstitials, and oxygen-related complexes—remains challenging due to the limitations of conventional methods like precision polishing and high-cost scanning tools. This study introduces a rapid technique leveraging controlled precipitation of supersaturated copper (Cu) impurities to decorate and reveal native defects in ultra-pure silicon. By modulating Cu supersaturation through contamination temperature (800°C or 1000°C) and cooling rate (air cooling), heterogeneous nucleation is confined to intrinsic defect sites, avoiding homogeneous precipitation that obscures defect distributions in earlier methods. Higher introduction temperatures yield elevated near-surface Cu concentrations, promoting characteristic precipitate morphologies: asterisk-like structures in self-interstitial-dominant regions (ejecting Si atoms to enhance branching) and line-type or cruciform shapes in vacancy-dominant environments (where vacancies compensate ejected Si, favouring directional growth). Surface precipitation dominates due to steep Cu gradients, while sub-surface (~120 μm depth) precipitates emerge only at sites with lower nucleation barriers, such as point defect aggregates or large oxygen precipitates, indicating excess point defects when present. Pre-annealing treatments (short-time or full) dissolve native defects, shifting precipitate size, density, and uniformity, further validating the role of defect size in modulating critical Cu thresholds. This cost-effective approach enables qualitative identification of point defect types via precipitate presence and morphology, with potential for semi-quantitative assessment through finer Cu dose and cooling control, accelerating defect engineering and crystal growth optimization in advanced monocrystalline silicon manufacturing.

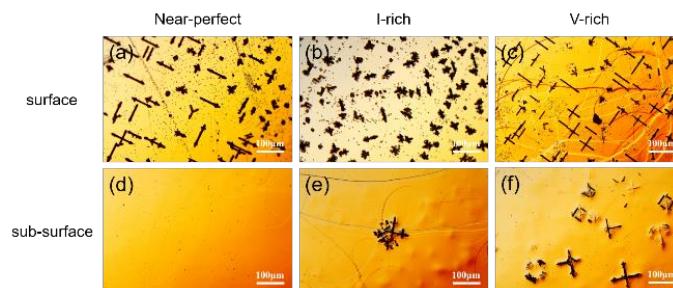


Fig. 1. OM images of Cu-decorated precipitates in near-perfect (a), I-rich (b), and V-rich (c) regions

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DFT Analysis of Gettering in Si Wafers for CMOS Image Sensors

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Extremely high gettering capability for removing metallic impurities (M) is crucial for fabricating Si wafers for CMOS sensors [1]. Recently, a new concept has been proposed for the development of Si wafers that outperforms those fabricated with the conventional gettering technique using dopants (D) or oxygen precipitates. Specifically, Si wafers treated with hydrocarbon cluster ion implantation [1] and those subjected to ultra-high-temperature rapid thermal processing (RTP) [2] have attracted growing attention. However, little is understood about the gettering mechanisms involving a carbon (C) -self interstitial Si (I) complex (CI) and a vacancy (V) -oxygen (O) complex (VO) that are presumed to be introduced by hydrocarbon cluster ion implantation [1] and ultra-high-temperature RTP [2], respectively.

In this study, first-principles calculations based on density functional theory (DFT) were used to evaluate the interactions between various gettering sites and M , which spans a broader range. The gettering sites considered were three dopants (B, P, and As) [3], CI and CIO defects, and a VO defect, in particular VO_4 . Twelve M (Ti, Cr, Mn, Fe, Co, Ni, Cu, Zn, Mo, Hf, Ta, and W) were considered. A 64-atom model (Fig. 1), obtained by expanding the conventional unit cell to a $2 \times 2 \times 2$ supercell, was primarily used, while models up to 1000 atoms were also employed for some calculations. The Si crystal symmetry was considered to select all the independent interstitial T- and H-sites for the positions of M (Fig. 2). The ultrasoft pseudopotential method was employed, with the generalized gradient approximation (GGA) based on the PBE functional for the exchange-correlation energy. The dependence of the binding energy (E_b) between the gettering site and M on their distance was investigated extensively. The calculated E_b of 0.50 eV for a B-Fe pair (0.25 eV for a B-Ni pair) was used as the lower (upper) bound for the presence (absence) of gettering.

The main results are summarized in Table 1. The results for dopant-induced gettering revealed that M is not always most stable at the nearest-neighbor site to the dopant. In the B-Zn pair, for example, Zn was most stable at the fourth-nearest-neighbor T-site (T_{4b}) of B with a Si atom located between B and Zn. The results obtained using the 1000-atom model suggest that B-induced gettering of Cu occurs up to approximately 20 Å from B. For CI type defects, the CI -Fe pair exhibited E_b of 1.09 eV, which was approximately twice that for B-induced gettering and comparable to the value reported in a previous study [3]. The superior Fe gettering ability of CI compared with B is attributed to C being highly negatively charged. Furthermore, the E_b of the CIO -Fe pair is 0.54 eV, which is approximately half that of the CI -Fe binding energy. The latter result explains the experimental finding [1] that the gettering ability decreases when CI transforms into a CIO defect in Czochralski-grown Si.

The calculated results for VO defects will be presented at the conference.

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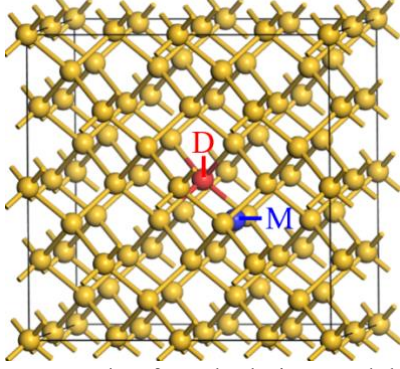


Fig. 1. Example of a calculation model including *D* (red) and *M* (blue) at a T-site in a 64-atom Si supercell.

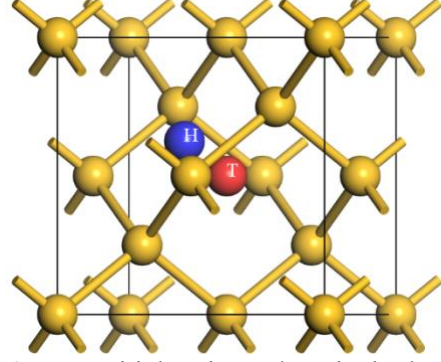


Fig. 2. Interstitial T-site and H-site in the Si 8-atom model.

Table 1. Summary of maximum E_b (eV) and stable sites in 64-atom model.

T_N and H_N denote the Nth nearest T-site or H-site from the dopant at which E_b maximizes.

	Ti	Cr	Mn	Fe	Co	Ni	Cu	Zn	Mo	Hf	Ta	W
B	0.97	0.57	0.66	0.50	0.49	0.25	0.84	0.53	0.48	0.97	0.96	0.61
	T_1	T_1	T_1	T_1	T_1/H_1	T_1/H_1	T_1	T_{4b}	T_1	T_1	T_1	T_1
P	0.24	-0.01	0.15	0.46	0.78	0.14	0.25	0.02	0.01	0.22	0.43	0.02
	T_2	T_2	T_2	T_2	T_1	T_{4b}/H_{5g}	T_{4b}	T_{4b}	T_2	T_2	T_2	T_2
As	0.22	-0.01	0.15	0.35	0.64	0.20	0.28	-0.03	-0.01	0.20	0.37	-0.04
	T_3	T_6	T_6	T_3	T_3/H_3	T_{4b}/H_{5g}	T_{4b}	T_{4b}	T_6	T_5	T_6	T_6

	Fe	Co	Ni	Cu
<i>CI</i>	1.09	1.14	0.73	0.77
<i>CIO</i>	0.54	0.69	0.59	0.40

Doping Engineering of Double-SOI Structures for Two-Channel Tunneling Transistors

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In response to the increasing demand for ultra-low energy consumption in electronic devices, novel transistor architectures beyond conventional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) designs are required. We propose a field-effect nanotransistor based on lateral resonant tunneling between two parallel conduction channels [1]. In this architecture, one channel is selectively coupled to the source contact, while the other is selectively coupled to the drain contact. As a result, a source–drain current can flow only when tunneling transport between the two channels is enabled, providing a fundamentally different operating mechanism compared to a conventional MOSFET. This concept can be experimentally realized by double SOI substrate, consisting of two separated crystalline Si layers on SiO₂ insulators [2]. One critical step is to selectively dope the source and drain regions, which are located in the top Si and lower Si layers, respectively, with ultra-high concentration ($>10^{19}$ cm⁻³). The challenge is that both Si layers are only 2-5 nm thick, thus lacking re-crystallization seed after ion implantation. To prevent full amorphization of the Si layers we apply both room and elevated temperature (200–400 °C) during implantation and demonstrate defect-free, highly doped S/D regions in those thin Si layers. Results of both implant methods as well as numerical (TCAD) simulations of the expected doping profiles are being compared and the final solution will be presented.

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Electric Field Distribution in Black Silicon Needles Under Reverse Bias: A TCAD Simulation Study

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Black silicon (b-Si) – a nanotextured silicon surface in the dimensions below the wavelength of incident light – is an attractive absorption-enhancing surface treatment for high-field silicon photodetectors such as avalanche photodiodes (APDs). However, the behavior of its high-aspect-ratio nanoscale needles under high reverse bias remains poorly understood. While earlier b-Si simulations have primarily focused on equilibrium field-effect passivation [1], [2] – how fixed charges in Al₂O₃ repel carriers from needle surfaces – the redistribution of electric field under applied reverse bias and its implications for leakage, trap-assisted generation, and breakdown have not been systematically studied. We present a simulation study examining how b-Si needle geometry governs electric field enhancement and localization under high reverse bias.

TCAD simulations with b-Si geometries (width, height, pitch) extracted from SEM images (Fig. 1a) are used to study how reverse bias redistributes the field in and around the b-Si layer under realistic substrate doping and Al₂O₃ passivation with fixed interface charge. Initial results (Fig. 1b) reveal two distinct regimes: at zero bias, field localization is dominated by the fixed Al₂O₃ charge, creating hotspots at needle tips and inter-needle valleys, but surprisingly under high reverse bias, the sub-array bulk field increases by several orders of magnitude while the field inside the needle bulk remains comparatively low. Notably, the peak field is spatially confined to discrete regions just below the inter-needle valleys rather than distributed uniformly, identifying these regions as the likely sites for microplasma formation and trap-assisted leakage current.

We will present a systematic study of varying needle geometry – width, height, and pitch – to map how the transition from a planar to a nanostructured surface drives field localization under bias. These findings will be discussed in the context of experimentally fabricated b-Si APDs, where the identified field localization mechanisms directly impact avalanche uniformity, breakdown onset, and dark current.

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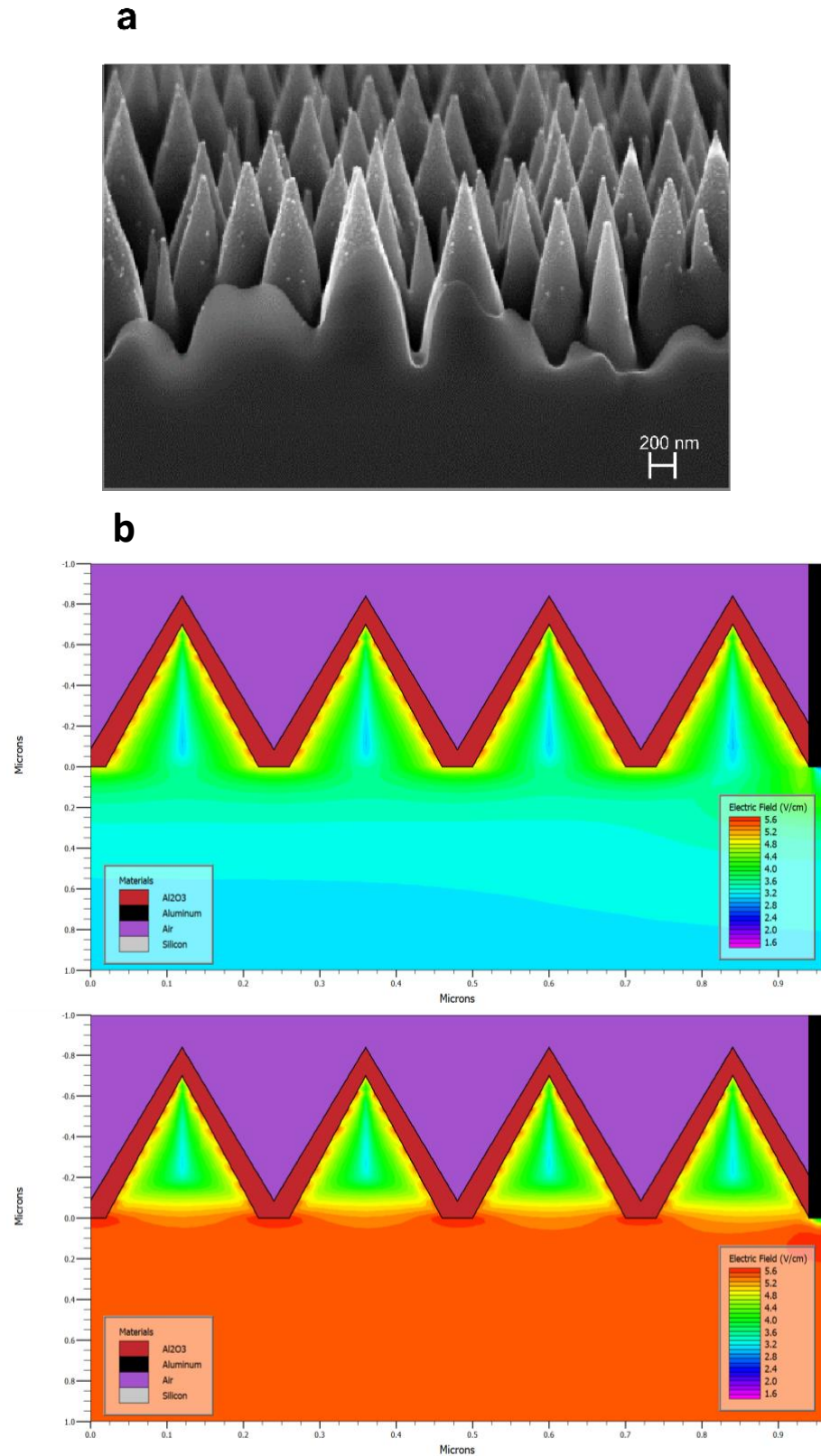


Fig. 1. (a) SEM image of black silicon nanotexture used as an example from [1], with needle dimensions matching those used in simulations. (b) TCAD simulated electric field magnitude ($\log_{10}|E|$) of a b-Si array under 0 V (top) and 100 V (bottom) reverse bias. Increased reverse bias affects the field distribution below the b-Si array but not inside the needle bulk. The simulated structure consists of a b-Si needle array (base width: 200 nm, height: 700 nm, pitch: 240 nm) on 5 μm thick high-resistivity n-type ($1\text{ k}\Omega\cdot\text{cm}$) silicon and an Al₂O₃ passivation layer with fixed interface charge density $Q_f = -2.5 \times 10^{12}\text{ cm}^{-2}$. Note x-y axes are not to scale.

Electrical and Optical Properties of Defect-Enhanced SiGe Heterostructures

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Defect engineering offers a pathway to modulate the electronic and optical properties of group-IV semiconductor heterostructures beyond traditional strain and composition design. Here, we investigate the impact of self-split interstitial (SSI) defects in $\text{Si}_{1-x}\text{Ge}_x$ alloy supercells using density-functional theory (DFT). Several alloy compositions and supercell sizes ranging from 128 to 432 atoms are employed to systematically analyze the evolution of the electronic band structure, band edge modification, emission and absorption characteristics in the presence of interstitial defects. In all supercells, the introduction of the Ge–Ge [110] split self-interstitial leads to the emergence of characteristic defect-related electronic states [1,2]. Specifically, two defect-induced valence bands appear above the pristine VBM, while one defect-induced conduction band is formed below the CBM. Although this qualitative feature is common to all supercell sizes, the dispersion, energetic separation, and hybridization of the defect-related bands depend strongly on the underlying lattice symmetry of the supercell. The 128 and 251-atom supercells are both constructed on FCC lattices and therefore exhibit qualitatively similar band dispersions and defect-defect interactions. In contrast, the 217-atom supercell is based on a SC lattice, resulting in a distinct Brillouin-zone topology and symmetry environment. Therefore, the defect-related bands in the 217-atom supercell exhibit weaker defect-defect hybridization and appear significantly flatter and more isotropic in dispersion compared to those in the FCC based 128 and 251 atom supercells. These differences arise primarily from symmetry-induced changes in band folding and defect–host coupling rather than from supercell size alone. The absorption properties calculated by Bethe-Salpeter (BSE) equations show an enhanced peak below the pristine SiGe direct band absorption, which proves that the defect induced bands are optically active and that the insertion of Ge-Ge split-[110] interstitials into crystalline Ge can open up a direct band gap transmission path in SiGe. Our results provide new insights into the defect mediated design of group-IV heterostructures for photonic device applications.

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Electrical Properties of Dislocation-Related Defects in Ge/Si Virtual Substrates

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Group IV heterostructures are key materials for advanced electronic and photonic devices [1-3] and rely on high-quality Ge/Si virtual substrates (VSs) for CMOS-compatible integration [4]. During Ge growth on Si, plastic strain relaxation inherently generates crystalline defects, including misfit dislocations at the Ge/Si interface and threading dislocations (TDs) propagating through the epitaxial layer. These extended defects introduce electronic states within the bandgap and can significantly modify the electrical properties of the material [5]. In this work, we investigate the interplay between threading dislocation density (TDD) and electrically active defects in plastically relaxed Ge/Si (001) epitaxial layers. A sample set with TDD values spanning more than four orders of magnitude (7×10^6 to $2.5 \times 10^{10} \text{ cm}^{-2}$) was analyzed.

Depth-resolved electrochemical capacitance–voltage (ECV) profiling reveals a pronounced carrier concentration peak at the Ge/Si heterointerface, attributed to misfit dislocations, and a nearly constant p-type background throughout the Ge layer. The background concentration decreases with improving crystalline quality and saturates at approximately $1 \times 10^{15} \text{ cm}^{-3}$ for TDD below $1 \times 10^8 \text{ cm}^{-2}$. This saturation indicates a lower limit governed by electrically active defect states and impurity-related complexes formed during growth and thermal processing. [6]. To assess the origin of these states, deep-level transient spectroscopy (DLTS) was performed. The extracted properties of deep levels were correlated with TDD and carrier concentration data, enabling the identification of dislocation-related deep levels and their separation from impurity-related defects, allowing their contribution to the unintentional p-type background doping to be assessed.

This approach enables a deeper understanding of the electrical properties and physical origin of dislocation-related defect states beyond a purely quantitative description of dislocation densities. Understanding the interplay between extended defects and electrically active deep levels supports defect engineering strategies to reduce electrically active states, enabling high-performance Ge-based electronic and photonic devices with improved doping control and device reliability.

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Table 1. Investigated Ge/Si sample set showing the Ge layer thickness, presence of cyclic annealing, and corresponding TDD determined by Secco defect etching.

Ge layer thickness [nm]	Cyclic annealing at 800°C	TDD [cm ⁻²]
120	-	2.5×10^{10}
220	x	6.3×10^9
420	x	3.5×10^8
420	-	7.8×10^9
1170	x	5.0×10^7
1170	-	2.1×10^9
1950	-	1.5×10^9
2315	x	1.7×10^7
7860	x	7.1×10^6

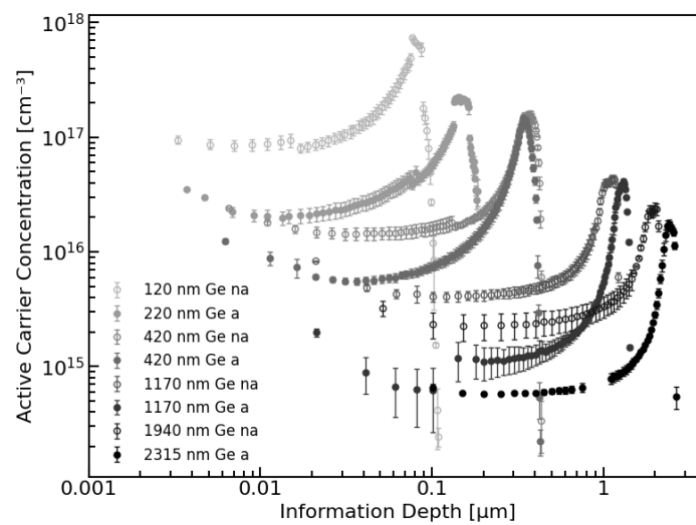


Fig. 1. ECV depth profiles of active carrier concentration in the Ge/Si VS set; a and na indicate annealed and non-annealed samples, respectively

Electrically detected magnetic resonance of telecom-wavelength G and C centers in silicon

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Silicon-based quantum technologies offer a scalable platform for integrated photonics due to their CMOS compatibility and advanced integration [1]. Electrically addressable spin defects in silicon represent a promising building block for scalable spin-photon interfaces. In particular, the G and C centers are spin-active defects that emit in the telecom O-band and L-band, respectively, making them compatible with low-loss fiber-based communication systems.

The first optically detected magnetic resonance (ODMR) on single G centers was reported last year, demonstrating for the first time coherent spin manipulation for this color center [2]. We previously demonstrated optical detection of spin-states in ensemble of C centers using ODMR, combining optical excitation with microwave driving [3]. While ODMR provides direct access to spin polarization and optical transitions, its sensitivity is limited in silicon by weak emission rates and low photon collection efficiency at telecom wavelengths.

Here, we investigate electrically detected magnetic resonance (EDMR) of G- and C-center ensembles in silicon-on-insulator substrates under continuous-wave (CW) microwave excitation and an applied external magnetic field. EDMR monitors microwave-induced changes in device current arising from spin-dependent recombination processes. In systems with efficient recombination pathways, this technique can provide enhanced detection sensitivity compared to optical readout and is naturally compatible with electrical injection and CMOS device architectures.

Our CW-EDMR measurements demonstrate spin-dependent transport in the G- and C-center ensembles, providing a complementary method to ODMR for the investigation of telecom-wavelength spin defects in silicon and laying the groundwork for future electrically integrated spin readout in silicon-based quantum devices.

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Elimination of slip lines induced by the pins in rapid thermal processing for Czochralski silicon wafers

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Czochralski silicon wafers serve as a base material in the integrated circuit industry, whose processing quality directly impacts device yield. By utilizing rapid thermal processing (RTP) to engineer the vacancy concentration distribution within the wafer, followed by subsequent annealing, an internal gettering structure consisting of a denuded zone (DZ) and bulk micro-defects (BMDs) can be formed [1]. Furthermore, in integrated circuit manufacturing, RTP is also employed in processes such as lattice damage repair, impurity profile modulation, and thin-film deposition [2]. Therefore, it is necessary to investigate and control the defects induced by RTP in silicon wafers.

Currently, commercial RTP systems typically adopt a three-pin support method to hold wafers during thermal treatment, which tends to induce slip lines and degrade the wafer's local geometric parameters. This study proposes an optimization strategy involving increased gas flow rate and modified annealing atmosphere to mitigate pin-induced slip lines during RTP. As shown in Fig. 1(a), following normal RTP (Ar, 25 slm), the wafer thickness map of a 300 mm silicon wafer clearly reveals pin-induced slip lines oriented along the $\langle 110 \rangle$ direction. Under the optimized RTP (N₂, 100 slm), however, Fig. 1(b) shows that these slip lines are essentially eliminated. Fig. 2 demonstrates that increasing the gas flow rate and modifying the annealing atmosphere effectively reduce the maximum site flatness least squares range (SFQR), with corresponding wafer information summarized in Table 1. Compared to argon, both nitrogen and oxygen exhibit higher isobaric heat capacity and heat transfer coefficient. Moreover, increasing the gas flow rate enhances forced convection intensity within the chamber. The heat dissipation capacity via forced convection is governed by both atmosphere and flow rate. Complementary numerical simulations further confirm that the optimized process significantly reduces the stress at the pin contact regions.

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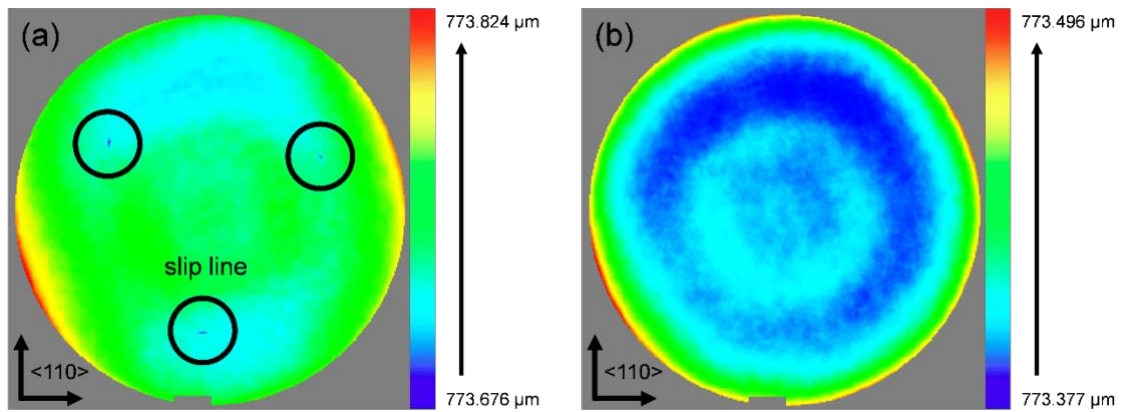


Fig. 1. Wafer thickness map of 300 mm silicon wafer after (a) normal RTP (Ar, 25 slm) and (b) optimized RTP (N₂, 100 slm).

Table 1. Basic RTP process parameters for silicon wafers.

Wafer	Atmosphere	Flow rate (slm)
1	Ar	25
2	Ar	50
3	Ar	100
4	N ₂	25
5	O ₂	25
6	N ₂	100
7	O ₂	100

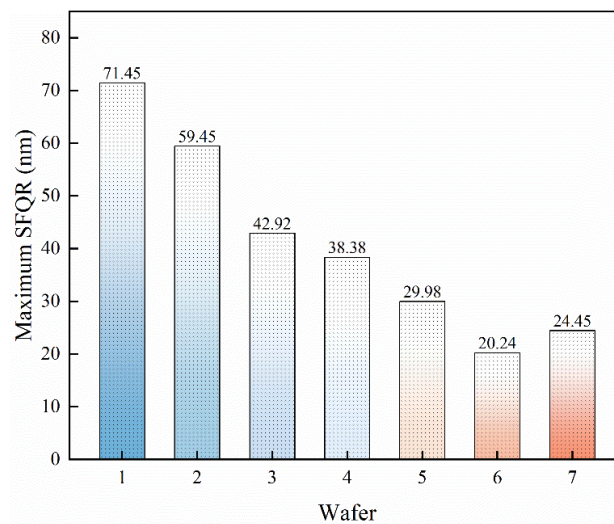


Fig. 2. Effect of atmosphere and flow rate variations on SFQR of silicon wafers.

Engineering Nanostructured Electrodes on Screen-Printed Carbon for Real-Time Monitoring of Nitrogen-Based Water Pollutants

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The monitoring of nitrogen compounds—specifically nitrates, nitrites, and ammonium ions—in water resources is a critical challenge for environmental protection and public health due to their role in eutrophication and potential toxicity. This work presents the development and characterization of portable, low-cost, and highly sensitive electrochemical sensors based on Screen-Printed Carbon Electrodes (SPCEs) modified with engineered nanomaterials and metal oxides. The core of our approach lies in the controlled growth of nanostructures to maximize electrocatalytic activity through defect engineering and surface area optimization. Regarding nitrate (NO_3^-) sensing, we performed electrochemical deposition to grow copper (Cu) micro-crystals and "micro-flowers." The high density of edges and structural defects in these morphologies serves as highly reactive sites for nitrate reduction, achieving a sensitivity of $44.71 \mu\text{A}/\text{mM}$ and a limit of detection (LoD) of $0.87 \mu\text{M}$ [1]. For nitrite (NO_2^-) sensing, a synergistic catalytic layer composed of manganese and copper oxides (MnO_2 and CuO) was developed. The complementary redox properties of these oxides enabled an exceptional sensitivity of $10.83 \mu\text{A}/\mu\text{M}$ and a LoD of $0.071 \mu\text{M}$, maintaining high selectivity against common interfering ions [2]. In addition, for ammonium (NH_4^+) sensing, we explored the integration of conductive polymers (Polyaniline) and gold nanoparticles (AuNPs). The addition of AuNPs enhances charge transfer and conductivity, allowing for a LoD down to $0.01 \mu\text{M}$ via chronoamperometric detection [3].

Detailed structural and morphological characterizations confirm that the electrochemical performance is strictly linked to the nanostructure of the deposited layers [1-4]. These devices offer a robust platform for real-time, in-situ water quality assessment, bridging the gap between advanced materials science and sustainable environmental monitoring technologies. This work was partially supported by the European Union (NextGeneration EU), through the MURPNRR project SAMOTHRACE [GA ECS00000022]. Part of the measurements were carried out in the Italian Infrastructure Beyond-Nano, co-funded by Regione Sicilia (D.D.G. 2929/5S), and by the Italian Ministry of University and Research (Decree 2510/2019). One of the authors (D.C.) acknowledges support from the Ministero delle Imprese e del Made in Italy (MIMIT) under IPCEI Microelettronica 2, project MicroTech_for_Green.

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Epi stacking fault defects in highly doped phosphorus 300 mm crystals

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The increasing demand for low-resistivity ($\leq 1 \text{ m}\Omega\cdot\text{cm}$) 300 mm phosphorus-doped silicon substrates introduces significant challenge in controlling grown-in defects that can trigger epitaxial stacking faults (ESF). These grown-in defects, reported by few authors [1,2], form at high concentration of phosphorus, are probably precipitates involving interstitial phosphorus [1]. This work investigates the combined role of crystal thermal history, resistivity and wafer surface preparation on ESF formation in continuous Czochralski (CCZ) grown crystals. Reconstructed thermal profiles obtained by simulations, were correlated with preferential etching, optical microscope analysis (OM) and laser light scattering (LLS). The study identifies the 550 - 650 °C temperature range as the critical window for defect generation. Prolonged dwell times $\geq 3.8 \text{ h}$ in this range, together with resistivity $< 1 \text{ m}\Omega\cdot\text{cm}$, lead to consistently elevated ESF densities after epitaxy. The presence and morphology of ESF were confirmed by scanning electron microscope (SEM) analysis. In contrast, wafers with even lower resistivity ($0.92 \text{ m}\Omega\cdot\text{cm}$) but a short dwell time ($\sim 1 \text{ h}$) show negligible ESF formation, confirming that high dopant concentration alone is not sufficient to promote defects without adequate thermal budget in the critical temperature range. Pre-EPI surface preparation further affects ESF behavior. Baking in H_2 alone systematically increases ESF counts compared to mixed HCl/H_2 mixing, suggesting different interactions with surface defect sites. Overall, the results highlight that ESF formation is governed by the interplay of dopant concentration, thermal budget, cleaning and baking procedures, rather than any single factor.

To support next-generation 300 mm substrates, optimizing CCZ hot-zone cooling efficiency is essential to minimize dwell time in the critical temperature window and suppress grown-in defect formation along the entire crystal length.

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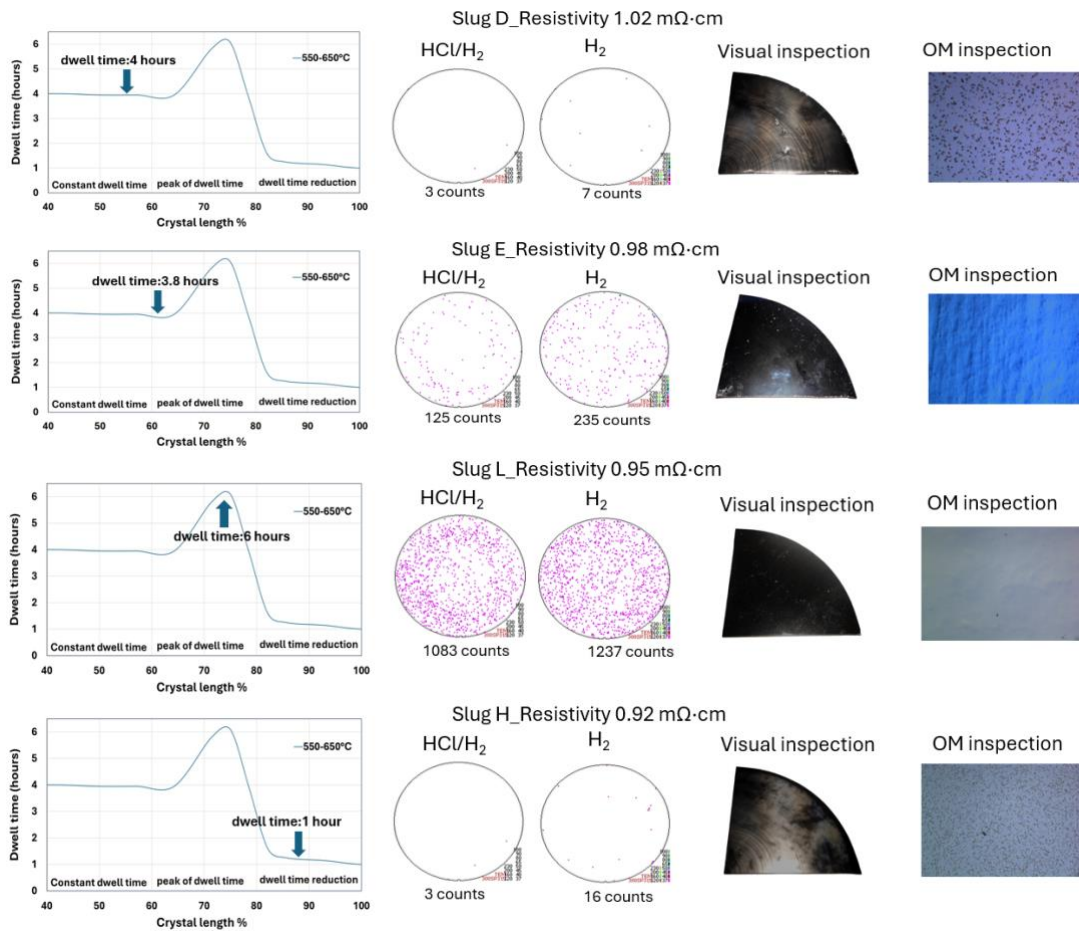


Figure 1: Overall results: ESF in 300 mm wafers with different resistivities (between 1.02 and 0.92 mΩ·cm) from axial positions with different dwell times in the critical temperature range (550-650°C). For each result, the corresponding visual inspection and optical microscope analysis (OM)

Evaluation of impurity effects in magic-angle twisted bilayer graphene by machine learning interatomic potentials

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Twisted bilayer graphene (TBLG) structures represent one of the most interesting platforms in quantum technologies due to their remarkable electronic properties [1]. In particular, magic-angle TBLG, at twisting angle $\sim 1.1^\circ$, has shown an electronic band flattening which enhances electron-electron interactions, paving the way to the exploration of unconventional superconductivity phenomena. From theoretical models, placing impurities inside the graphene sheets, such as vacancies or Stone-Wales defects, can induce flat bands above or below the Fermi level [2]. However, low twisting angles structures are characterized by large Moiré supercells which hinder a systematic study at *ab initio* level. To this purpose, we employed Machine Learning interatomic Potentials (MLIPs), that are capable of reproducing almost *ab initio* accuracy at a fraction of the computational cost. State-of-the-art MLIP software like NequIP [3] have been trained on available carbon-based *ab initio* datasets. The resulting trained models have been tested against both *ab initio* and experimental data and compared to existing interatomic potential foundation models [4]. The scalability of the MLIP approach has been employed to relax low twisting angles (i.e. magic angle 1.05°) systems, where the Moiré supercell includes over 10,000 atoms, facilitating more realistic structures for energy band and density of states calculations. In this work, we relaxed TBLG structures at various twisting angles obtaining different corrugations in the graphene sheets, allowing to investigate the electronic properties of each structure both in presence and without impurities.

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Experimental and simulated investigation of nitrogen shallow donors in Czochralski silicon wafers doped with nitrogen

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Nitrogen is an important technological dopant used in silicon crystal manufacturing. Due to its interaction with vacancies and oxygen in silicon, it is used to control vacancy- and oxygen-related defects. Despite its many advantages, the presence of nitrogen can also have negative effects, such as the generation of shallow donors through the formation of nitrogen-oxygen complexes, including NO, NO₂ and NO₃. However, not all nitrogen-oxygen complexes are electrically active. Therefore, in order to understand the relationship between NO_x complex formation and resistivity changes that may occur in silicon wafers, it is important to understand the formation of nitrogen-oxygen and nitrogen-oxygen vacancy defects, and the relationship between them, as a function of temperature.

We used ab initio calculations and the law of mass action to simulate the equilibrium concentrations of nitrogen-related complexes with oxygen and silicon vacancies. To verify the equilibrium concentrations obtained from the simulations, we carried out annealing experiments at various temperatures for different durations. Finally, we measured the absorption bands at liquid helium or liquid nitrogen temperatures using FTIR spectroscopy. Figure 1 shows a comparison between the sum of the measured and calculated NO_x (x=1–3) complexes. There is good agreement between the experimental results and the calculations. In this article, we will describe how the experimental and calculated results were matched in detail, including how we determined FTIR conversion factors and reaction energies from ab initio calculations.

This work is a result of the BEYOND5 (www.beyond5.eu) project, which has received funding from the ECSEL Joint Undertaking (JU) under Grant 876124. The JU receives support from the European Union's Horizon 2020 research and innovation programme and from France, Germany, Turkey, Sweden, Belgium, Poland, Netherlands, Israel, Switzerland, and Romania. The compute time provided by Gauss Centre for Supercomputing on the JUWELS cluster are acknowledged too.

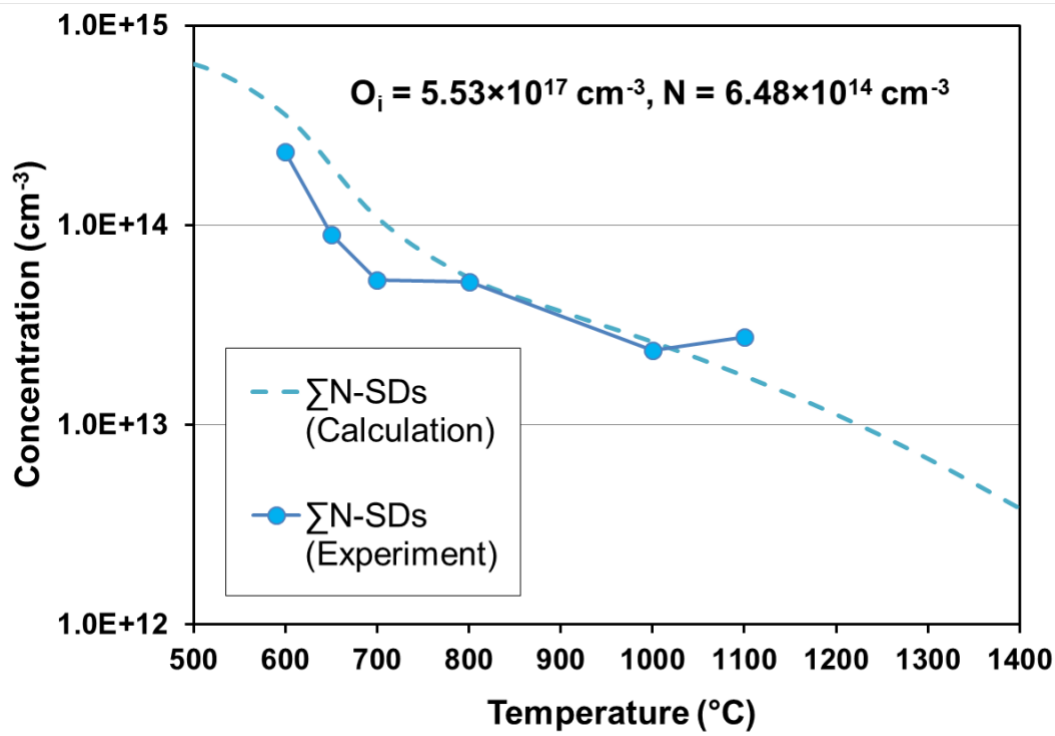


Fig. 1. Sum of NO_x ($x=1-3$) equilibrium complexes obtained from experimental and simulated data

Experimental observation and analysis of gliding I_3 basal stacking faults in hexagonal germanium

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Although in some systems defects are crucial for the realization of optically active group IV semiconductors, in other systems, defects form an obstruction for high quality optical performance. In particular, in direct bandgap 2H-hexagonal silicon germanium (hex-SiGe), the I_3 planar defect is suggested to hold back the realization of high-quality optical devices [1]. In the core/shell nanowire system, in which hex-SiGe is realized most effectively, the nucleation of the I_3 planar defect is found to be inherent to growth front merging, increasing the I_3 planar defect size radially outwards upon shell growth [2,3]. This work highlights a second I_3 planar defect expansion process, taking place post growth [4].

In-situ transmission electron microscopy (TEM) videos of an anneal experiment of a hex-Ge/GaAs core/shell nanowire reveals the perpendicular gliding of the I_3 dislocation line, expanding the I_3 basal stacking fault (**Figure 1**). This process is believed to be driven by the difference in free energy between the 2H hexagonal and 3C cubic crystal phase, favouring an expansion of the I_3 basal stacking fault. Analysis of the propagation trajectories provides the insight that the gliding is determined by dislocation line energy minimization. Furthermore, they suggest a propagation barrier at the core-shell interface. These insights are crucial to anticipate on the different shapes and sizes of the I_3 planar defect in any system, and will be utilized to correlate the optical and electronic properties of hex-SiGe with the I_3 planar defect density, structure and dimensions.

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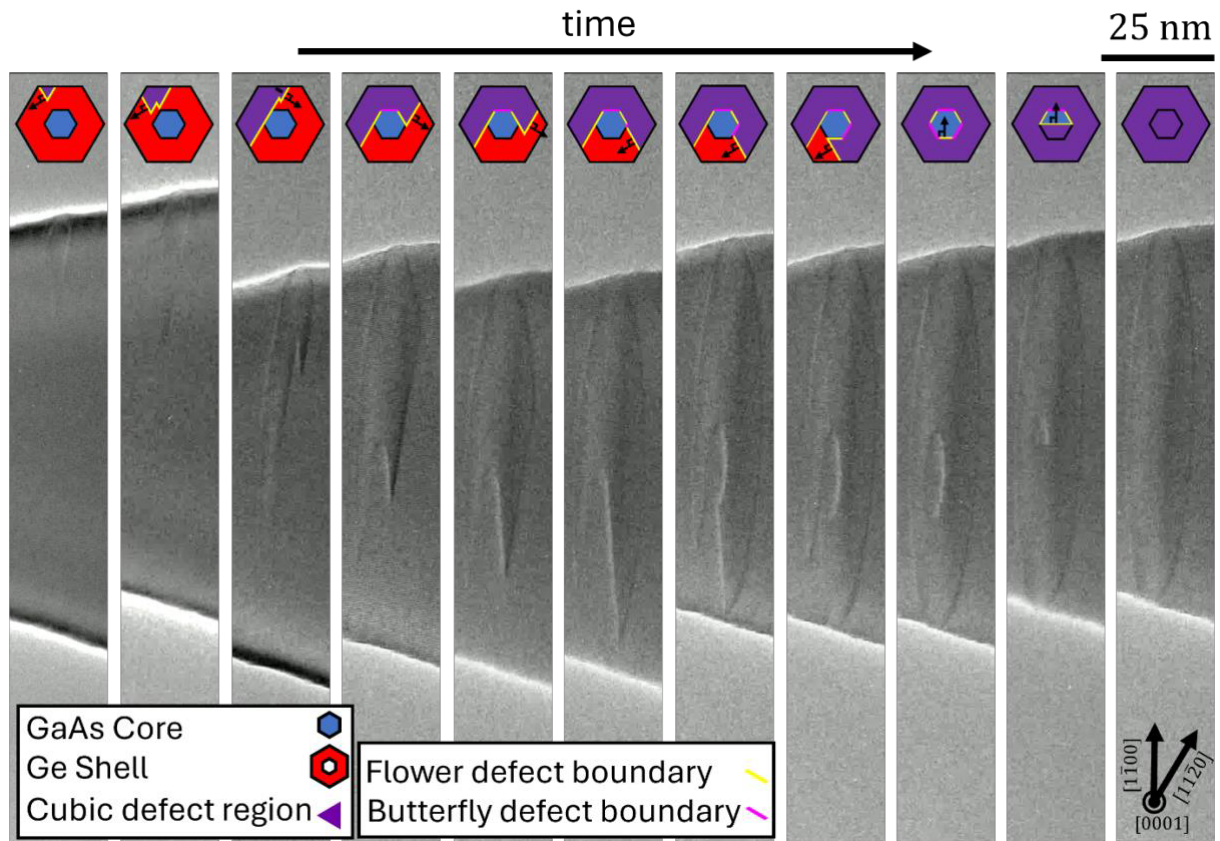


Fig. 1. *In-situ* TEM snap shots of important events during the expansion of an I_3 planar defect. The schematics show the shape of the I_3 basal stacking fault (purple) and propagation direction of the I_3 dislocation line (indicated by the black arrow). The ‘flower’(yellow) or ‘butterfly’(pink) reconstruction of the I_3 dislocation line is highlighted.

Ge-on-Si Substrates with Porous Silicon buffer as Compliant Layer

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The increasing global demand for germanium, particularly for efficient III-V solar cells, necessitates more sustainable solutions as germanium is classified as a critical raw material [1]. Virtual substrates, where germanium is epitaxially grown on silicon or SiGe buffers, present a promising strategy to reduce germanium consumption. The use of porous silicon (PorSi) as a buffer can improve elastic properties and adjust the lattice constant to overcome challenges related to lattice and thermal matching [2,3].

In this study, PorSi layers were fabricated by electrochemical etching of p-type silicon, achieving porosities between 14% and 30%. Various groups (e.g. as-etched, low and high temperature annealing, see Fig. 1) were investigated to analyze the effects on the structure and quality of germanium epitaxy. The SEM pictures in Fig. 1 (left) show clearly the pore growth in PorSi with increasing temperatures driven by vacancy diffusion and Oswald ripening. That goes hand in hand with a change in PorSi lattice constant as indicated by the PorSi peak shift in the rocking curves (right).

For germanium epitaxy, a GeCl₄-based process in an atmospheric pressure chemical vapor deposition (APCVD) reactor is used [4]. Germanium epitaxy on PorSi revealed differences in surface morphology and adhesion, with high temperature annealed samples demonstrating a lower stacking fault density, but also greater susceptibility to delamination. This is demonstrated in Fig. 2 by photographs (2a), SEM (2b) and defect maps (2c) of germanium on 17% porosity porSi. The matt germanium surface after low temperature annealing (Aa) indicates more stacking faults compared to the shiny surface after high temperature annealing (Ba). This is confirmed by the defect maps in (Ac) and (Bc).

Further research aims to minimize the influence of native silicon oxide and to complete defect characterization with TEM and electron channeling contrast imaging (ECCI) to reveal the dislocation density of the samples.

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Fig. 1. SEM micrographs (left) of PorSi with a porosity of 30%. At the top the As-Etched state, followed by PorSi annealed at low temperature in the middle, and PorSi annealed at high temperature at the bottom. The corresponding rocking curves (right) show a change of the PorSi peak position with annealing temperature.

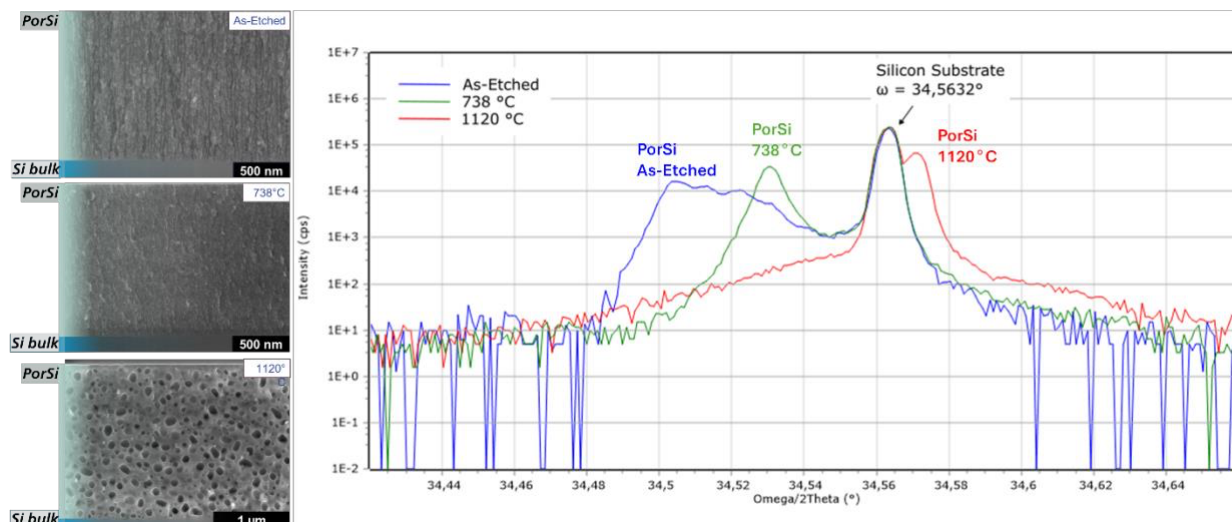
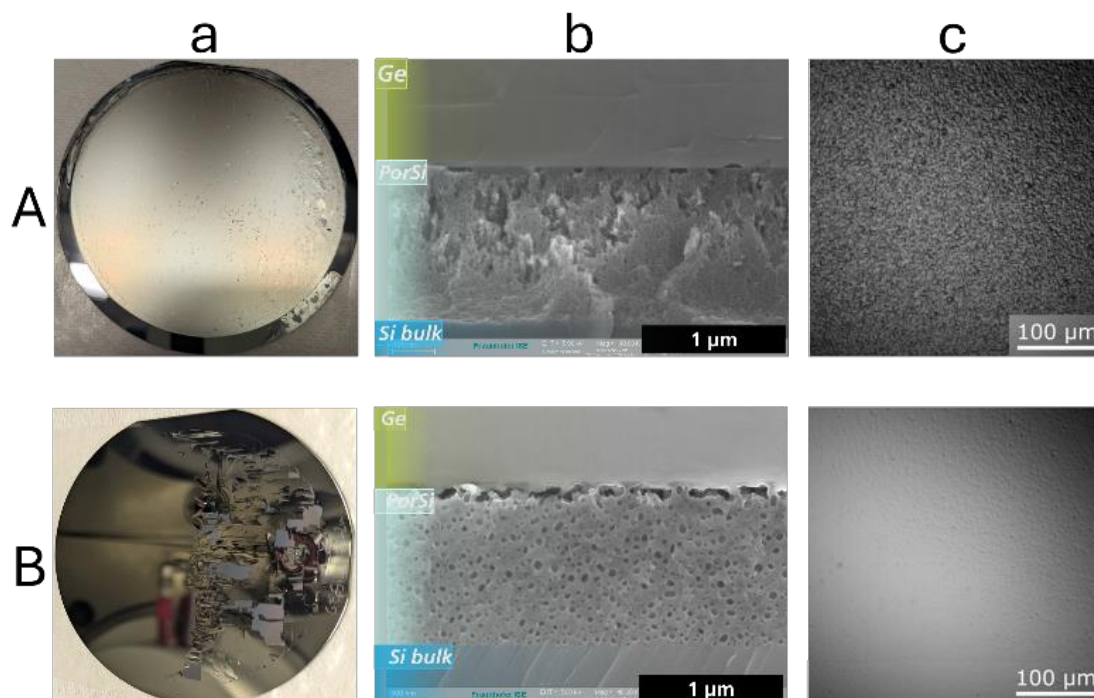


Fig. 2. (a) Photograph, (b) SEM, and (c) defect map of Ge on 17% porosity PorSi. Ge/low temperature annealed porSi (A) and Ge/high temperature anneal PorSi (B). The matt Ge surface after low temperature annealed PorSi (Aa) indicates more stacking faults, which is confirmed by the defect map in (Ac).



Impact of ion charge transport on perovskite solar cells simulated by TCAD Sentaurus

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The industrialisation of perovskite solar cells and their tandem counterparts poses a significant challenge to this technology. One of the main drawbacks so far is their short lifetime under field conditions [1]. One possible degradation mechanism is thought to involve non-reversible ion transport in the perovskite layer towards or into the electron or hole transport layer [2, 3]. To improve our understanding of charged ion transport, we updated our TCAD perovskite solar cell device model [4] to include the transport of both negatively and positively charged ions within the perovskite layer. To achieve this, the *MSC-Hydrogen Transport Degradation Model* is activated in *TCAD Sentaurus*, and anions with a density of $6 \times 10^{16} \text{ cm}^{-3}$ and an ion diffusion coefficient of $5 \times 10^{-10} \text{ cm}^2/\text{s}$ are assumed [5]. Device simulations of perovskite solar cells were carried out to model the dynamics of ion density and current-voltage (IV) curves in response to various sample treatment conditions (Fig. 1) assuming an initial homogeneous ion distribution. The sequence (similar to a possible measurement) without waiting for equilibrium states comprises: dark storage for one day in short-circuit (SC); light ramp to 1 sun within 1 s in short-circuit; ramp to open-circuit (OC) condition within 1 s; a 1 h hold time at open-circuit; and finally, a reverse (V_{oc} to j_{sc}) and forward (j_{sc} to V_{oc}) current-voltage scan within 10 ms. The fast IV scan already shows ion-drift related hysteresis effects for scan times of 10 ms, which are also evident for scan times for 1 s and less in Fig. 2, which confirms similar findings consistent with those reported in Ref. [5]. By incorporating cations into the model, a second time-dependent behaviour can be observed, which can be investigated using fast IV scans (not shown). The derived model, thus improves the understanding of perovskite-based devices using TCAD modeling.

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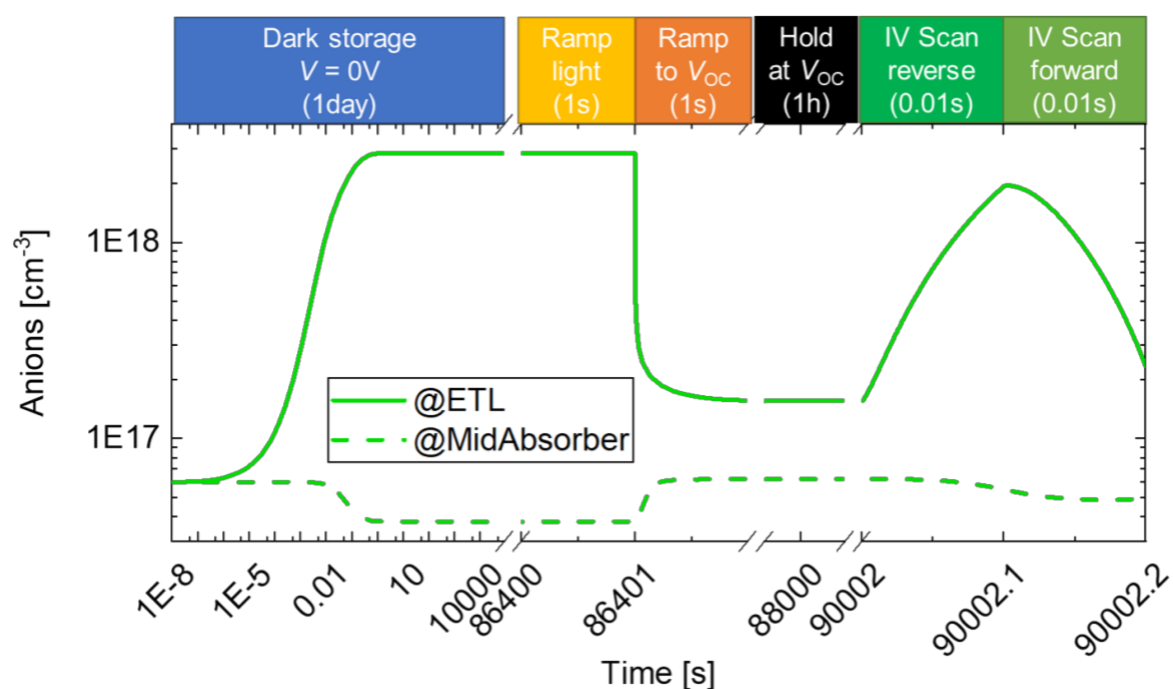


Fig. 1. Simulated anion density in the perovskite layer at the electron transport layer (ETL) and at in the middle of the absorber starting with homogeneously distributed ions. Different sample treatments/measurements are simulated in a transient sequence without waiting for equilibrium states: dark storage for one day in short-circuit, light ramp to 1 sun within 1s at short-circuit, ramp to open-circuit condition within 1s, hold time of 1h at open-circuit, reverse and forward current-voltage scan within 10ms.

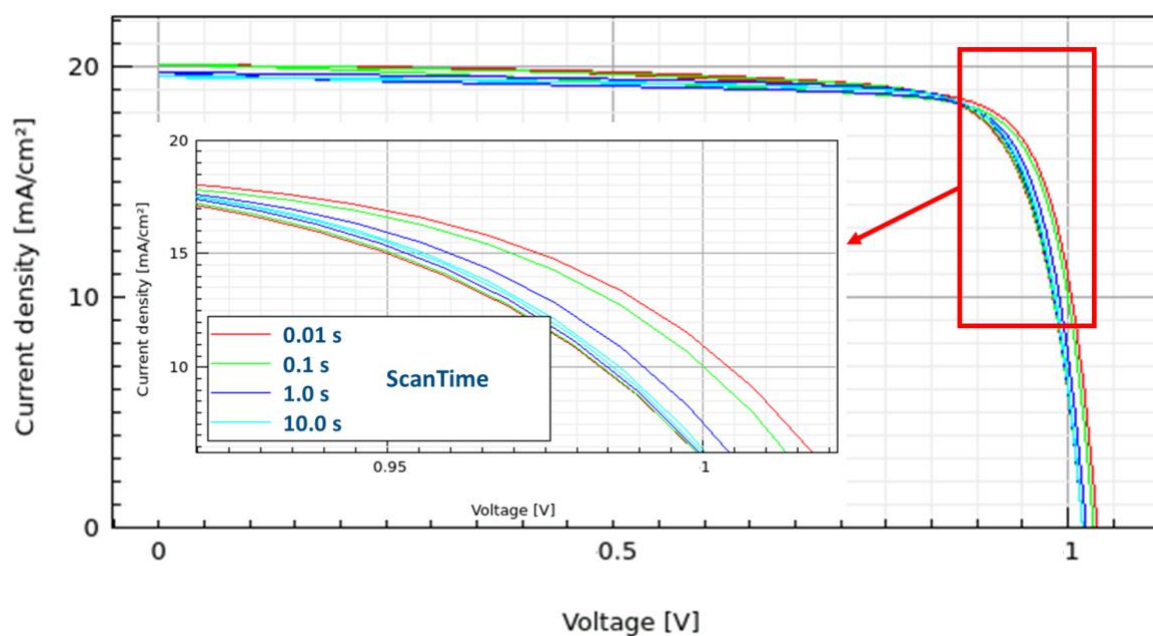


Fig. 2. Simulated current-voltage characteristics at various scan times (voltage rates) showing the influence of moving ions (hysteresis) within the perovskite layer.

Impact of Substrate Carbon Impurities on MOSFET Breakdown Voltage via Enhanced Phosphorus Out-Diffusion in n/n⁺ Epitaxial Wafers

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n/n⁺ epitaxial wafers using heavily phosphorus-doped Czochralski (HP-CZ) silicon as substrates are widely employed in the fabrication of power MOSFETs, and the impurities in the substrate may affect the performance parameters of the MOSFETs. This paper investigates the effect of carbon impurities in HP-CZ silicon substrates on the phosphorus out-diffusion from the substrate during the MOSFET fabrication process. It is found that, compared to the MOSFET devices fabricated on the epitaxial wafers using low-carbon-concentration ($\sim 6.5 \times 10^{15} \text{ cm}^{-3}$, LC) HP-CZ substrates, the mean breakdown voltage (BV) of the MOSFETs fabricated on the epitaxial wafers using high-carbon-concentration ($\sim 3.4 \times 10^{16} \text{ cm}^{-3}$, HC) HP-CZ substrates was significantly lower, and the BV values exhibited a pronounced ring-shaped non-uniform distribution, with lower values at the center and higher values at the edge (as shown in Fig. 1(a)-(b)). Further comparative analysis revealed that this ring-shaped distribution of BV values closely matched the ring-shaped distribution of oxygen precipitates in the HP-CZ substrate (as shown in Fig. 1(c)). Correspondingly, the resistivity of the epitaxial layer on the HC substrate was significantly lower than that on the LC substrate [as shown in Fig. 1(e)-(f)], which can explain the significantly reduced mean BV of MOSFETs fabricated on the epitaxial wafers with HC substrates. Moreover, from Fig. 1(e), it can be seen that the resistivity of the epitaxial layer on the HC substrate increases from the center to the edge, which correlates with the increase in BV values from the center to the edge of the MOSFET devices [Fig. 1(a)]. From Fig. 1(f), it can be seen that the resistivity of the epitaxial layer on the LC substrate shows little variation from the center to the edge, which corresponds to the small variation in BV values from the center to the edge.

During the medium-to-low temperature (700-1000 °C) processes in MOSFET fabrication, for the epitaxial wafers using HC substrates, the high concentration of carbon promotes oxygen precipitation in the HP-CZ silicon substrate. These oxygen precipitates emit a large number of non-equilibrium self-interstitial silicon atoms, which can rapidly diffuse outward the epitaxial layer, significantly increasing the concentration of self-interstitial silicon atoms in the epitaxial layer. In a word, the enhanced oxygen precipitation leads to a higher concentration of self-interstitial silicon atoms in both the substrate and the epitaxial layer, which promotes the out-diffusion of phosphorus impurities from the substrate to the epitaxial layer, reducing the resistivity of the epitaxial layer and consequently leading to a lower BV for the MOSFET devices.

In conclusion, this paper reveals the physical mechanism by which carbon impurities in the substrate of n/n⁺ epitaxial wafers adversely affect the BV of MOSFETs, providing a scientific basis for controlling the carbon concentration in HP-CZ silicon

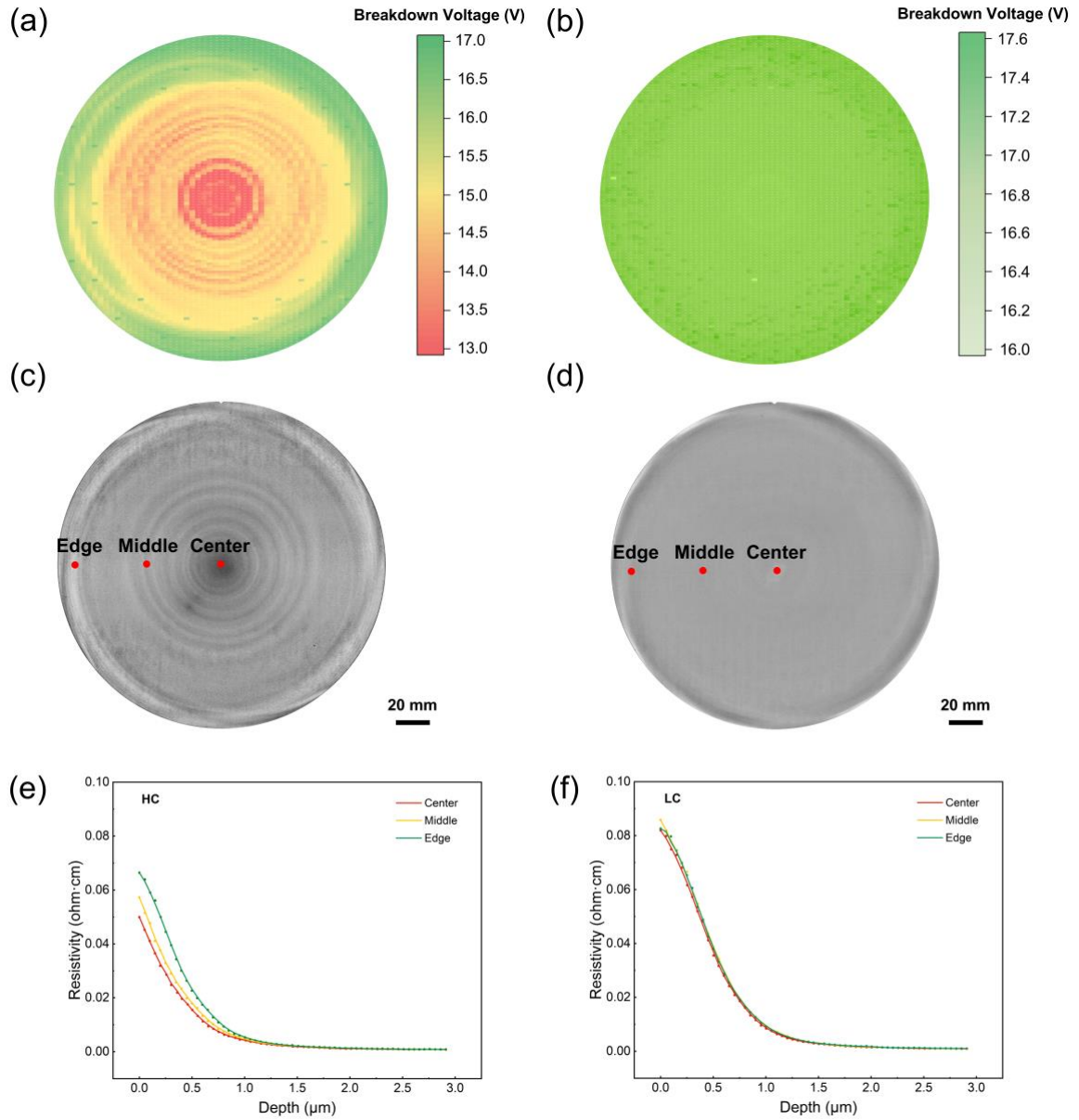


Fig. 1. (a) and (b) Breakdown voltage distribution maps of MOSFETs fabricated on n/n^+ epitaxial wafers using heavily phosphorus-doped substrates with high and low carbon concentrations, respectively. (c) and (d) XRT images of oxygen precipitates in heavily phosphorus-doped substrates with high and low carbon concentrations, respectively, after undergoing the MOSFET fabrication process. (e) and (f) Spreading resistance profiling curves showing the resistivity distribution across different regions of the n/n^+ epitaxial layers on substrates with high and low carbon concentrations, respectively, after undergoing the MOSFET fabrication process.

Infrared properties of a perfectly compensated germanium doped with shallow donors and acceptors below the Mott transition

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Compensation engineering of elemental semiconductors offers a versatile material for specialized, high-performance technological and quantum-level electronic applications, see e.g. [1, 2]. Controlling the compensation in moderately doped germanium (Ge) crystals enables high performance in the ultra-fast detection of infrared free-electron laser pulses [3]. For such applications, materials with low static infrared losses and high dynamic free-charge concentrations are desirable. We investigated the infrared properties of highly compensated (up to 100%) and moderately co-doped (up to the Mott transition [4]) Ge with shallow substitutional centers, gallium (Ga) and antimony (Sb).

The Ge:Sb:Ga crystals (Fig. 1a) were produced using the Czochralski method. The doping material was introduced directly into the crucible. Due to the different depletion of the Ga and Sb during growth because of the different segregation and diffusion coefficients, both the content and ratio of impurities vary along the growth axis of the ingot crystal (Fig. 1b).

Uncompensated, moderately and heavily doped Ge exhibits significant absorption in the far-infrared and also mid-infrared ranges, making the samples far-infrared-opaque as the doping approaches the Mott transition for Ga and/or Sb. The infrared loss is dominated by free carrier absorption at lattice temperatures above thermal ionization of impurities and by photothermal and photoionization processes at low (< 10 K) temperatures (Fig. 1c). With increasing compensation, these losses are gradually decrease to low values in perfectly compensated samples. High compensation prevents the formation of surface and bulk plasmons in the mid-infrared wavelength range up to large doping concentrations, and results the reflection coefficients similar to those of undoped Ge.

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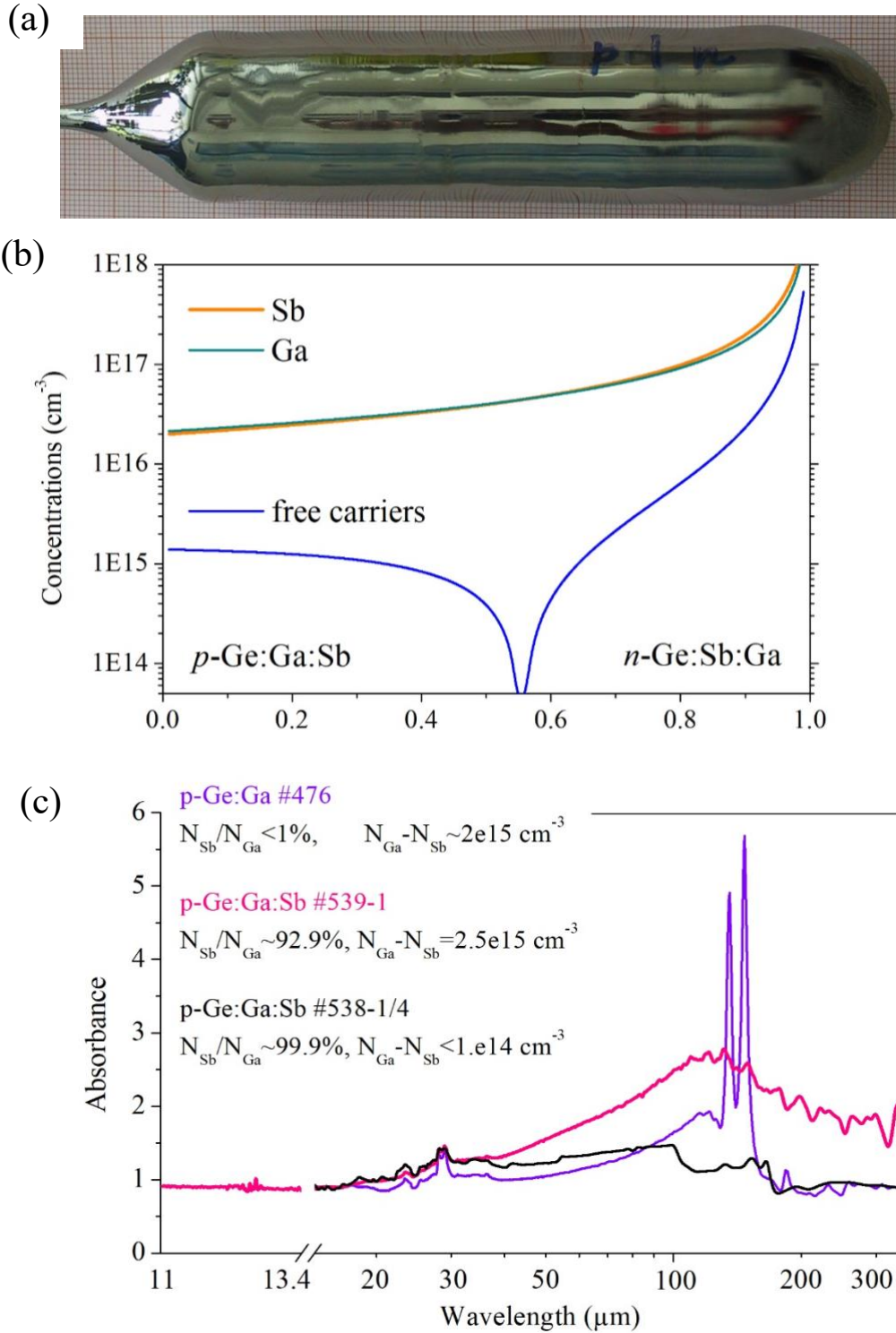


Fig. 1. (a) Image of the grown germanium crystal with the gradient of co-doping with gallium and antimony along the growth axis. (b) Perfect compensation was achieved in the middle of the Ge:Ga:Sb ingot. (c) Low-temperature far- and mid-infrared absorption spectra reveal a clear evolution with increasing compensation: from strong, discrete impurity transitions at low density and compensation to the weak intense, concentration-broadened impurity bands with difference concentration of optically-active charge carriers.

Mechanism of slip line propagation in advanced 300mm silicon substrates

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Abstract

Silicon plastic deformation is known to occur by well-defined glide planes and directions, through the propagation of slip lines defects along (111) planes. We previously reported that such defects originate from dislocations that propagate from silicon edge [1]. They are influenced by several factors such as the annealing temperature and the mechanical support between single wafer tool and substrates. Oxygen concentration in handle silicon is also suspected to play a significant role [2]. This paper dives in the mechanism of slip line formation and propagation on 300mm Cz p- handle Si substrates in batch furnace tools. Temperature and time of anneal process are investigated on Si substrates with different oxygen content. An innovative measurement protocol has been developed on interferometry Pattern Wafer geometry (PWG) tool. The typical defects counted in density and length depending on substrate type are shown fig.1. Slip line formation is activated by both temperature and time, and strongly favored during usual Front-End temperatures higher than 1050°C. Whereas their origin are scratches deepening with time on high-Oi content Si substrates ($> 5.10^{17}$ at.cm⁻³), their thermally-activated propagation is mainly driven by multiplication of single dislocations on substrates with low Oi concentrations ($< 4.5. 10^{17}$ at.cm⁻³) (fig.2). We illustrate the pinning effect played by oxygen by determining a threshold in the Oi concentration (fig. 3) [3]. The mechanism of slip-line propagation is confirmed to increase with time in a exponential mode. An activation energy close to the one reported for Oi migration is finally determined. These result additionally point out the impact of mechanical support in 300mm industrial equipments which influence the nature of stress (thermal-gradient vs gravitational type) depending on the type of substrates.

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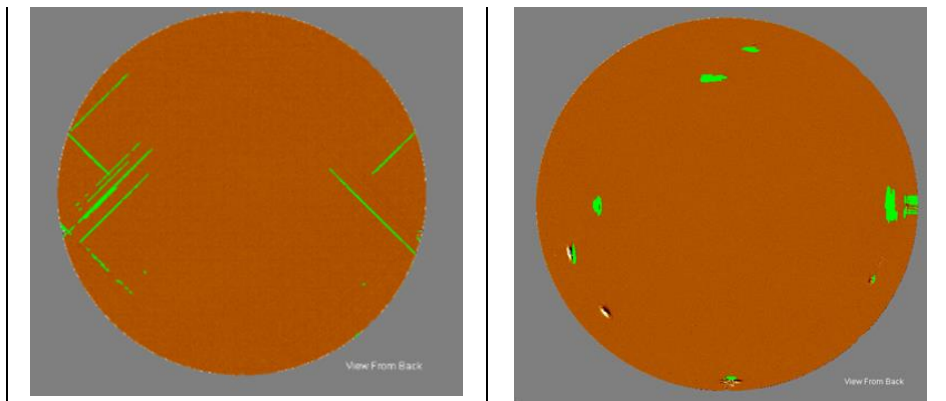


Fig. 1. PWG images of defects formed on a 300mm p- Cz Si wafer after 4 hours at 1100°C; left: low-Oi Si substrate ($O_i < 2.5 \cdot 10^{17} \text{cm}^{-3}$) right: high-Oi Si substrate ($O_i > 5 \cdot 10^{17} \text{cm}^{-3}$)

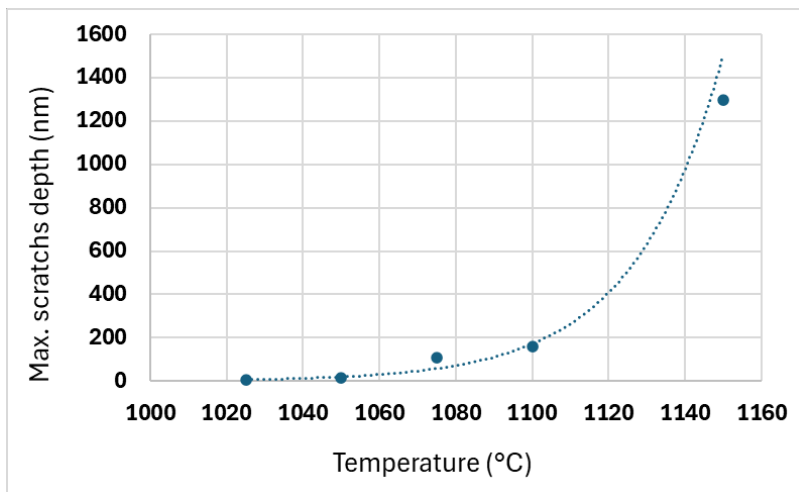


Fig. 2. Scratch depth (nm) evolution with temperature (°C)

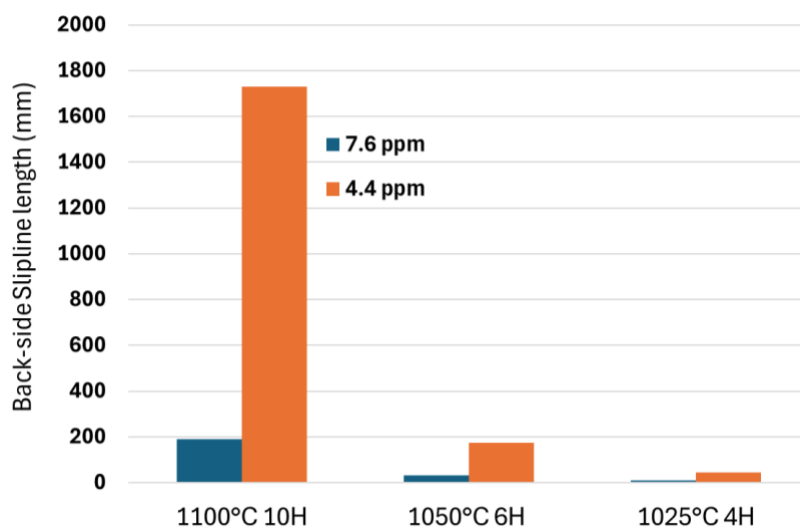


Fig. 3. Back-side slipline length (mm) after different temperature and time in batch furnace tool.

On the formation of local molten regions on Si surfaces by pulsed laser annealing at the melting threshold

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Microsecond (μ s) or nanosecond (ns) laser annealing are attractive techniques for advanced devices requiring high active dopant concentrations, or 3D sequential integrations in which the top layers need to be annealed while the underlying structures have to be kept at low temperature. Annealing in the liquid phase regime gives access to the highest active dopant concentrations in silicon and germanium. Nevertheless, in this case, the edge of the laser beam can leave some undesired defective and rough regions where the laser energy density intercepts the melting threshold as it decreases from its maximum value to zero. The generated topography being detrimental to the future devices, it is of prime importance to understand the involved mechanisms and tentatively identify ways to avoid the formation of the defective regions. The present work provides an in-depth description of the nanostructures formed at the surface of silicon when exposed to a pulsed laser beam with an energy density close to the melting threshold [1].

(100) and (111)-oriented silicon surfaces submitted to various surface preparations were exposed to μ s and ns laser beams using energy densities ranging from conditions leaving Si in the solid-phase up to conditions leading to the formation of a continuous liquid Si film (Fig. 1a). For intermediate values close to the melting threshold, local molten regions (LMRs) could be generated, *i.e.* islands of molten Si surrounded by still solid Si, resulting in surface roughening upon solidification. The obtained LMRs were carefully characterized by scanning electron microscopy (SEM) top-view observations, atomic force microscopy (AFM) and transmission electron microscopy (TEM) in cross-section mode.

On (100) surfaces with a 1 nm thin oxide, the shape of the LMRs formed by ns-laser evolves from a square-based pyramid for the smallest ones (Fig. 1b) to a pseudo-square castle-like nanostructure with one peak located in each corner for the largest ones (Fig. 1c). The average LMR size is about 464 nm for a 160 ns pulse duration. The edges of these square LMRs are aligned along $\langle 110 \rangle$ crystalline directions. On (111) surfaces, LMRs are pyramids with a triangular basal shape (Fig. 1d). The size of the LMR increases with the laser pulse duration with a dependence close to the square root of the annealing duration. This suggests that the size of the LMRs is limited by heat diffusion. No geometrical LMR is found after HF-last surface preparation indicating that the presence of a thin oxide is critical. Multi-pulse experiments show that each corner of the nanostructures acts as a preferential melting point for the subsequent pulse (Fig. 1e). Finally, the top oxide layer thickness has an impact on the nanostructure shape, stretching their corners along $\langle 100 \rangle$ directions when the oxide becomes thicker. In summary, this work provides a set of original data accurately describing the LMRs obtained at the melting threshold during laser annealing of Si surfaces. Their formation would start with the nucleation of a semi-spherical droplet of liquid silicon at the Si/surface oxide interface. Such molten nuclei would grow in-depth and laterally, their contour being governed by the temperature gradient and the anisotropy of silicon melting rate.

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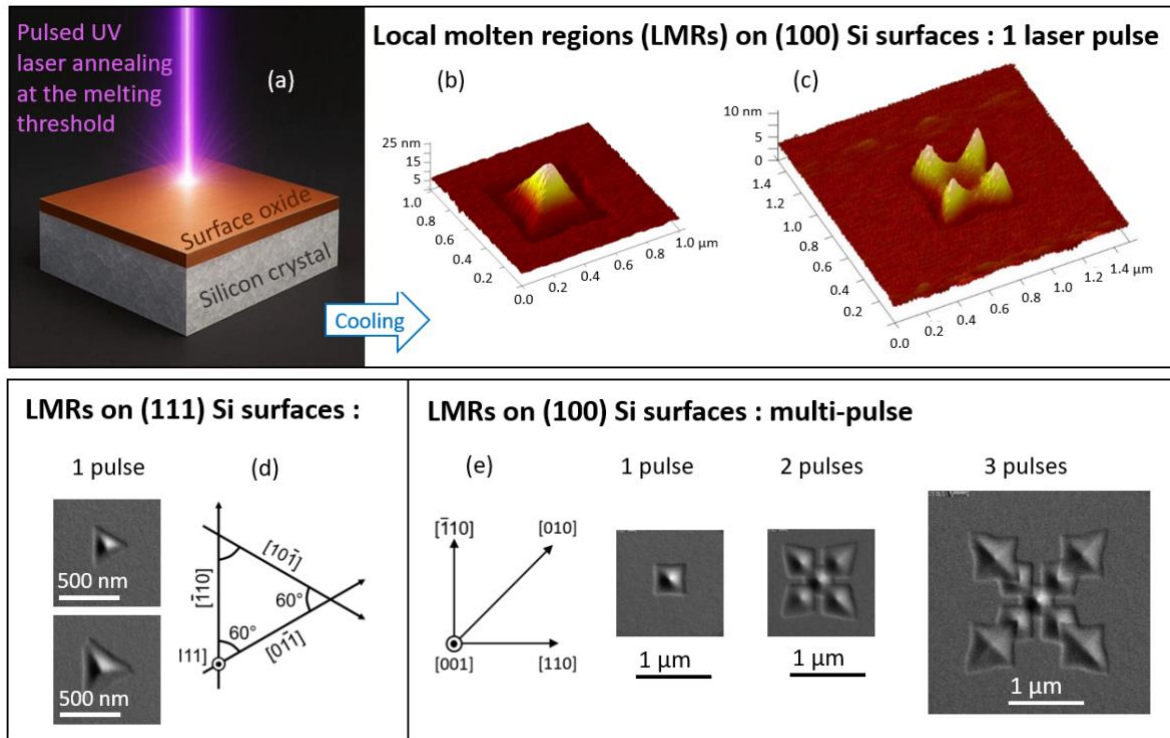


Fig. 1. (a) Experimental protocol. AFM pictures illustrating small (a) and (b) larger local molten regions (LMRs) formed on (100) Si surfaces. SEM observations of LMRs obtained on (111) Si surfaces (d), and on (100) Si surfaces (e) upon laser irradiation with 1, 2 and 3 pulses.

On the gettering properties of isovalent tin and lead impurities in n-type Czochralski silicon

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Doping silicon (Si) with group IV isovalent impurities is an effective technique for controlling oxygen precipitation and radiation hardness (see, e.g., [1–3]). Recently [4], we found that minority-carrier lifetime (τ) in tin (Sn) doped n-type Czochralski (Cz) silicon increases significantly after annealing at temperatures above 300 °C ($\tau_{\text{ann}} \gg \tau_0$, see Fig. 1). This may indicate the gettering properties of tin.

In this paper, we study the influence of Sn, lead (Pb), and Sn–Pb co-doping on the change of τ in as-grown Cz n-Si and after subsequent isochronal (20 min) annealing at temperatures between 300 and 440 °C. Doped and undoped Si were grown from the same starting material under similar conditions. Cz n-Si was doped in the melt with Sn and/or Pb impurities. The concentrations of Sn and Pb in the samples were $\approx 3 \times 10^{17} \text{ cm}^{-3}$ and $\approx 1 \times 10^{18} \text{ cm}^{-3}$, respectively.

It is found (see Fig. 2) that: 1) In as-grown Cz n-Si, Sn and Pb impurities have different effects on τ . The carrier lifetime in n-Si:Pb is higher compared to undoped n-Si (by approximately twice) and conversely in n-Si:Sn; 2) Annealing in the range of 300–440 °C leads to an increase in τ in all samples. Maximum τ changes are observed around 400 °C. At the same time, the relative changes are the same in n-Si:Pb and undoped n-Si but significantly larger in n-Si:Sn (τ becomes comparable to that of the control sample); 3) The τ behavior in n-Si:Sn+Pb samples is the same as in n-Si:Pb.

These results suggest that Pb acts as an effective internal getter for impurities and defects that determine the carrier lifetime in Cz n-Si. The role of Sn is discussed.

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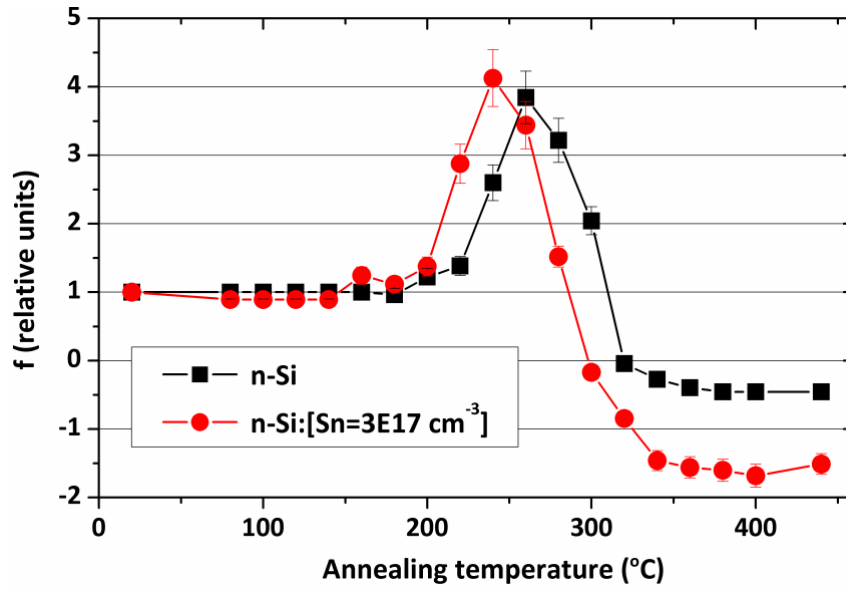


Fig. 1. Isochronal (20 min) annealing of the carrier lifetime in Cz n-Si:Sn and control n-Si after ^{60}Co γ -irradiation with a dose of $\Phi = 5.9 \times 10^{14} \text{ cm}^{-2}$. $f = (1/\tau_{\text{ann}} - 1/\tau_0)/(1/\tau - 1/\tau_0)$, where τ_0 – the initial carrier lifetime (as-grown Si), τ – the carrier lifetime after irradiation, and τ_{ann} – the carrier lifetime after each annealing step.

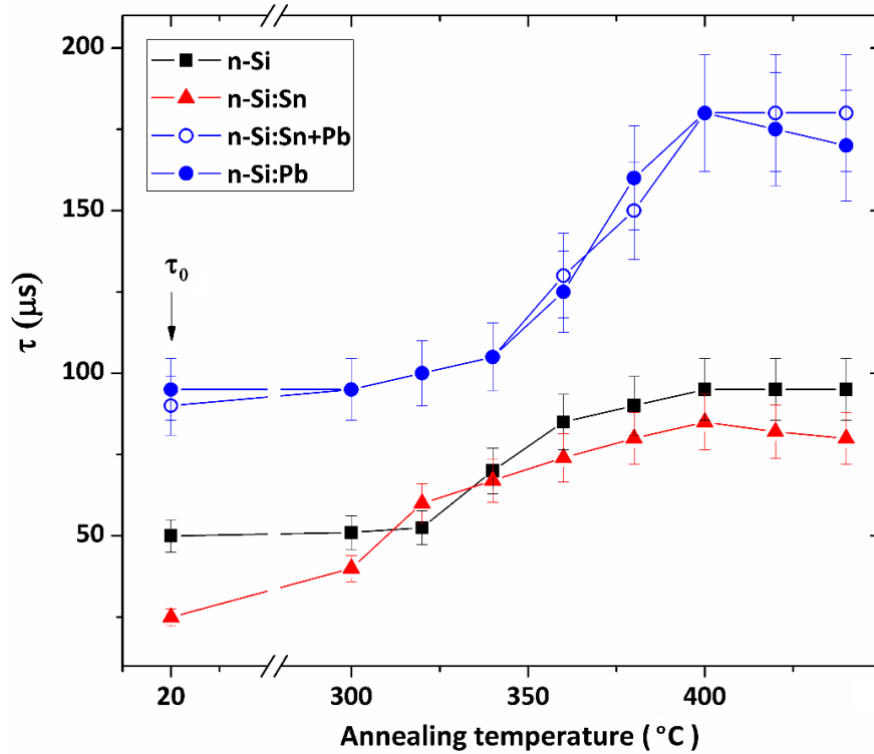


Fig. 2. Isochronous (20 min) annealing of the charge carrier lifetime in Cz n-Si doped with isovalent Sn and Pb impurities. All samples are n-type phosphorous doped with resistivity $\approx 2 \Omega \cdot \text{cm}$. The excitation level used was typically $\Delta n/n_0 \approx 5 \%$.

Optically detected spin properties of the telecom L-band C center in silicon

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Color centers in silicon are emerging as optically addressable defects with potential relevance for silicon-based photonic and quantum devices [1]. In particular, defects combining telecom-wavelength emission with accessible spin states are of considerable interest. However, experimental evidence of spin-active centers operating in the telecom L-band (1565–1625 nm) has remained limited.

Here, we report on the optically detected spin properties of the C center in silicon emitting at 1570 nm. Under optical excitation, the defect exhibits stable photoluminescence in the telecom L-band. Using optically detected magnetic resonance, we resolve its spin transitions and investigate their magnetic-field dependence [2]. The observed resonance features confirm the spin-active nature of the defect and provide direct experimental validation of the theoretically predicted electronic structure and spin configuration [3].

Our results establish the C center as a telecom-emitting, spin-active defect in silicon and contribute to the microscopic understanding of this complex. These findings are relevant for defect engineering in silicon and highlight the potential of tailored color centers for advanced silicon-based quantum photonic device platforms.

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Origin of optically active Er^{3+} sites in Silicon on Insulator-based photonic waveguides

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Quantum emitters with spin degree of freedom in solid-state hosts emerge as promising candidates for quantum communication and computing applications. Erbium (Er) trivalent ions in Si demonstrate excellent optical and spin properties including optical transitions within the telecommunication C-band, low inhomogeneous broadening, long optical and spin coherence times at cryogenic temperatures [1, 2, 3, 4]. Although the successful generation of Er^{3+} sites in Silicon on Insulator (SOI), a complementary-metal-oxide-semiconductor platform, was previously reported [1], little is known about their origin and formation conditions. Here, we report the comprehensive study of the optically active Er^{3+} sites observed in fiber-packaged photonic waveguide using photoluminescence (excitation) spectroscopy. These waveguides were fabricated in the 10^{16} Er/cm^3 implanted commercial Silicon on Insulator (SOI) with Czochralski (CZ, 8–15 $\Omega\cdot\text{cm}$, Boron(B)-doped) and Float Zone (FZ, > 3000 $\Omega\cdot\text{cm}$, B-doped) device layers annealed at 500 and 700 °C. The comparison with Er^{3+} sites generated in FZ bulk Si with different Oxygen (O) levels points towards the O role in the formation of observed Er^{3+} sites. While no optically active Er^{3+} sites were found in bulk FZ Si wafers (> 3000 $\Omega\cdot\text{cm}$, B-doped) implanted at 10^{16} Er/cm^3 level, Er^{3+} sites in the FZ SOI-based waveguides matched Er^{3+} sites in FZ bulk Si with O and Er co-implantation (10^{16} Er/cm^3 and 10^{17} O/cm^3). Similar sites were found in micropillar arrays fabricated in FZ bulk Si (10^{17} Er/cm^3 and 10^{17} O/cm^3 implantation). This similarity between sites observed in the commercial Er-implanted FZ SOI and FZ Si implanted with both Er and O suggests that the background O level in FZ SOI is significantly higher than the expected value of $<10^{14} \text{ O/cm}^3$. The observed Er^{3+} transitions possess long spin lifetimes (>1 s at moderate magnetic fields of ~100 mT), and low inhomogeneous broadening (<1 GHz). Annealing at 700 °C was essential to obtain the single exponential optical decay (>1 ms) of Er^{3+} sites indicating the reduced density of implantation-induced defects. The reliable generation of Er^{3+} sites in SOI-based photonic waveguides is a promising step towards scalable and fully integrated on-chip quantum photonic systems.

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Progress in understanding optically detected magnetic resonance (ODMR) spectra of $A_{Si}-Si_i$ -defects

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Defects from the acceptor-interstitial silicon ($A_{Si}-Si_i$)-defect species were found to be promising candidates for qubits in silicon-based quantum technology [1]. To further explore their qubit properties optically detected magnetic resonance (ODMR) measurements were carried out on quenched indium-doped silicon samples featuring $In_{Si}-Si_i$ -defects. Several different ODMR signals were found in the spectra. An approach to understand these spectra in frame of a ground and excited state triplet system in similarity to the NV-defects in diamond is investigated. Additionally, ideas for a quantum computing system architecture in silicon based on $A_{Si}-Si_i$ -effects are put into the discussion. Some possible switching mechanism for the qubit interaction as well as readout mechanism based on photoluminescence excited by a moving laser are proposed. The latter works like a train driving by and taking the information to the core.

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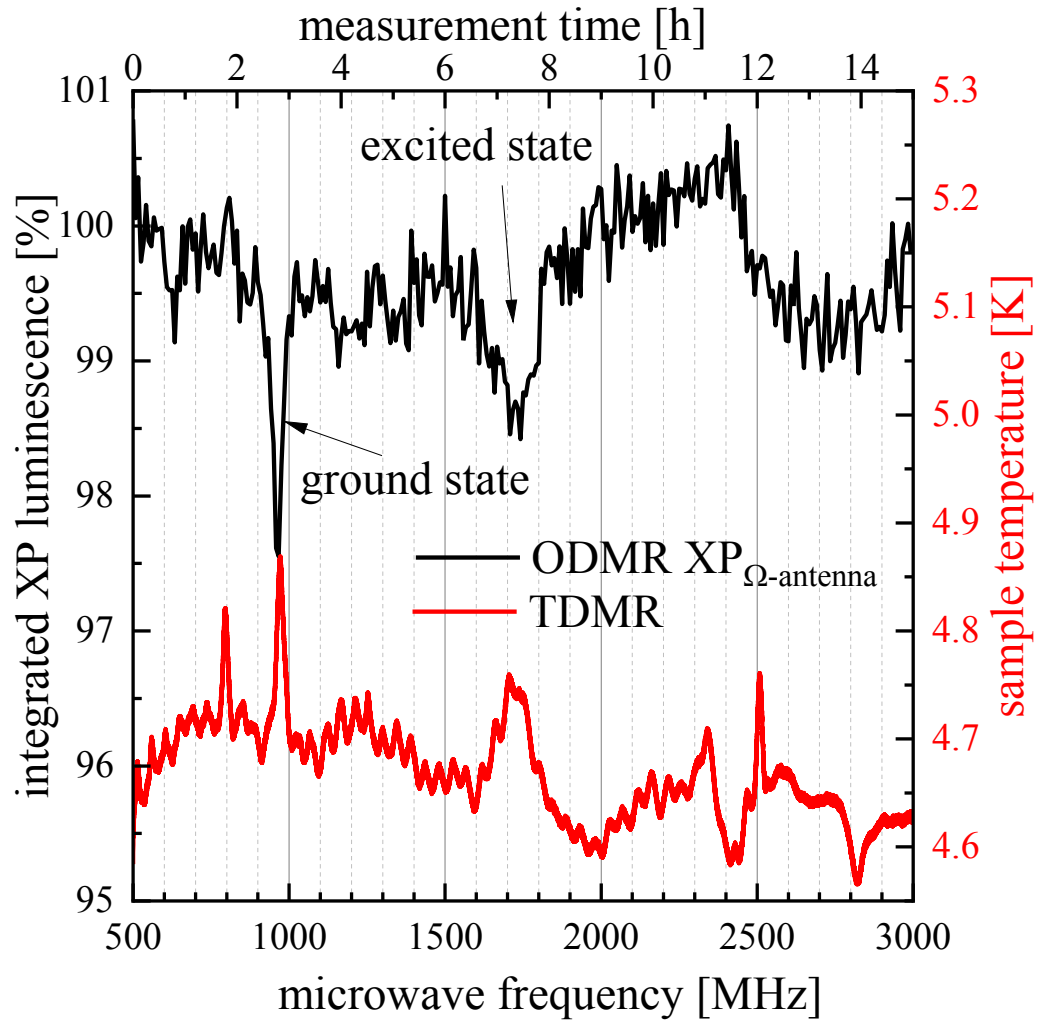


Fig. 1. Optically detected magnetic resonance (ODMR) and temperature detected magnetic resonance (TDMR) spectra measured on quenched indium-doped silicon samples featuring $\text{In}_{\text{Si}}\text{-Si}_i$ -defects. Two ODMR signals are visible which can be attributed to a ground and excited state.

Pulsed Laser Melting for TOPCon technology: new routes to higher efficiency

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Tunnel oxide passivating contacts (TOPCon) are a leading route to high-efficiency crystalline-silicon (c-Si) solar cells. The core structure poly-Si/SiO_x/c-Si uses an ultrathin (<2 nm) tunnel oxide to passivate the c-Si surface while a heavily doped poly-Si layer provides carrier selectivity. Carrier transport is dominated by tunneling through the SiO_x layer, although direct conduction through local oxide openings (“pinholes”) in textured contacts can also contribute. In this work we investigate both pathways and show how pulsed laser melting (PLM) can be used to enhance performance without sacrificing passivation.

Using nanosecond-PLM, we achieve hyperdoping of poly-Si with boron and gallium beyond their equilibrium solid-solubility limits, yielding low-resistivity contacts while preserving the SiO_x/c-Si interface. The surface-localized heating inherent to PLM suppresses boron diffusion through SiO_x that typically degrades passivation in conventional processes [1,2]. Thermal-stability assessments further support the robustness of the laser-treated stacks and their suitability for industrial integration.

For the pinhole-mediated pathway, we explore PLM as a method to create nanoscale openings at the tips of pyramidal-textured cells while maintaining passivated contacts on the pyramid facets [3]. Atomic force microscopy (AFM) tracks morphology as a function of laser parameters, and conductive AFM (c-AFM) provides spatially resolved current maps that clarify carrier transport through individual pinholes [3,4].

Overall, PLM enables hyperdoped, low-resistance poly-Si contacts with preserved passivation and controlled pinhole formation compatible with textured surfaces, together outlining a viable route to TOPCon performance gains with manufacturable process windows.

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Radiation-induced defect reactions in Silicon Junction Barrier Schottky Diodes upon irradiation with alpha particles in different regimes

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Junction barrier Schottky (JBS) diodes have significant advantages in comparison with conventional Schottky diodes and p-n junctions and are widely used nowadays in high-temperature and high-power electronics [1,2]. The JBS diodes combine the low voltage drop of a Schottky diode with the low leakage current of a p-i-n diode. The processes of radiation-induced defects (RIDs) formation in semiconductor devices are more complicated compared to those in bulk crystals and in many cases depend on architecture and working regimes of devices [2,3]. In spite of many studies there are still some experimental observations that have not been understood properly and even for simple silicon-based devices there is no consensus on the interpretation of some aspects of the radiation damage processes [3,4].

In this work we present results of a study of the radiation-induced defect reactions in JBS silicon diodes produced on boron-doped epi-Si ($\rho \approx 20 \Omega \text{ cm}$) with a mesh of about $5 \mu\text{m}$ deep n^+ regions in the drift layer which screen the Schottky contact from high fields upon reverse bias. The diodes were irradiated with alpha-particles with energies of about 5 MeV at about 290 K in passive (no bias) and active (different values of bias applied in forward and reverse directions) regimes. The penetration depth of the particles is $\sim 25 \mu\text{m}$, i.e. the radiation-induced damage layer is beyond the mesh of n^+ regions. Current-voltage (I - V) and capacitance-voltage measurements were carried out in order to evaluate the quality of the diodes and to determine the uncompensated shallow acceptor concentration (p) and the width of the probed depletion regions. Deep-level-transient spectroscopy (DLTS) has been used for the detection of hole and electron emission from deep level defect states. It has been found that irradiation results in a significantly lower formation rates of the RIDs with deep levels in the depleted region of the reverse biased structures and in the forward-biased diodes with forward current of $I_f \geq 0.05 \text{ A}$ as compared with those in similar diodes irradiated without applied bias or with small values of bias in the forward direction ($I_f \leq 0.03 \text{ A}$). Further, post-irradiation minority-carrier-injection treatments at 80 K have resulted in significant changes in p values and in the DLTS spectra. It is argued that the observed phenomena are related mainly to some specific features of the silicon self-interstitial atoms produced by the irradiation: a very strong dependence of their thermal stability on charge state and a highly enhanced mobility under minority carrier injection conditions.

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Search for stable atomic configurations in SiGe, SiSn, and GeSn alloys using DFT and optimization algorithms

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SiGe, SiSn, and GeSn are group-IV binary alloys based on the diamond crystal structure, whose optical and mechanical properties can be engineered through composition control. SiGe is a particularly important material with a wide range of applications, including thermoelectric devices, substrates for strained-Si technology, solar-cell substrates, and fabrication processes for gate-all-around (GAA) transistors. In addition, SiSn and GeSn are attractive for near- and mid-infrared optoelectronic devices because they undergo an indirect-to-direct bandgap transition at high Sn concentrations[1,2]. These alloy systems have conventionally been assumed to exhibit random atomic distributions, and especially at the 1:1 composition, a zincblende-type atomic configuration has often been presumed. However, recent experimental and theoretical studies have suggested the presence of short-range order in these alloys, indicating that such assumptions are not necessarily valid[3]. Furthermore, in the SiSn and GeSn systems, the solid solubility of Sn is low, making crystal growth difficult; as a result, many aspects of their atomic configurations and physical properties remain unclear. Since many semiconductor properties strongly depend on atomic configurations, clarifying specific atomic configurations is important not only for deepening the understanding of material properties but also for improving the accuracy of physical property predictions based on theoretical calculations.

In this study, we explored stable atomic configurations of SiGe, SiSn, and GeSn alloys by combining a combinatorial optimization algorithm with first-principles calculations. We used a 64-atom supercell constructed by expanding the conventional unit cell of the diamond structure to $2 \times 2 \times 2$. Starting from 64-atom models of pure Si or Ge, eight Ge or Sn atoms were substituted to construct seven compositions ($x = 0.125, 0.250, 0.375, 0.500, 0.625, 0.750$ and 0.875) for $\text{Si}_x\text{Ge}_{1-x}$, $\text{Si}_x\text{Sn}_{1-x}$, and $\text{Ge}_x\text{Sn}_{1-x}$. Multiple independent searches were performed for each composition. For all explored structures, statistical trends in atomic configurations were analyzed by counting the number of nearest-neighbor Y atoms ($Y = \text{Si}, \text{Ge}, \text{Sn}$) coordinated to an Y atom. In addition, the formation energies of each alloy were calculated to compare the energetic stability of various crystal structure models.

The analysis revealed that in SiGe alloys, Si (Ge) atoms preferentially have same-species atoms as their nearest neighbors. In contrast, GeSn alloys exhibit a tendency for Ge (Sn) atoms to be preferentially coordinated with different species. SiSn alloys were found to show intermediate atomic-ordering behavior between those of SiGe and GeSn. Notably, these characteristic tendencies in atomic configurations were found to be independent of composition.

Focusing on the 1:1 composition ($x = 0.500$), we discovered stable structures exhibiting ordering patterns that differ from the conventionally assumed zincblende-type atomic configurations. In the identified $\text{Si}_{0.5}\text{Ge}_{0.5}$ structure, each Si (Ge) atom is coordinated by three Si (Ge) atoms and one Ge (Si) atom at nearest-neighbor sites. In $\text{Ge}_{0.5}\text{Sn}_{0.5}$, each Ge (Sn)

atom is coordinated by three Sn (Ge) atoms and one Ge (Sn) atom. In $\text{Si}_{0.5}\text{Sn}_{0.5}$, each Si (Sn) atom is consistently coordinated by two Si (Sn) atoms and two Sn (Si) atoms.

Furthermore, in SiGe, the conventionally assumed zincblende-type atomic configuration was found to be the most unstable among the considered structures, whereas in GeSn it is the second most stable. In SiSn, similar to SiGe, the zincblende-type atomic configuration was found to be relatively unstable; however, it was also revealed that many configurations exist that are even less stable than the zincblende-type atomic configuration.

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Structure loss during the Czochralski silicon process: causes, remedies and ML aid

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The Czochralski (Cz) silicon method is the most used process to grow monocrystalline silicon ingots both for the photovoltaic industry and microelectronics. During this process, the silicon ingot can experience the loss of the monocrystalline structure and become multicrystalline. This is one of the major challenges for the industry as structure loss significantly reduces the production yield and increases the cost of the final monocrystalline silicon wafers.

In this work, we present the different types of structure loss. We also discuss their causes and mechanisms as well as how machine learning can help reduce their occurrence.

We combine non-destructive surface examination and production data analysis to characterize structure loss types and root causes. Surface examination enable categorizing of failed ingots; for example the width of growth ridges provides a practical representation for the thermal gradient, with most failures preceded by reduced gradients, and some showing clear particle-hit causing immediate transition to multicrystalline structure [1]. Root-cause analysis reveals four dominant categories: melt contamination/particles, thermal fluctuations, melt vibration, and growth-rate variations. All of them can be affected by process control [2]. For automated monitoring, CNN-based vision models classify SL from ingot surface/process images; transfer learning with incremental training gives the most stable high-accuracy pipeline among tested architectures [3]. The model was trained on more than 14,000 ingots and shows high detection accuracy but also indicate that many predictive variables develop later [3, 4].

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Superacid-based diagnosis of damage in high-carrier-lifetime crystalline silicon

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As silicon passivation and processing improves, small changes in surface recombination or bulk lifetime can have considerable impacts on the overall device performance. There have been significant improvements in efficiency of both industrial and research scale solar cells [1]. This improvement is, in part, due to continual developments in passivation approaches and processing steps. As both surface and bulk processing improve, and we approach silicon's intrinsic lifetime limit [2], previously minor sources of degradation can have significant impacts on overall effective lifetimes, with even dilute levels of defects (concentrations $\sim 10^{10} \text{ cm}^{-3}$) detectable with lifetime-based (i.e., photoconductance decay, photoluminescence imaging) techniques.

Diagnosing any degradation sources is of utmost importance, and accurate separation of surface and bulk effects is vital. Conventional silicon passivation techniques, such as thermal oxidation or dielectric deposition, involve high ($\gg 200^\circ\text{C}$) temperature processing, which can modify the bulk properties of the silicon, and change the sample under investigation. Instead, superacid-based passivation is a rapid, room temperature approach, employing the superacid bis(trifluoromethanesulfonyl)amide [3]. Using superacid passivation alongside lifetime techniques allows the presence of induced defects to be inferred, and enables development of processes (e.g., thermal annealing) to mitigate the effects of defects created [4]. Superacid passivation can be combined with chemical etching to sequentially remove material from the substrate surface, identifying the depth within the substrate that such defects are formed.

This presentation will discuss key examples of superacid-based diagnosis of silicon defects, with particular reference to those induced by ion exposure. Ion beam techniques are employed to enable advanced characterisation of the properties of semiconductors – e.g., time-of-flight elastic recoil detection (ToF-ERDA), which provides depth-resolved compositional analysis, and photoexcited muon-spin spectroscopy (photo- μSR), which provides information on charge carrier dynamics within semiconductors. Both techniques involve implantation of high energy species (14 MeV $^{127}\text{I}^{8+}$ and 4 MeV μ^+ , respectively), and each have been described as non-destructive or “inert” probes [5, 6]. However, superacid-based studies have recently revealed that these “inert” techniques do indeed damage samples under investigation [4, 7], as summarized in Figure 1.

Superacid passivation enables straightforward identification of surface- and bulk-degradation of silicon, which can be exploited to glean information on impacts of process steps or underlying material quality.

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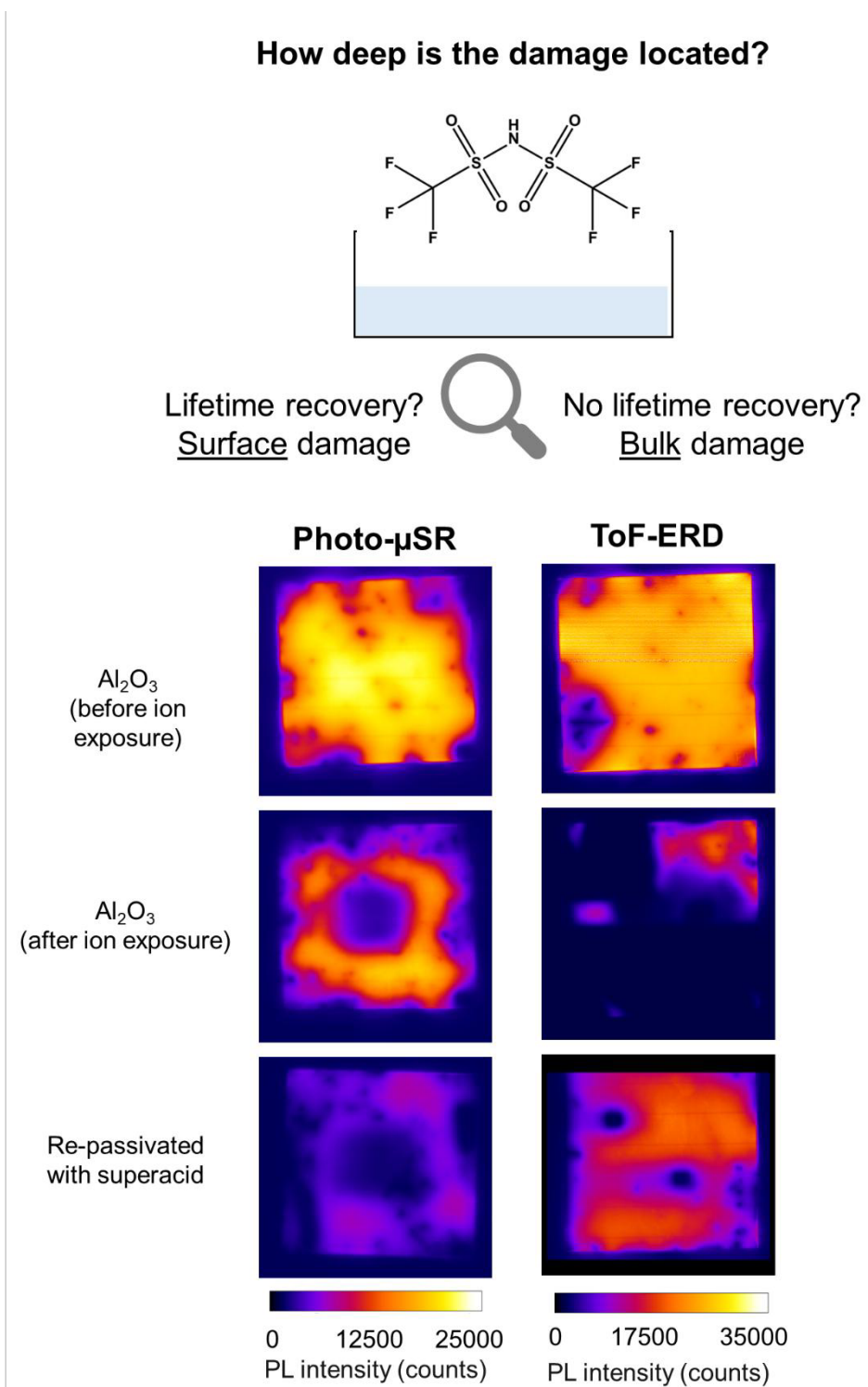


Figure 1. Examples of beam damage in high-lifetime crystalline silicon following muon exposure [4] and implantation of 14 MeV $^{127}\text{I}^{8+}$ ions. The photoluminescence (PL) image shows a high-lifetime silicon wafer measuring 5 cm by 5 cm.

Surface passivation of silicon by ZnO/Al₂O₃ stacks with controlled SiO_x interlayers

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High efficiencies in solar cells with architectures including silicon heterojunction (SHJ) or tunnel oxide passivated contact (TOPCon) cells are typically achieved by using passivating contacts to reduce recombination at the interfaces. However, these cell architectures suffer from parasitic absorption and relatively high manufacturing costs. Transparent conductive oxides (TCOs), such as ZnO, have been explored as a promising candidate to reduce parasitic absorption due to good optical transparency, while offering electron selectivity. Recently, it has been demonstrated that ZnO grown by atomic layer deposition (ALD) can also provide effective silicon surface passivation, which can be augmented by Al-doping of the ZnO film [1,2]. Adding further to the advantages, ZnO also offers low sheet and contact resistivity [2], making it a compelling candidate for passivating contacts.

In our work, we have examined silicon surface passivation using ZnO/Al₂O₃ stacks deposited by atomic layer deposition (ALD), with a particular focus on the role of the interlayer formed between the ZnO and the silicon substrate. Controlled interlayers were formed by carefully applying different surface treatments prior to ALD. These treatments included an HF dip (to remove any native oxide) and oxides grown by treatments including RCA1, RCA2, nitric acid oxidation (NAOS) and UV-ozone exposure. Prior to ALD, the treated silicon surfaces were characterised by X-ray photoelectron spectroscopy (XPS) and the SiO_x thickness was determined via the thickogram method [3]. Selected XPS results are shown in Fig. 1. SiO_x layers in the ~0.2-0.5 nm range were formed by chemical treatments other than HF, with HF treated samples having almost no detectable SiO_x.

ZnO (20 nm)/Al₂O₃ (25 nm) stacks were grown by ALD on both sides of pre-treated silicon samples at 200 °C. Post-deposition annealing was required to activate the surface passivation. Effective lifetime data in Fig. 2 show that good passivation levels were achieved in samples for which XPS showed there was a pre-existing SiO_x layer at the surface. Annealing at 500 °C was found to give optimal passivation, with NAOS-treated samples giving marginally higher lifetimes than with the other pre-treatments. High-resolution transmission electron microscopy (TEM) was then used to characterise the interface between the Si substrate and the ZnO layer. Results in Fig. 3 show the presence of a SiO_x layer in both poorly passivated samples which had been HF-dipped and in well-passivated samples with a NAOS pre-treatment. Thus, although there is a SiO_x interlayer at the end of both processing sequences, high-quality passivation seems to require the presence of a certain type of SiO_x layer prior to ALD. Further work will aim to identify the differences between the SiO_x layers and their role in the surface passivation mechanism.

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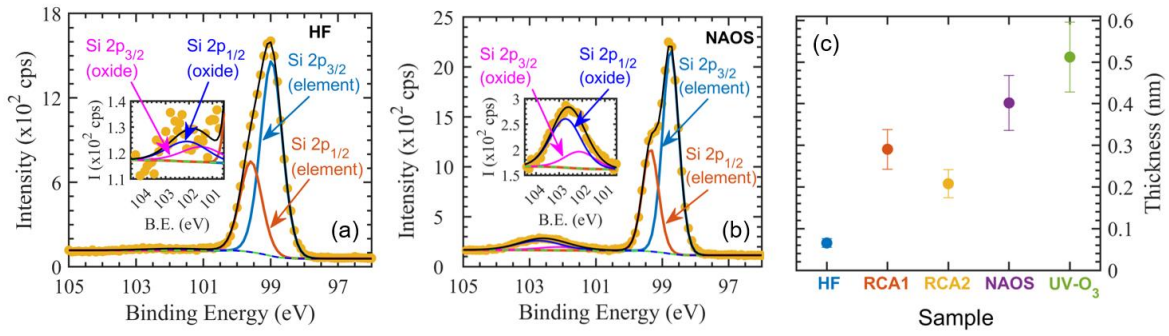


Fig. 1. Selected results from X-ray photoelectron spectroscopy (XPS) of silicon surfaces to which different chemical pre-treatments has been applied. Si 2p core level spectra for silicon and SiO_x prepared via treatments of (a) an HF-dip; and (b) NAOS. (c) Thicknesses of the SiO_x layers calculated from the Si 2p core levels using the thickogram method for five different surface pre-treatments.

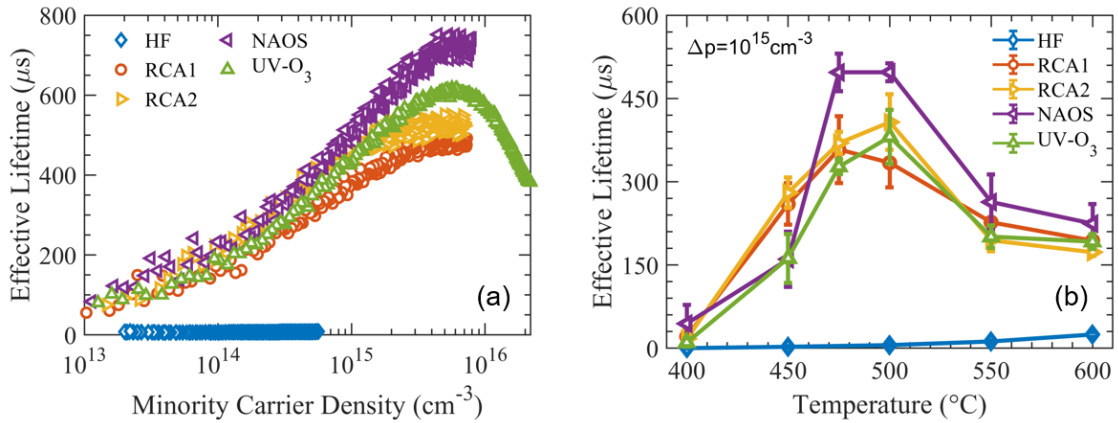


Fig. 2. Effective charge carrier lifetime data for 5 Ω -cm, *n*-type, 150 μm thick silicon wafers passivated with ZnO(20 nm)/Al₂O₃(25 nm) stacks after different pre-treatments (HF-dip, chemical (RCA1, RCA2, NAOS), and UV-O₃ exposure) followed by a passivation activation anneal. The effective lifetime is plotted versus minority carrier density for samples annealed at 500 $^{\circ}\text{C}$ in (a). The graph in (b) shows the effective lifetime at a minority carrier density of 10^{15} cm^{-3} versus activation annealing temperature.

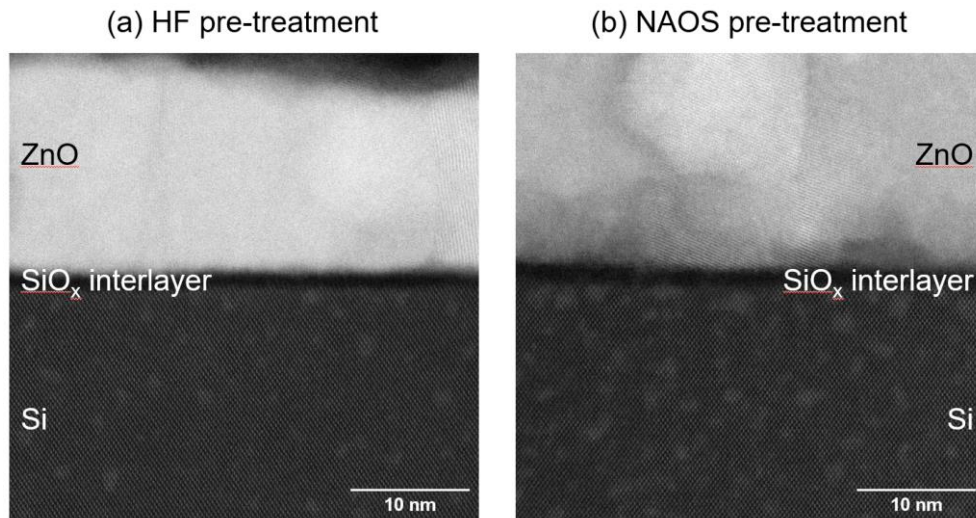


Fig. 3. Cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images of the interfacial region between silicon and ZnO in polished silicon samples coated with ZnO/Al₂O₃ stacks. Image (a) is from a sample which was HF-dipped prior to ALD. Image (b) is from a sample on which a SiO_x layer was grown by NAOS treatment prior to ALD. Both samples have been annealed at 500 $^{\circ}\text{C}$.

Theoretical study on the stability of Sn atom in Ge thin film grown on GaSb substrates

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GeSn semiconductors are attracting attention as a material for electronic and optoelectronic devices [1]. To increase the Sn concentration, GeSn thin films are grown on substrates (GaSb, InP, etc.) with a larger lattice constant than Ge [2][3]. However, the growth of GeSn thin films poses various issues, such as optimization of the substrate surface, electrical interaction between the GeSn thin film and the substrate, and understanding the physical properties near the interface.

To address the above problems, we used density functional theory calculations to clarify the influence of a GaSb(001) substrate on the stability of a Sn atom in Ge thin films. A 24-layer (48-atom) Ga₂₄Sb₂₄ model was first optimized, and its cell lengths were determined. After that, the top 15 layers of the model were replaced with Ge layers, and the atomic coordinates of the middle 3 of the lower 9 layers of GaSb (Ga-surface or Sb-surface) were fixed (Fig. 1). Finally, the model was optimized again. Note that a Ge layer was subjected to a planar tensile stress of about 2 GPa. One of the atoms in the Ge layer was replaced with a Sn atom while changing the distance from the interface with the GaSb substrate. The distance dependence of the Sn substitutional formation energy (E_f) was intensively investigated.

The most important result is that the E_f of a Sn atom in the Ge layers increased monotonically up to the 3rd layer from the interface with the GaSb substrate and almost saturated at 0.10-0.11 eV above the 4th layer (Fig. 2). Analyses on the density of states revealed that the electron transfer from the Ge layers to the GaSb substrate increased the stability of the Sn atom near the interface. The saturated value away from the interface was smaller than the Sn substitutional formation energy of 0.28 eV in bulk Ge, which can be attributed to the planar tensile stress applied to the Ge thin film on the GaSb substrate. More detailed results will be presented at the conference.

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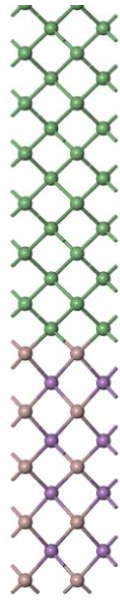


Fig. 1. $\text{Ge}_{30}/\text{Ga}_{10}\text{Sb}_8$ model.

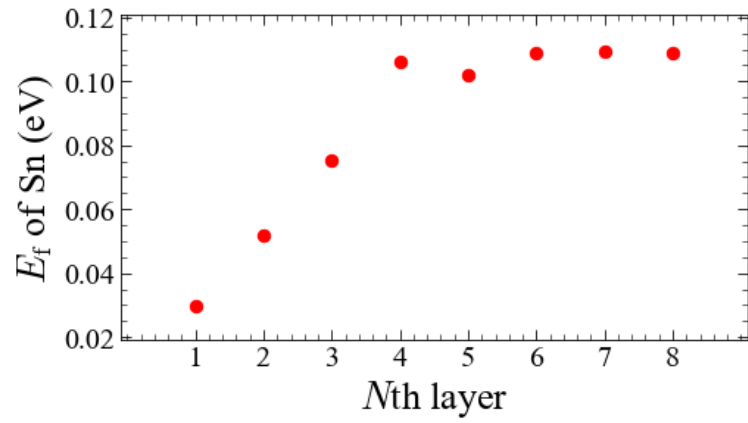


Fig. 2. E_f of the Sn atom in a GeSn (001) layer on a GaSb (001) substrate.

Defects identification, testing and screening for reliable SiC devices

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Performances of power devices are of paramount importance in energy consumption reduction in many practical applications. The roadmaps of modern power devices is driven by three major development pillars; a) novel elementary cell structure; b) advanced interconnects; c) use of different semiconductor materials (moving from Si to SiC and GaN). The focus of the presentation is to show how the introduction of SiC, with its superior electronic and thermal properties and in spite of problems linked to defects and higher costs compared to Si, has revolutionized the field of power devices. Today semiconductor companies are heavily using SiC in the production of power devices. In this talk it will be shown how the effort in reducing defects during crystal growth, mapping of residual crystallographic defects, testing and electrical screening of defective parts is used to guarantee reliable behavior of SiC power device in demanding applications in the automotive and industrial domain .

SiC color centers for quantum sensing: an Electro-Luminescence based approach for their investigation

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Many literatures focus on defects in Wide Band Gap (WBG) materials for Photonics and Quantum Technologies. Among WBG semiconductors, SiC stands out due to its technological maturity [1-7].

In this work, we introduced color centers into pn-junction 4H-SiC diodes. Building on prior literature and our own studies of ion irradiation effects, we irradiated the diodes with 40 keV He ions at a dose of $5 \times 10^{12} \text{ cm}^{-2}$ [1]. This energy was selected to target the pn-junction region, while the dose ensured sufficient defect concentration for diode operation and observable electroluminescence (EL) signal.

We combined electro-optical measurements with theoretical modelling, exploring a temperature range from 100 K to 450 K. This integrated approach allowed us to identify the types of defects present in the material, determine their localization in the device, and assess that electro-luminescence can only occur under specific configurations of the energetic levels of defects in their neutral and charged states.

Thermal treatments were also investigated through modelling and experimental approach for their impact on electro-optical performance. Results reveal that a mild anneal at $\sim 540 \text{ K}$ reorganizes defects within the crystalline matrix, significantly enhancing NIR emission ($\sim 930 \text{ nm}$) from silicon vacancies as observable in Figures. CL was also adopted for all the devices investigation but comparison with EL results showed only partial agreement: while peak positions aligned, a variation in peaks relative intensities post-annealing is only in the EL spectra. This discrepancy arises because EL and CL excite different defects; post-annealing lattice rearrangements favouring NIR color-center emission are detectable via EL but not CL. This confirms the fundamental role of our study, since if it had been conducted on passive material rather than on a device, and therefore using techniques other than EL, the effects of the mild thermal treatment would not have been revealed.

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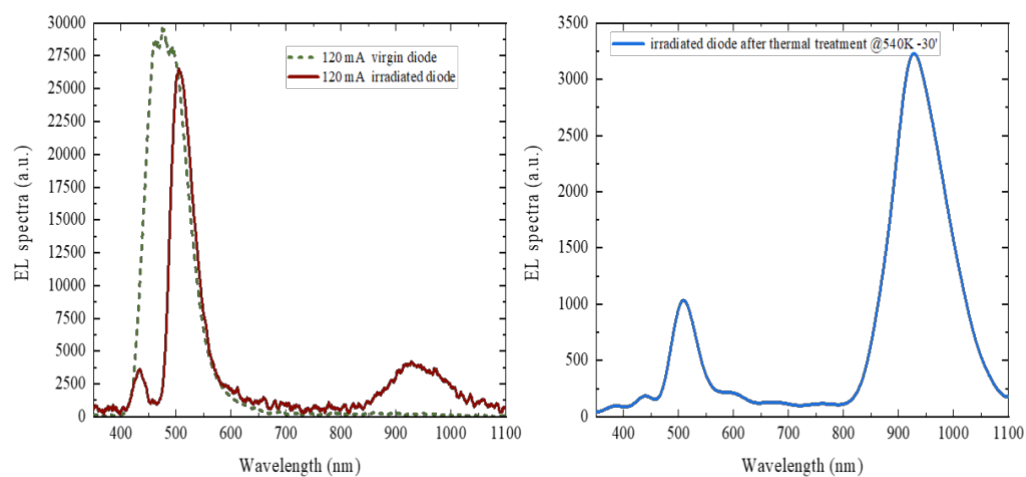
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Figures: on the left, Electro-luminescence spectra of a virgin diode and of a diode irradiated to introduce defects. A current of 120 mA was fixed for the luminescence pumping; on the right, spectrum of a diode irradiated and thermally treated. A relevant change in the ratio between peaks in the visible and in NIR region is observable due to the rearrangement of the crystalline matrix hosting Silicon vacancies of interest.

Benchmarking single Er^{3+} coherence in Silicon Carbide on Insulator-based micropillars

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Developing quantum emitters with long spin and optical time coherence in complementary metal-oxide-semiconductor (CMOS) platforms is a promising pathway towards optical quantum applications. Recently, excellent optical and spin coherence of trivalent Er ions was demonstrated in isotopically purified Silicon (Si) [1] and Silicon on Insulator (Si) [2, 3]. Here, we show the coherent optical control of single Er^{3+} ions in SiC micropillar arrays. These micropillars were fabricated in Silicon Carbide on Insulator (SiCOI), CMOS-compatible quantum material, implanted with 10^{16} Er/cm^3 . Single Er^{3+} ions in micropillar arrays were measured using sample-on-superconductor single photon detector (SSPD) method [1]. Micropillar arrays enabled ~ 0.1 collection efficiency of Er^{3+} optical signal when corrected for the SSPD detection efficiency. The measured linewidth of single Er^{3+} ions varied from ~ 1 MHz (limited by the wavemeter resolution and laser frequency stability) to ~ 10 MHz. The larger linewidth ions exhibited the top-hat line shape suggesting unresolved internal structure due to interactions with nearby Si and C nuclear, and Er electron spins. Optical Hahn coherence time measured for an ion with sub-MHz linewidth was ~ 30 μs . The observed narrowest Er^{3+} linewidth and optical coherence are superior to values measured in both Si^{28} , and SOI-based photonic cavities at similar implantation densities [4]. These results position Er^{3+} in SiCOI as a promising candidate for scalable and fully integrated on-chip quantum photonic systems.

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Exploring erbium quantum emission in CMOS compatible hexagonal Silicon Carbide on Insulator photonics

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Telecom C-band single-photon emitters (SPEs) with spin-carrying defects are vital for scalable quantum computing and secure fiber-based networks. Integrating these emitters into CMOS-compatible platforms like 4H-Silicon Carbide-on-Insulator (4H-SiCOI) enables long-distance communication without frequency conversion. Erbium ions (Er^{3+}) are ideal candidates due to their 1540 nm emission and robust optical coherence [1,2].

Our research progress is summarised. We demonstrated that ensemble Er^{3+} implanted in 4 inches wafer scale research grade 4H-SiCOI is robust at room temperature (RT) [3], outperforming silicon-on-insulator (SOI) benchmarks [4]. We also identified ion-clustering effects at high implantation doses [3]. At cryogenic temperatures, we performed high-resolution spectroscopy, observed sub-megahertz homogeneous linewidths and identified two stable lattice sites. By the characterisation of optical lifetimes and magneto-optical responses, we confirmed the platform's scalability for on-chip networks [5]. We successfully demonstrated RT single-photon emission from Er^{3+} in microring resonators and nanopillars, observing a Purcell enhancement of ~ 70 [6], overcoming traditionally low emission rates to achieve narrow (52 MHz) emission lines. Finally, we observed RT Zeeman splitting in single photon emitting ions, confirming that the quantum properties are preserved after nanofabrication. This work stems for the first demonstration of Er^{3+} integrated single photon emission at RT and paves the way to advance the current state of the art of single-photon sources, providing solutions compatible with existing photonic integrated circuits to achieve scalable operations within the telecommunication frequency band, enabling applications as quantum memory or spin-photon interfaces.

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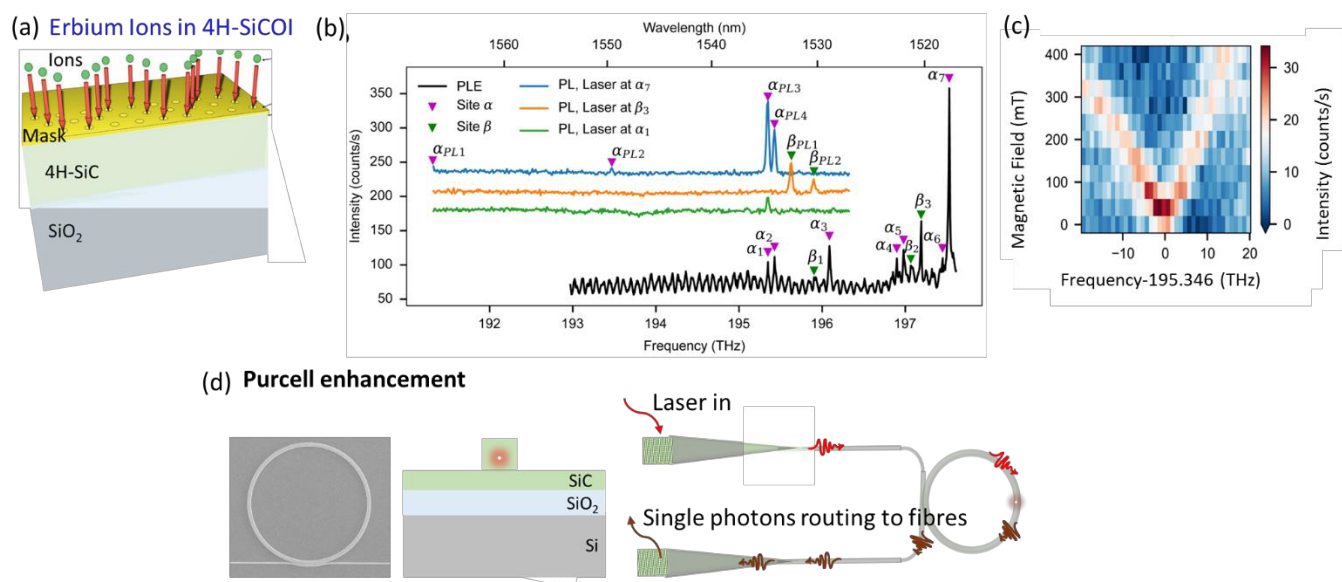


Fig. 1. Erbium emitters in 4H-SiCOI (a) Erbium ions implantation (b) PLE and PL at 20 mK of Erbium in 4H-SiCOI identifying narrow emission with Zeeman splitting (c). (d) Integrated single erbium emitters in 4H-SiCOI microring resonators.

Gate-defined quantum circuits in silicon-germanium heterostructures

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The enormous progress achieved in the experimental control of quantum mechanical few-level systems has opened the realm of implementing a novel paradigm of information processing: quantum computing. The physics of group IV semiconductor-based heterostructures offers sizeable assets to realize long qubit coherence times in condensed matter using gate-tunable electric circuits, allowing to leverage the processes of the current silicon chip industry.

In this presentation, I will discuss aspects which make silicon-germanium heterostructures unique to implement two types of qubits – *spin qubits* and *superconducting qubits* – within the same materials platform, based on similar gate-tunable field-effect thin film stacks.

I will show that spin qubits in isotope purified ²⁸Si/SiGe quantum well heterostructures are becoming a serious option in the quest for massively scalable qubit systems. In addition to isotope purification, details of the quantum well heterostructure design [1] as well as the interface with the field-effect stack [2] are important ingredients to reach longest spin qubit coherence times [3]. Design and processing principles are starting to be successfully transferred into heterostructure pilot lines [4] and into industrial production lines [5], allowing the industrial realization of prototype qubit chips [6].

I will also discuss how proximity-induced superconductivity in two-dimensional carrier systems in silicon-germanium heterostructures allows to realize gate-tunable superconducting junctions as well as microwave resonators, both of which represent central parts [7] of electronic circuitry for the realization of noise-protected superconducting qubit architectures as well as cryo-electronic components.

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UV-nanosecond laser hyperdoping of Ge/Si and SiGe/Si epilayers

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Germanium in the hyperdoping regime has attracted growing interest in recent years due to its tuneable electronic and plasmonic properties and bandgap narrowing. However, conventional in situ n-type doping in Ge often results in poor electrical activation, mainly due to low solid solubility, high dopant diffusivity, and the formation of dopant–vacancy complexes.

In this work, we demonstrate that thick Ge/Si and SiGe/Si layers, as well as shallow Ge/Si layers in-situ doped by Low Energy Plasma Enhanced Chemical Vapor Deposition, can be electrically activated through UV nanosecond Pulsed Laser Melting (PLM). This process induces ultrafast melting and recrystallization, enabling dopant incorporation into electrically active substitutional sites [1,2].

Van der Pauw–Hall (VdP–Hall) measurements reveal that, once the melting threshold is exceeded, activation reaches ~40% in SiGe and nearly 90% in Ge relative to the chemical concentration. Differential VdP–Hall indicates uniform activation across the entire layer thickness, yielding box-like dopant distributions. Laser energy density provides direct control of junction depth, spanning thick hyperdoped junctions for photonics and ultra-shallow junctions for nanoelectronics. In the ultra-shallow regime, explored here under PLM, the same activation trends are preserved, confirming the effectiveness of in-situ growth combined with PLM at extremely reduced thicknesses. Notably, when the melt front reaches the substrate interface, SiGe alloying occurs due to intermixing, suggesting PLM as a route for local composition and property engineering.

Finally, successful device integration of thick and ultra-shallow junctions requires both surface preservation and thermal robustness [2,3]. AFM verifies that PLM maintains high surface quality, and a thermal stability study based on rapid thermal annealing combined with reflection spectroscopy and VdP–Hall measurements shows rapid deactivation of hyperdoped Ge above 300 °C, whereas SiGe exhibits significantly greater stability.

Overall, in-situ growth plus PLM provides a single, scalable pathway to design hyperdoped junctions.

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[3] M. Faverzani, S. Calcaterra, P. Biagioni, and J. Frigerio, “Strong coupling in metal-semiconductor microcavities featuring Ge quantum wells: a perspective study,” *Nanophotonics*, vol. 13, no. 10, pp. 1693–1700, Apr. 2024, doi: 10.1515/nanoph-2023-0730.

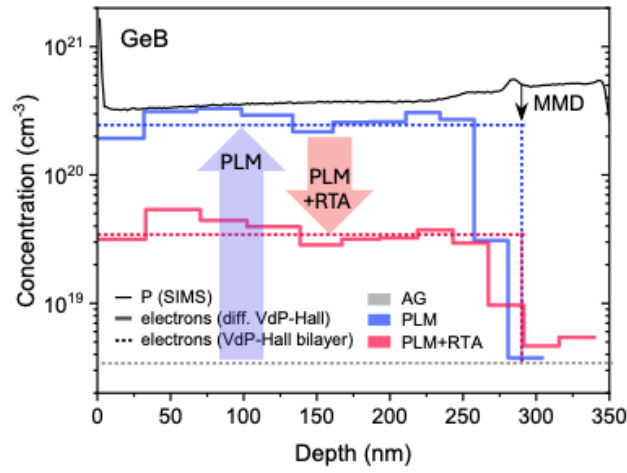


Fig. 1. Carrier depth profiles (solid colored lines) obtained from differential VdP–Hall measurements on Ge:P/Si are compared with phosphorus SIMS profiles (solid black lines). Results are shown for the as-grown sample (gray), after PLM at 0.9 J/cm^2 (blue), and after subsequent 10 min isochronal RTA steps (red) from 150 to 325°C in 25°C increments. Dashed lines report the active carrier concentration from standard VdP–Hall analysis using the bilayer model.

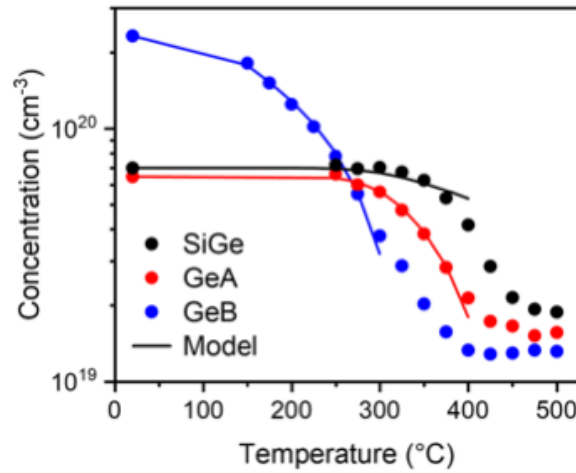


Fig. 2. Electron density versus annealing temperature for Ge:P (GeA, GeB) and SiGe:P during stepwise isochronal anneals, illustrating thermal deactivation. Filled markers are obtained from FTIR reflectivity, open markers from conventional VdP–Hall measurements, and solid lines denote the model predictions.

Crystallization of Sn-rich Si and Ge thin films by flash lamp annealing

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Sn-rich Si and Ge materials are of high interest for various applications such as high-mobility electronic devices, Si-based light emitters, IR photodetectors, and thermoelectrics. Unfortunately, the solid solubility limit of Sn in Si and Ge is very low, and the incorporation of Sn introduces significant lattice disorder and triggers the formation of defects. In addition, the desired process of crystallization and the unwanted processes of diffusion and segregation are closely linked to each other. In order to achieve Sn concentrations above the solubility limit, non-equilibrium fabrication methods like ion implantation or flash lamp annealing (FLA) are required.

In this contribution we discuss the use of FLA to crystallize amorphous layers of Sn-rich Si and Ge compounds. The layers were made by molecular beam epitaxy, magnetron sputtering or ion implantation, followed by FLA. The different examples show that the segregation of Sn also depends on co-doping. In detail, very high phosphorous concentrations tend to foster Sn segregation, whereas carbon prevents or delays it to some extent.

Ex-situ incorporation of Al in Ge by sputter deposition and pulsed laser melting: a new approach to fabricate hyper-doped Ge:Al alloys.

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Ge-based alloys have attracted considerable interest over the last two decades due to their promising properties for high-performance nanoelectronics, mid-infrared photonics, gamma- and X-ray radiation detectors, and quantum computing. A key challenge is the fabrication of alloys incorporating high concentrations of electrically active dopants. In recent years, nanosecond Pulsed Laser Melting (PLM) has emerged as a powerful technique to overcome the limitations of conventional out-of-equilibrium growth processes, such as epitaxy, enabling improved dopant incorporation and activation [1,2].

In this work, hyper-doped Ge:Al films were fabricated through a novel approach combining two-step RF sputter deposition and subsequent PLM [3]. The method consists of sequential deposition of a thin Al layer followed by an amorphous Ge capping layer to prevent Al oxidation before and during laser processing (fig. 1). Laser treatments were performed under a broad range of experimental conditions, using single or multiple pulses and finely tuning the Energy Density (ED).

To achieve an in-depth understanding of the melting and recrystallization mechanisms, including Al diffusion and electrical activation, a comprehensive set of electrical, structural, and chemical characterizations was carried out. SIMS analyses were employed to determine Al concentration profiles and detect possible contaminants. Van der Pauw-Hall measurements allowed evaluation of carrier concentration and mobility, revealing a hyper-doping regime with hole concentrations exceeding $1 \times 10^{21} \text{ cm}^{-3}$ (fig. 2). Surface morphology and microstructure were investigated by AFM and SEM/TEM techniques, enabling direct observation of lattice reconstruction and the formation of Al-rich regions after laser irradiation. Raman spectroscopy was correlated with the other analyses to provide insight into amorphous-to-crystalline phase transformations and the contribution of active dopants to Raman peak shifts.

Overall, this work demonstrates that PLM is an effective strategy for ex-situ p-type doping of Ge and offers an interpretative framework for understanding laser-induced recrystallization under different processing conditions.

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[2] E. Di Russo et al., Fully relaxed Ge_{0.9}Sn_{0.1}/Ge by Sn/Ge deposition and nanosecond pulsed laser melting, *Applied Surface Science* 612, 155817 (2023).

[3] E. Di Russo et al., Ex-situ incorporation of Al in Ge by sputter deposition and pulsed laser melting: a new approach to fabricate hyper-doped Ge: Al alloys. *Applied Surface Science*, 710, 163946 (2025).

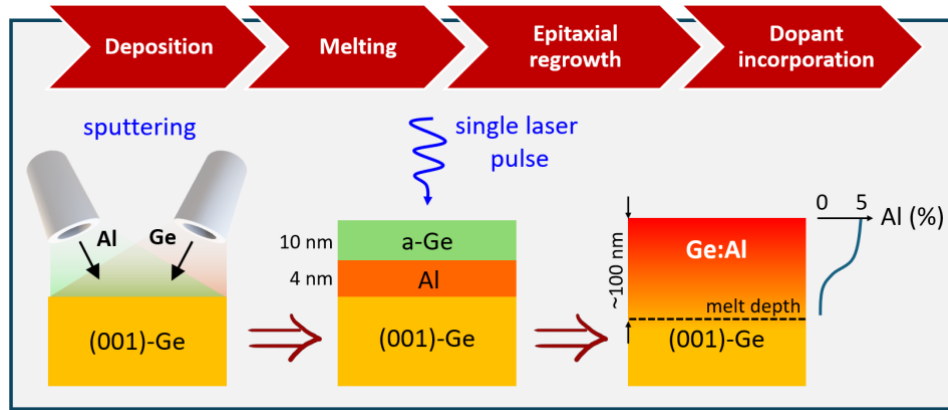


Fig. 1. Schematic illustration of the two-step sputter deposition followed by pulsed laser melting for the fabrication of hyperdoped Ge:Al samples.

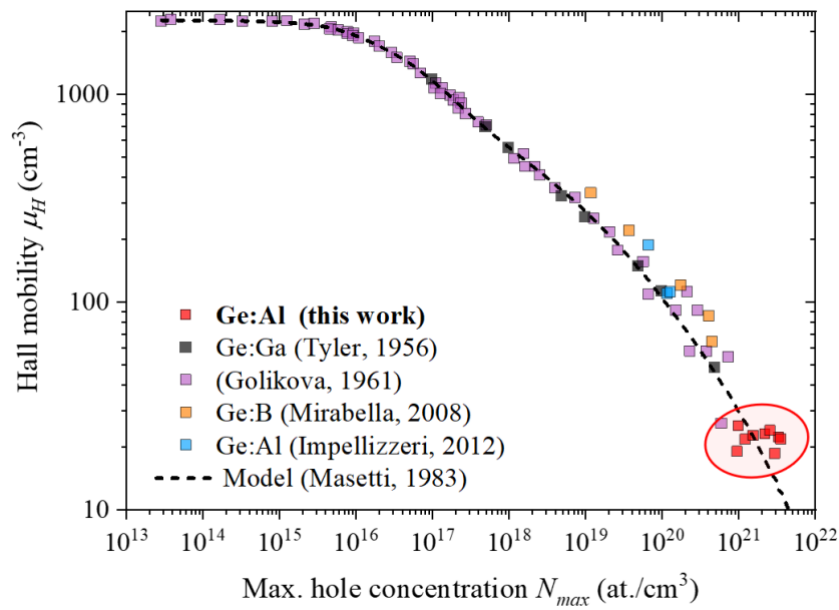


Fig. 2. Hall mobility μ_H versus maximum hole concentration N_{max} in Ge:Al samples.

Positron trapping in highly *p*-type Ge

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Point defects play an important role for the electronic properties of semiconductor materials. Positron Annihilation Spectroscopy is a unique method for characterizing and quantifying neutral and negatively charged vacancy-type defects. However, *p*-type Ge has been researched very little using Positron Annihilation Spectroscopy due to the low sensitivity of the method to positively charged defects.

Here, we studied highly Ga-doped and B-doped Czochralski-grown Ge, with doping concentrations of 10^{18} - 10^{20} and 5×10^{17} cm⁻³, respectively. Comparing gallium and boron is particularly interesting as both are *p*-type dopants, while differing in both size and electron structure. Both as-grown and proton irradiated samples were studied. In all samples, both as-grown and irradiated, a positron trap with an unusual behavior is observed at temperatures below RT.

Positron Annihilation Lifetime Spectroscopy measurements showed a decrease in positron lifetime as a function of temperature [1]. This is typical for negative ion trapping and could be related to the high *p*-type doping. However, this is to some extent unexpected, considering that most of the samples are degenerate. Even more surprisingly, the positron lifetime dropped below that of the positron trap free reference sample, indicating that the electron density of this trap is higher than the electron density in the interstitial region of the reference sample. This effect has not previously been observed in any semiconductor material, *n*- or *p*-type.

To study this positron trapping state in more detail we employed the 2D-Coincidence Doppler Broadening Spectroscopy technique, which allowed us to investigate how the electron momentum distribution differs at the abnormal annihilation state. In addition, we performed DFT calculations to further study this effect. These results and their implications will be discussed in the presentation.

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GeSn Semiconductors: A Tale of Defects and Devices

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Germanium-tin (GeSn) alloy is a leading group-IV platform for extended short-wave infrared (e-SWIR) and mid-infrared photonics, offering bandgap tunability, direct-gap behavior, and monolithic integration on silicon. Yet GeSn is intrinsically metastable: the equilibrium solubility of Sn in Ge is below 1 at.%, while device-relevant compositions require an order of magnitude higher Sn content. As a result, defects are not peripheral, but they define both the limitations and the opportunities of the material.

This talk attempts to present a unified view of GeSn from defects to devices, showing how dislocations, strain relaxation, and vacancy complexes govern solute transport, phase stability, and ultimately optoelectronic performance. Atomic-scale investigations reveal that once the alloy approaches its thermodynamic instability, dislocation pipe diffusion becomes a dominant pathway for Sn migration, driving surface segregation and compositional inhomogeneity. Rather than being merely detrimental, these mechanisms expose the kinetic and strain-mediated levers that control high-Sn epitaxy. By engineering strain relaxation in, Sn incorporation exceeding ~25 at.% can be achieved while mitigating phase separation, establishing practical design rules for metastable growth.

Point defects provide the second critical axis of control. Positron annihilation and complementary analyses identify vacancy complexes, primarily divacancy-related defect, in nonequilibrium GeSn alloys. These open-volume defects may influence carrier lifetime, recombination dynamics, and leakage currents, linking growth conditions directly to device metrics. Understanding and managing these defects is therefore essential to translate materials advances into functional photonic components.

Building on these defect-aware studies, we discuss the performance of GeSn devices. These include photodetectors and light emitters. Device architectures such as microbridge geometries further illustrate how strain engineering and thermal management intersect with materials quality to enhance efficiency and operating stability. Together, these results highlight the need to understand defect physics and provide the basis to discuss the path to scalable and practical GeSn optoelectronics devices.

Material and Design Trade-offs in GeSn-Based MQW Lasers on Silicon

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Mid-infrared laser sources monolithically integrated on silicon are highly desirable for applications in sensing, communications, and on-chip spectroscopy, particularly when realized in CMOS-compatible group-IV material systems. GeSn alloys have emerged as a promising platform for monolithic integration of photonics, electronics, and spintronics owing to their tunable direct bandgap, advantageous spin properties, including strong spin-orbit coupling and long spin coherence times, and CMOS compatibility [1–3]. In this work, laser structures based on bulk GeSn, GeSn and GeSn/(Si)GeSn MQWs are compared to evaluate the advantages of quantum confinement and heterostructure engineering for improved device performance.

We systematically study GeSn-based bulk and MQW designs with varying Sn compositions and compare barrier layers with and without silicon incorporation. The analysis focuses on the fundamental trade-off between achieving low lasing threshold and maintaining high operating temperature. Increasing the Sn content in the wells enhances bandgap directness and optical gain, enabling reduced threshold. However, high Sn fractions also introduce stronger compressive strain, increased defect density, and enhanced carrier leakage, which degrade material quality and thermal stability. Lower Sn contents improve crystalline quality but require higher carrier densities to reach population inversion. For MQW heterostructures, barrier composition strongly influences carrier confinement: SiGeSn barriers provide larger band offsets and suppress thermally activated carrier escape, whereas Si-free GeSn barriers reduce strain but offer weaker confinement and faster thermal quenching.

Additionally, the under-etched cavity geometries used in this work, which improve optical confinement and reduce strain in the free-standing rim where whispering gallery modes form, impose stringent constraints on heat dissipation. Reduced thermal coupling to the substrate limits heat removal and introduces additional requirements for resonator design. Experimental results indicate that the present micro-disk and micro-ring cavities are thermally limited rather than gain limited, highlighting the need for improved thermal management and cavity engineering to advance high-performance GeSn-based lasers on silicon.

This work was funded by the European Union's Horizon Europe research and innovation program under the grant agreement no. 101070208 (LASTSTEP project).

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Room-Temperature Optical Gain Analysis in Biaxially Strained Bulk GeSn for Mid-Infrared Silicon Photonics

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Monolithic integration of Group-IV light sources on silicon is the central objective of CMOS-compatible photonics, particularly for mid-infrared (MIR) gas sensing and on-chip spectroscopy [1–5]. GeSn alloys grown by non-equilibrium RP-CVD on Ge virtual substrates offer a tunable direct-bandgap platform in the 2–5 μm range: Sn incorporation reduces the Γ -valley energy faster than the L-valley, while epitaxial strain engineering increases the Γ -L valleys spacing to further enhance bandgap directness.

We present a comprehensive optical gain analysis of bulk GeSn under biaxial strain, targeting the MIR gas-sensing windows at 3.3 μm and 2.8 μm . The electronic band structure is evaluated using 8-band $k\cdot p$ model based on Bahder's Hamiltonian, with Sn-related Varshni and bowing parameters calibrated against photoluminescence data. The net material gain is computed as the sum of direct interband transitions, intervalence-band absorption (IVBA), and free-carrier absorption (acoustic and optical phonon, alloy disorder, and ionized impurity scattering), separately resolved for TE and TM polarizations over biaxial strain from -0.5% to $+0.2\%$.

For $\text{Ge}_{0.844}\text{Sn}_{0.156}$ at room temperature ($T = 293\text{ K}$), positive net gain is achievable at 3.3 μm under specific strain and carrier-density conditions. Strain-driven valence-band mixing yields pronounced TE/TM polarization selectivity, enabling strain-controlled optical response at fixed wavelength. At 2.8 μm , stronger interband and hole-related absorption prevents net gain under identical conditions, highlighting the role of unintentional p-type background doping, linked to bulk point defects and the misfit dislocation network at the GeSn/Ge-VS interface, in constraining the transparency density. Decreasing compressive strain is identified as a prerequisite for positive net gain at room temperature.

These results provide quantitative design rules for Sn composition, strain state, and doping in (Si)GeSn multilayer heterostructures targeting waveguide-integrated and microdisk MIR laser cavities on silicon.

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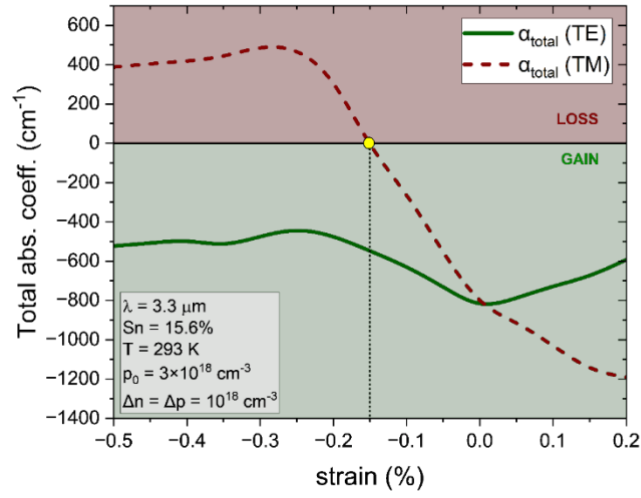


Fig. 1. Total absorption coefficient α_{total} (negative values = net optical gain) at $\lambda = 3.3 \mu\text{m}$ in bulk GeSn (Sn = 15.6%) at T = 293 K, as a function of biaxial strain (−0.5% to +0.2%), for TE (solid) and TM (dashed) polarizations. Background p-type doping ($p_0 = 3 \times 10^{18} \text{ cm}^{-3}$); injected electron and hole densities $\Delta n = \Delta p = 10^{18} \text{ cm}^{-3}$. TE polarization has net gain across most of the compressive-strain range, while TM polarization transits from loss to gain around −0.2% strain, demonstrating strain-controlled polarization selectivity in the MIR gain window.

MBE Growth of Sn/Ge MQW Structures

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Due to its unique electronic and optical properties, the GeSn material system is gaining increased importance. The formation of a direct band structure, in particular, makes it interesting for the realization of efficient light-emitting diodes (LEDs) and lasers on Si substrates. The epitaxial growth of GeSn alloys in a diamond lattice on a Ge surface proves to be extremely difficult. This difficulty results from the existence of two different Sn phases (diamond lattice α -Sn, metallic tetragonal β -Sn), the lattice mismatch between the two elements (approx. 14.7%), the extremely low equilibrium solubility of Sn in Ge (approx. 1%), and massive demixing phenomena. One possibility to produce GeSn alloys above the solubility limit is the growth under non-equilibrium conditions, i.e., at very low growth temperatures. However, low growth temperatures favor the formation of excessive point defects or even the collapse of crystal growth into an amorphous state. Another possible solution is the growth of multi-quantum wells (MQW) consisting of several monolayers of Sn, each overgrown with Ge.

Here we present the epitaxial growth of Sn/Ge MQW structures in a p-type/intrinsic/n-type (PIN) semiconductor stack. Molecular beam epitaxy (MBE) is employed for this purpose. The MQWs consist of two monolayers of Sn separated by a Ge barrier of thickness t_b and stacked a total of five times. The schematic setup of the entire structure is shown in Fig. 1a). In a sample series, the thickness of the Ge barrier is varied between 5 nm and 40 nm. First, we thoroughly investigated the structural properties of MQW with different barrier thicknesses. Material analyses performed using high-resolution x-ray diffraction, secondary ion mass spectroscopy, and scanning transmission electron microscopy confirmed the excellent quality of our ultrathin GeSn QW layers, which feature well-defined interfaces and a tin content exceeding 4 atomic percent. We then operated the fabricated diodes in the forward region as LEDs. In a cryostat, we investigated the electroluminescence (EL) of the devices between 12 K and room temperature (see Fig. 1b). We observed a light emission spectrum extending well beyond the telecommunications U-band into the short-wave infrared range.

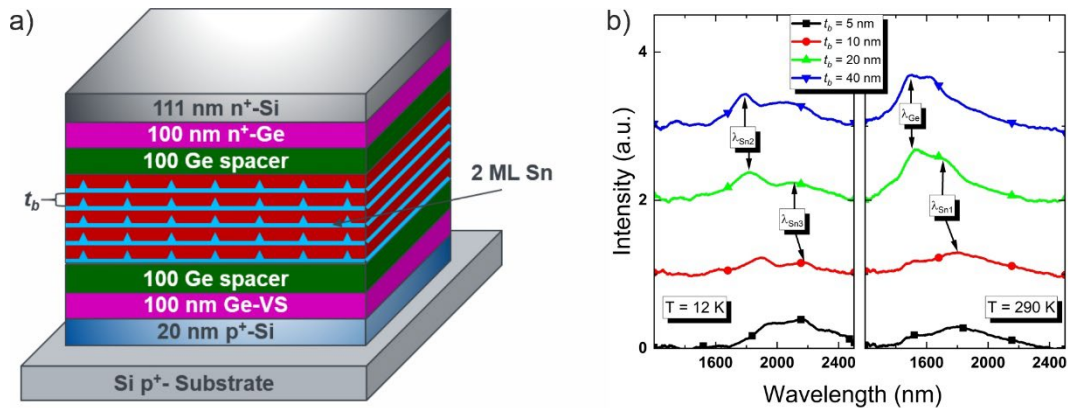


Fig. 1. a) Schematic structure of a Sn/Ge MQW PIN device stack. b) EL spectra of all investigated Sn/Ge MQW at 12 K and room temperature at a constant current.

Germanium tin on insulator, a suitable platform for electrically driven Mid-IR emitters and detectors

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The development of high-performance Group-IV optoelectronics in the mid-infrared (MIR) has long been hindered by the high density of threading dislocations originating from the lattice mismatch between GeSn and Ge-buffered silicon substrates. While optical pumping resulted in lasing up to room temperature in GeSn alloys [1,2], transitioning to efficient electrically driven devices requires a paradigm shift in material integration [3,4].

The GeSnSOI platform offers a twofold advantage [5]: first, it enables the complete removal of the defect-heavy buffer layers through wafer bonding and etch-back processes, resulting in high-crystalline quality active layers. Second, the high refractive index contrast between the GeSn layer and the underlying buried dielectric provides a drastic improvement in optical confinement. This enhanced confinement, which was instrumental in achieving room-temperature lasing under optical excitation [1,2,6], is now leveraged for carrier injection schemes.

We demonstrate the feasibility of integrating these high-quality layers into PIN diode heterostructures, including quantum heterostructures, designed for electrical pumping. Experimental results show I-V characteristics with low leakage currents, confirming the superior material quality of the transferred GeSn layers. Furthermore, this platform proves highly effective for integrated detectors, exhibiting room temperature extended cut-off wavelengths up to 3 μm . They can be extended to even higher values thanks to the strain-engineering possibilities offered by GeSnOI [6].

Our results indicate that the GeSnOI platform not only bypasses the structural limitations of traditional epitaxy but also provides a scalable, CMOS-compatible route toward fully integrated MIR transceivers and sensors. We conclude by discussing the path toward performant electrically-pumped GeSn lasers by leveraging these optimized diode architectures and superior modal gain.

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SiGeSn Technology for Monolithic Infrared Silicon Photonics

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All-group-IV SiGeSn semiconductors have attracted increasing attention recently for the development of infrared optoelectronic devices. In this work, SiGeSn alloys were grown on Si substrates using a commercial CVD reactor with low-cost precursors. The research progress on optically pumped and electrically injected lasers as well as photodetectors operating in broad IR wavelength range will be presented.

Improving the performance of GeSn infrared photodetectors on Si through nanoscale engineering

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Over the last decade, direct band gap GeSn semiconductors grown on a Si wafer have been established as a promising monolithic platform for infrared photonic devices (photodetectors, lasers, and LEDs) that are essential to infrared imaging and sensing technologies.[1-4] The essence of the GeSn materials lies in the possibility to exceed by one order of magnitude the equilibrium solubility of 1 at.% Sn in Ge and achieve an indirect to direct band gap transition above 8 at.% Sn. The ability to control the composition of GeSn thus enables a wealth of passive and active photonic devices in the short-wave infrared (SWIR: 1.5-3 μm) and mid-wave infrared (MWIR: 3-5 μm), and potentially longer wavelengths. Moreover, nanostructuring GeSn into ordered arrays of nanowires (NWs) boosts the infrared optical absorption through leaky-mode resonance (LMR) peaks that can be tailored with the dimensions of the NWs.[5]

In this presentation, we will discuss the growth, structural, and optoelectronic device properties of $\text{Ge}_{0.92}\text{Sn}_{0.08}$ NW arrays photodetectors fabricated from a thin film sample grown on a Si wafer. The photodetector operates at room-temperature with controllable LMR peaks until the 2.6 μm cut-off wavelength, hence covering the majority of the SWIR. The NW arrays show enhanced optical absorption and emission compared to the planar samples. These experimental findings are further supported by Finite-Difference Time-Domain (FDTD) simulations. This nanoengineered platform has the potential to cover longer wavelengths into the MWIR by increasing the Sn content of the samples. To this end, we will demonstrate the control of the LMR in a prototype MWIR $\text{Ge}_{0.89}\text{Sn}_{0.11}$ NW array photodetector with a 3.4 μm cut-off.

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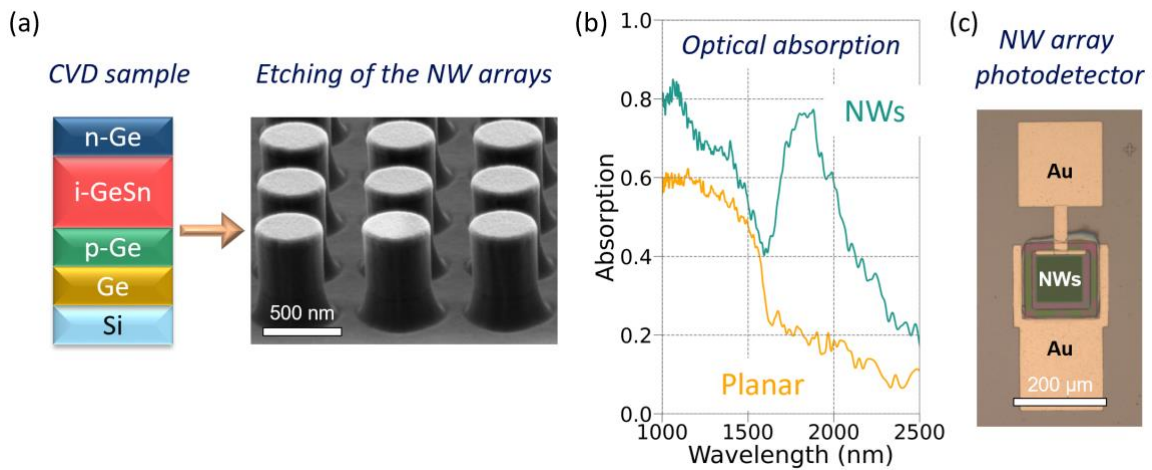


Fig. 1. (a) Schematics of the p-Ge/i-GeSn/n-Ge p-i-n multi-layer heterostructures grown on Si wafer using CVD and SEM of an etched GeSn NW array. (b) Optical absorption measurements of the NW array showing a cut-off wavelength of 2.6 μm at room-temperature and LMR peaks that are controlled by the NW geometrical parameters. (c) Optical image of a NW photodetector.

Influence of Electrode Geometry and Thermal Annealing on the Electroluminescence of GeSn LEDs

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Germanium-tin (GeSn) alloys are emerging as promising CMOS-compatible materials for monolithic mid-infrared emitters, as they exhibit a direct bandgap when the Sn content is high enough (8% in relaxed layers, typically). They can also be epitaxially grown on 200 mm Ge-buffered silicon wafers. In this study, we examine vertical p-i-n GeSn light-emitting diodes (LEDs) containing up to 16% of Sn, which were grown using reduced-pressure chemical vapour deposition on Ge strain-relaxed buffers. Circular mesa LEDs were fabricated with diameters ranging from 50 to 200 μm and various top electrode geometries (including dot, flower and spider-web designs), in order to study their influence on carrier injection and optical emission.

Room-temperature electroluminescence was characterised under current injection using FTIR spectroscopy, while infrared surface imaging with an InSb camera provided insight into current spreading and emission uniformity. Devices with smaller mesa diameters exhibited higher integrated electroluminescence intensities. Infrared imaging revealed localised emission near the injection contacts, highlighting the impact of current crowding limited by p- and n-type doped layers (Fig. 1a and 1b). Using these guidelines, arrays of even smaller diameter mesas were subsequently fabricated and characterized before and after annealing, leading to a 17% enhancement in electroluminescence, suggesting defect curing and a reduction of non-radiative recombination pathways (Fig. 1c).

Our results demonstrate the critical role of contact design in optimising carrier injection and the interest of using post-growth thermal treatments in order to improve internal quantum efficiency. The integration and operation of these LEDs in a dedicated gas cell will be discussed.

Acknowledgment: This work was supported by the European Union's Horizon 2020 LASTSTEP Project under grant agreement ID: 101070208, the IPCEI Microelectronics and Connectivity project. It was also supported by the French Public Authorities within the frame of France 2030.

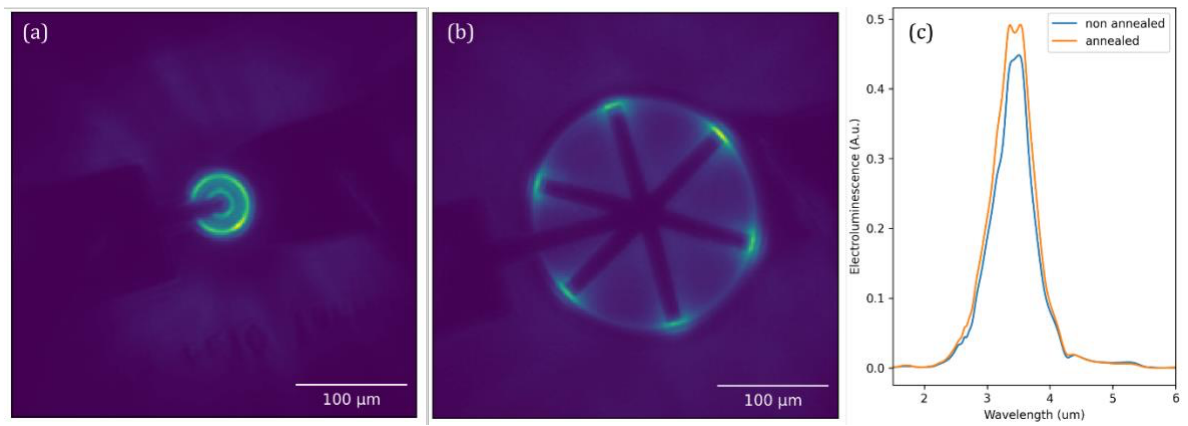


Fig. 1. Infrared images acquired with an InSb camera of Ge_{0.846}Sn_{0.154} LEDs with a dot (a) and flower (b) top contacts shape under a current injection of 150 mA. (c) Spectra of annealed and not annealed Ge_{0.846}Sn_{0.154} LED arrays for an injection current of 150 mA.

High Sn content GeSn-based Avalanche PhotoDiode for Medium InfraRed detection

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The integration of Sn into the Ge lattice offers a promising route for extending the operational wavelength of Group-IV photodetectors into the Mid-InfraRed (MIR) range. Particularly, a Sn content exceeding 11% must be employed to extend absorption into the MIR range and to guarantee GeSn direct bandgap despite a residual compressive strain [1]. However, the low equilibrium solubility of Sn in Ge requires GeSn epitaxy to be performed at relatively low temperatures, promoting the formation of crystalline defects.

Avalanche PhotoDiodes (APDs) enhance signal detection by leveraging impact ionization for charge multiplication. However, GeSn APD architectures must be engineered to counteract degradation from the low crystalline quality of epitaxial GeSn. To this aim, we present a mesa SACM GeSn-based APD (Figure 1). Compared to state-of-the-art GeSn APDs [2][3][4], we included a high Sn content, bulk GeSn absorption layer for detecting photons beyond 3 μm . Devices with 1.3 and 0.3 μm Ge strain-relaxed-buffers (SRBs) were fabricated to investigate crystal quality and GeSn layer depletion. The epitaxial layer stacks were characterized with XRD-RMS and RBS techniques, providing insights into Sn incorporation and crystal quality (**Error! Reference source not found.**). Electro-optic characterization of the devices is presented in Figure 3. The I-V characteristics of the thin Ge-SRB APD exhibit a ~ 2000 -fold dark current increase compared to its thick Ge-SRB counterpart, as well as a “smooth” transition to the breakdown region. These features are clear indicators of high defect density within the thin Ge-SRB device's active region. Conversely, the thin device exhibits higher responsivity due to more efficient carrier transport through the Ge buffer [2]. As expected, responsivity scales with bias voltage, and the cut-off wavelength experiences a red shift with increasing temperature. The thick SRB APD achieves lower Noise Equivalent Power (NEP) as its significantly reduced dark current, stemming from superior crystal quality, outweighs its lower responsivity.

This work was funded by the European Union's Horizon Europe research and innovation program under the grant agreement no. 101070208 (LASTSTEP project).

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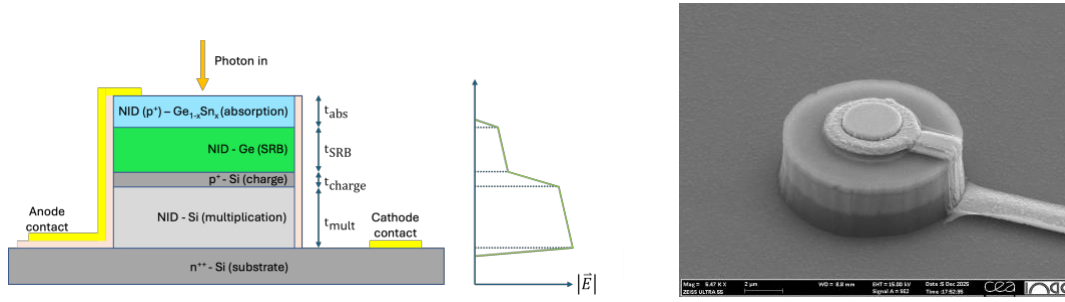


Figure 1- (Left) SACM (Separated-Absorption-Charge-Multiplication) GeSn APD cross-section with a qualitative representation of the electric field profile inside the active volume. (Right) SEM image of a fabricated device.

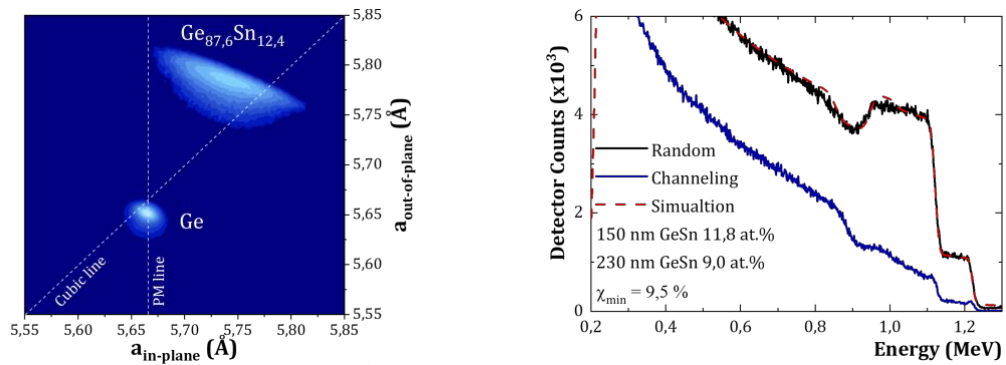


Figure 2 – (Left) XRD-RSM characterization of the thick SRB GeSn APD. The $\text{Ge}_{87.6}\text{Sn}_{12.4}$ layer is almost fully relaxed on the Ge SRB. (Right) RBS measurement of the thick SRB GeSn APD. The experimental data are accurately fitted by a simulated model assuming a dual-layer $\text{Ge}_{88.2}\text{Sn}_{11.48}$ and $\text{Ge}_{81}\text{Sn}_9$ configuration with 150 and 230 nm thickness, respectively.

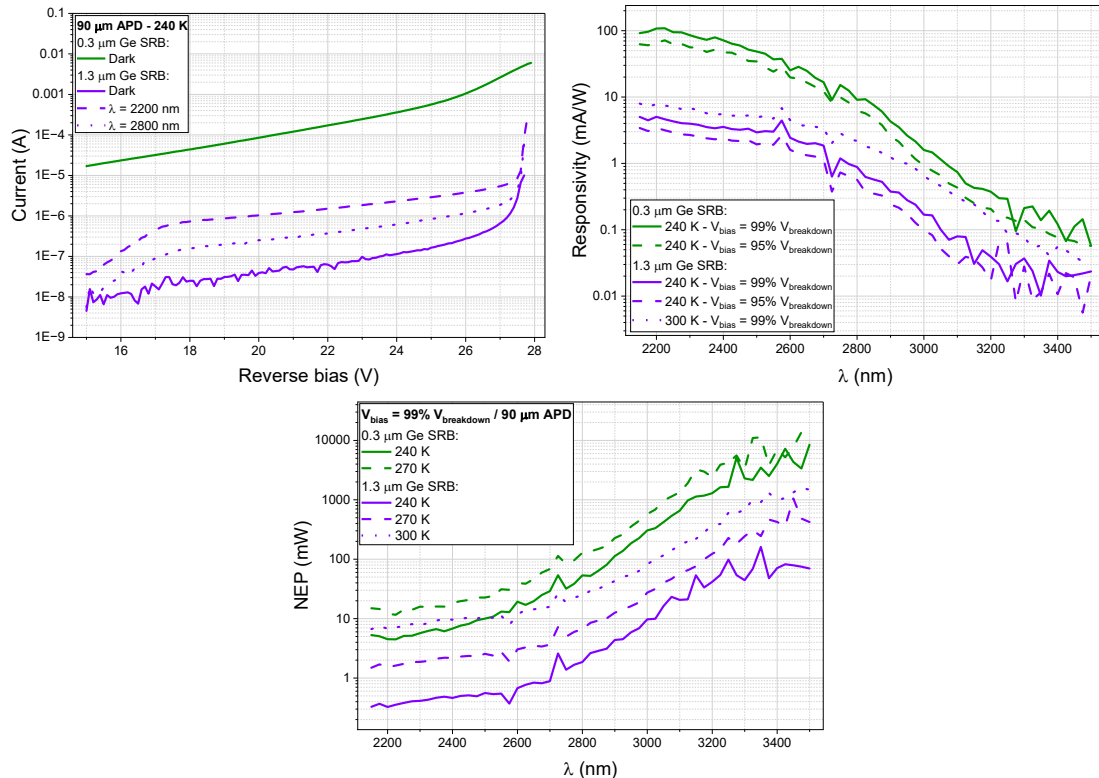


Figure 3 – (Left, Top) Dark currents of APDs with 0.3 and 1.3 μm SRB and photocurrent at 2200 and 2800 nm for the 1.3 μm SRB APD. (Right, Top) Spectral responsivity at different temperatures and bias conditions. (Bottom) Calculated NEP at 99% of the breakdown voltage.

Operando study of device heating using full-field x-ray diffraction microscopy

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Lattice strain critically determines the electronic and optical behavior of semiconductor optoelectronic devices, influencing band structure, gain, and thermal response. Mapping its spatial distribution with high resolution in fully fabricated, operating devices remains a major experimental challenge, especially for embedded active layers and fast transient processes. Conventional techniques lack either the necessary sensitivity, spatial resolution, or the capability for non-destructive operando measurements.

In this work, full-field x-ray diffraction microscopy (FFDXM) in stroboscopic mode was used to investigate strain dynamics in an electrically pumped SiGeSn/GeSn multi-quantum-well microdisk laser at the ESRF ID01 beamline [1]. FFDXM is a diffraction-based imaging technique that provides real-space maps of lattice strain and crystal orientation in buried layers with high spatial and angular resolution, while preserving the device structure. In the stroboscopic configuration, short X-ray pulse trains are synchronized with electrical excitation, enabling time-resolved imaging of lattice evolution during operation with ~150 nm spatial and <10 ns temporal resolution.

The device was operated at 120 K under 100 ns current pulses of 150 mA, conditions comparable to those required for lasing [2]. By recording FFDXM images at controlled delays between the electrical and X-ray pulses, the transient lattice expansion caused by Joule heating was directly visualized. The measurements revealed that heat accumulation is highly localized in the Ge bottom contact layer, which exhibits a temperature increase of approximately 70 K. In contrast, the microdisk active region shows significantly slower and nearly undetectable thermal expansion on the same timescale, indicating efficient thermal isolation and a delayed heat transfer to the gain medium.

The spatially resolved strain maps identify the regions of maximum thermal load and provide insight into the device's heat dissipation pathways. The experimental observations show excellent agreement with multi-physics thermal simulations, validating both the measurement approach and the device model.

These results demonstrate that stroboscopic FFDXM enables non-destructive, nanoscale, operando visualization of fast thermally induced strain in complex semiconductor lasers. This capability provides a powerful tool for optimizing thermal management, improving reliability, and guiding strain engineering in advanced group-IV optoelectronic devices.

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Ab Initio Modeling of Surface-Induced Effects on Quantum Gate Fidelity in 3C-SiC Divacancy Qubits

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The development of scalable solid-state in wide-bandgap based quantum technologies, ranging from high-sensitivity quantum sensors to quantum computation, critically depends on the deterministic engineering of point defects in these materials [1]. The neutral silicon-carbon divacancy $V_{\text{Si}}V_{\text{C}}^0$ in cubic silicon carbide (3C-SiC) has emerged as a leading qubit platform due to its long spin coherence times, optical addressability, and integrability with mature microelectronic fabrication processes.

However, practical device integration often requires positioning these qubits in close proximity to surfaces, where broken crystalline symmetry, surface reconstruction, and the presence of nuclear spin environments introduce perturbations to the defect's spin Hamiltonian. A quantitative understanding of these surface-induced effects is therefore essential for enabling high-fidelity quantum operations in realistic device architectures.

In this work, we present systematic investigation of surface-induced perturbations at the 3C-SiC(001)-(2×1):H reconstructed surface. Using first-principles Density Functional Theory (DFT) calculations, we characterize the modulation of the Zero-Field Splitting tensor as a function of defect depth (0.6–1.2 nm) and crystallographic orientation (basal versus axial configurations, see Figure 1) [2]. We thereon compute the hyperfine coupling tensors between the divacancy electron spin and the nuclear spins associated with the hydrogen passivation layer.

These ab-initio hyperfine parameters establish the microscopic foundation for evaluating the performance of two-qubit logic operations in near-surface architectures. In particular, we consider the Controlled-Rotation (CROT) gate [3], where the electron spin of the divacancy acts as a control qubit coupled to surface-bound nuclear spins. Furthermore, we investigate the potential impact of isotopic surface engineering as a strategy to tailor the hyperfine landscape and modify nuclear spin-bath dynamics.

Ongoing quantum dynamics simulations aim to quantify how surface-induced variations in the hyperfine interaction influence gate fidelity and operational robustness. This integrated approach, combining predictive materials modelling with quantum control protocols, provides a framework for the rational design of SiC-based quantum devices. In this context, isotopic engineering emerges as a promising pathway to further refine the local spin environment and enhance the stability of quantum gate operations in near-surface architectures.

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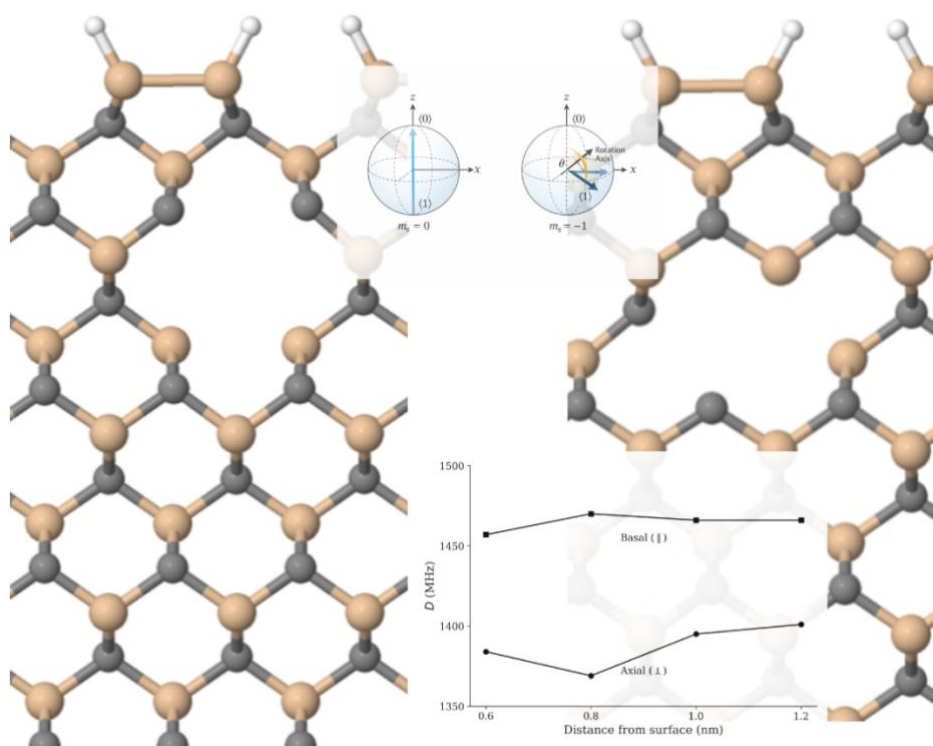


Fig. 1. Axial ($\perp$) and basal ($\parallel$) configurations of the $V_{Si}V_C^0$ and respective trends of component D of the ZFS tensor (inset) as depth varies in the atomistic model of a $(2 \times 1):H$ reconstructed 3C-SiC surface.

Atomic-scale mechanism of step-edge-induced stacking fault evolution during HVPE growth of (100) β -Ga₂O₃

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β -Ga₂O₃ has emerged as a promising semiconductor for high-voltage/high-frequency electronics, due to its ultrawide bandgap (~ 4.8 eV) and remarkable theoretical breakdown field strength (8 MV cm^{-1}). In pursue of the commercialization of β -Ga₂O₃ devices, β -Ga₂O₃ (100) orientation has attracted wide interest based on its facile wafer processing and scaling-up. However, the inherent pseudo-symmetry of (100) plane renders it highly susceptible to planar defects, such as stacking faults and twins [1-2], which degrade the surface morphology of epitaxial layers and induce premature device breakdown [3]. For instance, (100) stacking faults could propagate through the entire film, yielding a surface covered by hillocks [4]. Nevertheless, the specific mechanism of stacking fault propagation and the influence of $[00\bar{1}]$ -offcut on stacking faults in (100) epilayer remain undetermined [5].

To address these concerns, we systematically investigated the formation, evolution and electrical impact of stacking faults and related defects in (100) β -Ga₂O₃ homoepitaxial layers grown by halide vapor phase epitaxy (HVPE). We revealed that the commonly observed stacking fault SF_{100-B} originates from a consecutive twinning process, and subsequently undergoes an edge-dependent upward transformation into out-of-phase boundaries (OPBs) during epitaxial growth. The formation of OPBs directly triggers the nucleation of pyramidal hillocks on the epitaxial surface and act as a killer defect, significantly increasing off-state leakage current of Schottky barrier diodes. Moreover, we proposed that the formation of SF_{100-B} is governed by the balance between two key parameters: the adatom diffusion length (λ) and the width of terrace (ω). Based on this principle, two corresponding effective strategies, employing lower VI/III ratios or larger offcut angle (up to 6°), were developed to achieve hillock-free (100) β -Ga₂O₃ epitaxy. The insights gained from this work provide a fundamental understanding of defect evolution and offer practical guidance for defect-engineering surface control, thereby paving the way toward high-performance β -Ga₂O₃-based power devices.

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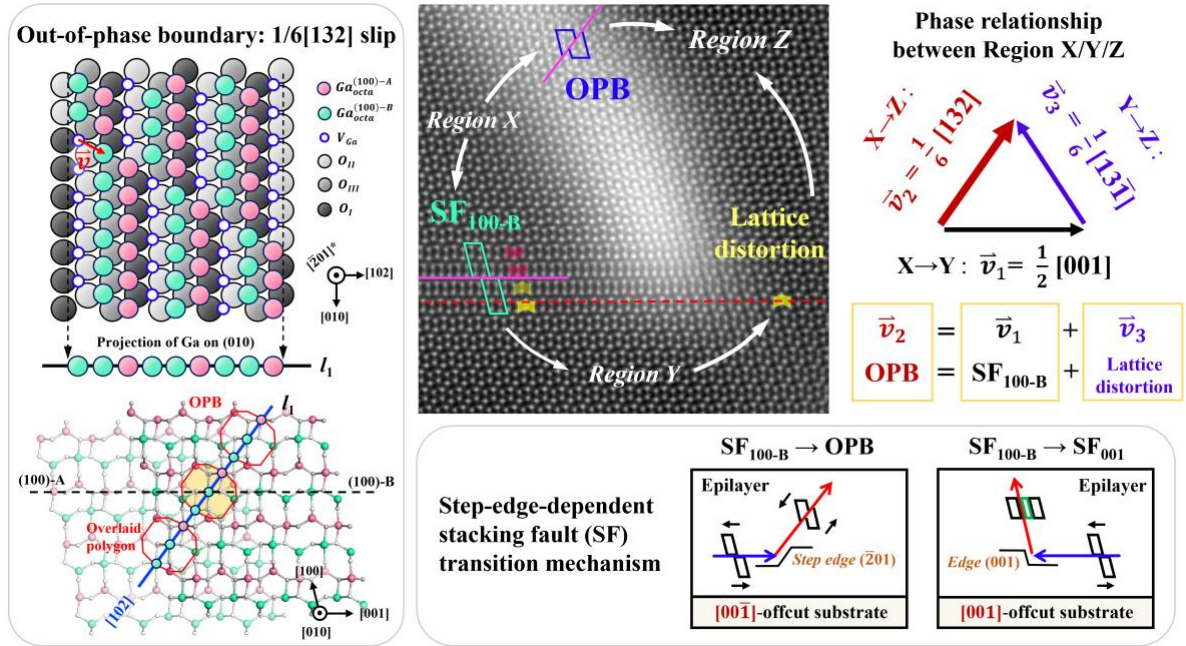


Fig. 1. An overview of stacking fault transformation in the (100) β -Ga₂O₃ epitaxial layer. Center: STEM image highlighting the slip of unit cell at out-of-phase boundary (OPB) and stacking fault SF_{100-B}. Left panel: possible lattice structure at OPB observed in STEM, viewed along $[\bar{2}01]^*$ and $[010]$ zone axis. Right panel: displacement vector analysis of Region X, Y, and Z marked in the STEM image. Bottom: schematic illustrating the distinct transformation behaviors of SF_{100-B} under $[00\bar{1}]$ - and $[001]$ -offcut conditions when encountering step edge facet.

Atomic-Scale Microscopy Insights into Order and Disorder Phenomena in $\text{Al}_x\text{Ga}_{1-x}\text{N}$

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Order and disorder in III-V compound semiconductors critically determine their electronic, optical, magnetic, thermal, and mechanical properties, directly impacting device performance and reliability. In these materials, disorder manifests through elemental distribution in ternary and quaternary alloys, substitutional arrangements on sublattices, solute impurity distribution, point and extended defects, and compositional variations across heterostructure interfaces. These phenomena affect band-gap engineering, carrier mobility and recombination rates, emission wavelengths in lasers and LEDs, absorption spectra in photodetectors and solar cells, thermal management, and emerging spintronic functionalities. While reciprocal-space techniques like X-ray diffraction have provided valuable ensemble-averaged information for decades, understanding local atomic arrangements and nanoscale compositional fluctuations in III-V semiconductors requires direct-space imaging with atomic resolution. This presentation examines three decades of research applying atomic-scale microscopy techniques, namely atom-probe tomography (APT) and scanning transmission electron microscopy (STEM), to III-V materials, and in particular $\text{Al}_x\text{Ga}_{1-x}\text{N}$ [1]. APT enables three-dimensional compositional mapping of alloys with near-atomic resolution, quantifying chemical species distribution and interfacial abruptness in heterostructures. Aberration-corrected STEM offers versatile imaging and spectroscopy for characterizing crystal structure, interface quality, and defect configurations [2,3]. We comprehensively review the application of these techniques to key phenomena in $\text{Al}_x\text{Ga}_{1-x}\text{N}$: spontaneous atomic ordering, compositional fluctuations (fig. 1), phase separation, short-range and long-range order quantification, interface roughness, and the interplay between cellular disorder (chemical distribution) and structural disorder (dislocations, stacking faults, inversion domains) (fig. 2). Analytical and statistical methods specific to each technique are discussed, along with correlative approaches connecting microscopy with functional properties. This work establishes a methodological reference framework for III-V semiconductor researchers, synthesizing achievements and identifying future opportunities.

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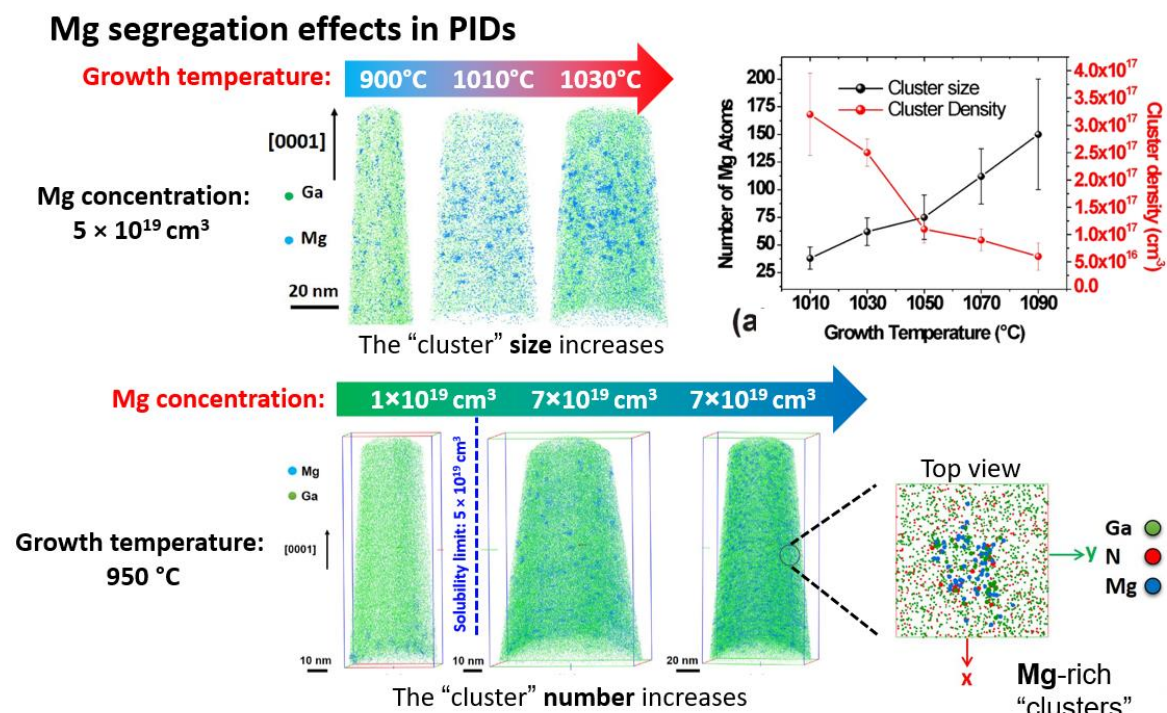


Fig. 1. Atom probe tomography (APT) reconstructions of Mg-doped GaN (GaN:Mg) showing Mg segregation within pyramidal inversion domains (PIDs): samples grown at increasing temperatures, samples with increasing Mg concentration.

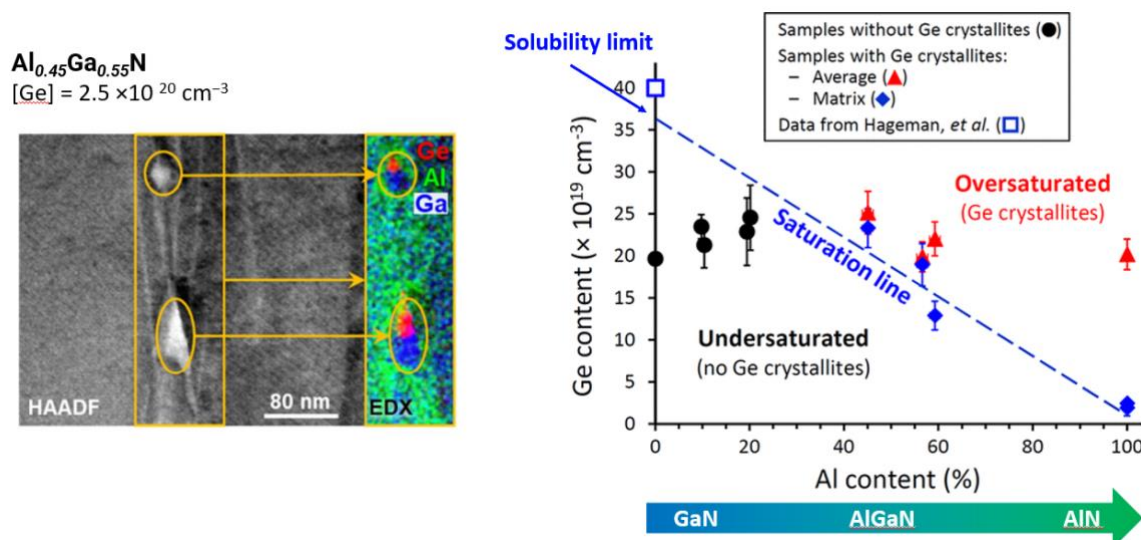


Fig. 2. Ge solubility in $\text{Al}_x\text{Ga}_{1-x}\text{N}$. Limited incorporation results in diffusion along structural defects, Ge precipitate formation, and surface crystallites. Ge incorporation is significantly lower in AlN than in GaN and increases with Ga mole fraction, consistent with substitution on Ga sites, with a maximum occupancy of ~1% of Ga sites.

Deep Level Defects in β -Ga₂O₃: Insights from Hydrogenation and Oxygen Annealing Studies

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The origin of n-type conductivity in β -Ga₂O₃ remains a subject of ongoing debate. In this study, we investigate the role of hydrogen and intrinsic defects in Czochralski-grown β -Ga₂O₃ single crystals using capacitance-voltage (CV) measurements, deep-level transient spectroscopy (DLTS), and high-resolution Laplace DLTS. We demonstrate that annealing in hydrogen atmosphere at 1200 °C significantly increases the free carrier concentration, whereas oxygen annealing under identical conditions reduces it. FTIR measurements performed by K. Irmscher (private communication) confirm the presence of OH-related species (3437.5 cm⁻¹) in as-grown and hydrogenated samples. These species disappear after oxygen treatment, supporting the hypothesis that interstitial or substitutional hydrogen acts as a shallow donor in β -Ga₂O₃.

Using Laplace DLTS, we resolve the dominant E360 peak into multiple components (E390, E370, and E355) with activation enthalpies ranging from 640 to 1020 meV. The enhancement of emission rates as a function of electric field is investigated using the Poole-Frenkel model and the phonon-assisted tunneling model. Depth profiling reveals that the E370 concentration decreases after oxygen annealing and increases after hydrogenation, while a new defect E355 emerges near the surface in hydrogen-treated samples.

Based on these correlations, we discuss the origin of the observed defects with an emphasis on oxygen-vacancy-related and hydrogen-related complexes. Furthermore, we address the influence of these deep-level defects on the free carrier concentration and their role in determining the n-type conductivity in β -Ga₂O₃.

Magnetron-Sputtered HfO₂ Thin Films for Microelectronic and Sensor Applications

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HfO₂ layers and HfO₂/SiO₂ stack structures deposited on silicon are essential components in modern microelectronics, with applications ranging from gate dielectrics and memory devices to advanced sensor technologies. Optimizing the performance of HfO₂-based layers requires an understanding of how deposition parameters influence their structural, electrical, and optical properties.

In this work, we systematically investigate HfO₂ layers of varying thickness deposited on Si wafers by magnetron sputtering under different process conditions. Structural analysis reveals that partial crystallization of HfO₂ can occur already during deposition, depending on film thickness and sputtering pressure. The mechanical stress in the deposited layers is quantified and correlated with the deposition parameters.

The electrical characterization focuses on the density of interface states and positive fixed charges at the HfO₂/Si interface, and the origin of these defects is discussed in relation to the sputtering conditions. Macroscopic defects formed during deposition are characterized using scanning electron microscopy. Complementary ellipsometry measurements allow extraction of the optical band gap of the HfO₂ layers and reveal its dependence on sputtering pressure.

Our results provide a comprehensive understanding of how magnetron sputtering conditions affect the properties of HfO₂ films and offer practical guidelines for optimizing HfO₂ layers for electronic and sensor applications.

Defect Engineering and Passivation at Halide Perovskite and Kesterite Nanoparticles Interface: A Combined Experimental and DFT Study

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The long-term stability and reliability of advanced optoelectronic devices, such as perovskite solar cells (PSCs), depend heavily on structurally robust charge-transport layers. Kesterite ($\text{Cu}_2\text{ZnSnS}_4$, or CZTS) nanoparticles offer a stable, earth-abundant, and non-toxic inorganic alternative to conventional organic hole-transport materials [1]. This study investigates the defect engineering and structural optimization of CZTS nanoparticles by coupling experimental processing with Density Functional Theory (DFT) to elucidate the interface physics. Comprehensive structural and morphological characterizations (XRD, Raman, EDX-SEM, and TEM) confirmed phase purity.

DFT calculations were carried out to model the interface between CZTS and the perovskite absorber (MAPI). Two interface configurations were examined, differing in the lattice parameters adopted to construct the junction. In the first case, the perovskite lattice constants were imposed, thereby shrinking the CZTS layer to emulate the experimental n-i-p architecture, where CZTS is deposited onto MAPI. In the second configuration, the lattice parameters of CZTS were retained, mimicking the p-i-n layout. Structural relaxation shows that constraining CZTS to the perovskite lattice induces substantial interfacial reconstruction and marked distortion. Conversely, preserving the CZTS lattice results in a more relaxed interface with limited structural deformation, indicating that the p-i-n configuration is structurally more favorable. Two CZTS surface terminations were further analyzed, namely S- and Cu-terminated interfaces. Binding energy calculations reveal stronger adhesion for the S-terminated surface, as reflected by its more negative interaction energy. Nevertheless, density of states (DOS) analysis indicates that only the Cu-terminated interface ensures a suitable band alignment for hole extraction, with the valence band maximum of CZTS positioned at higher energy relative to that of MAPI.

Overall, these findings provide a solid atomistic foundation for further investigations into the defect chemistry of inorganic transport layers and offer valuable guidance for the design of highly durable semiconductor interfaces.

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Defect studies and down conversion strategies of double-cation mixed perovskite solar cells

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Recently, perovskites have become one of the most promising materials for solar cells, thanks to ease of production and increasing efficiency. Since their first use by Kojima in 2009[1], perovskite solar cells have increased their photovoltaic efficiency, exceeding 25 % and approaching the performance of silicon, the benchmark material for the sector, which nevertheless presents criticalities, primarily regarding its sustainability. One of the limits hindering the scalability of perovskites solar cells is their instability, which is linked to structural defects. In this context, the analysis of defective activity is crucial to understanding degradation mechanisms and to guiding material engineering.

In this study, we investigated a double-cation mixed-halide $CsFAPb(IBr)_3$ perovskite solar cell to establish dominant defects and to improve its photovoltaic efficiency through down-conversion strategies. This complex composition ensures superior stability [2][3][4] but may introduce additional disorder, making defect characterization essential. For the first purpose, the technique employed was the Photo-Induced Current Transient Spectroscopy (PICTS) [5][6], which allows the identification of the defect activation energy. The analysis highlighted a single dominant trap attributed to interstitial halides (iodine or bromine), which showed activation energy about 0.4 eV. Measurements were conducted after several days and under bias to assess stability and the potential evolution of defects. To further improve device robustness, we introduced a Cytop capping layer— a highly fluorinated and solvent-orthogonal material— to mitigate interaction with atmosphere.

To improve photoconversion efficiency, the cell was coupled with a layer of PDMS doped with Europium complexes capable of absorbing UV radiation and converting it into red light, reducing the spectral mismatch between the light absorption of the perovskite and the solar radiation.

In conclusion, we identified the most dominant defect in double-cation mixed perovskite solar cells and improved the solar cell efficiency through the addition of a downshifting layer.

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Defect Suppression in Boron-Doped MW-PECVD-Grown (113)-Oriented Diamond Substrates for Vertical Power Schottky Diodes

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Boron doped diamond (BDD) grown under (113) orientation offers excellent trade-off between the surface morphology, epilayer roughness and electrical properties compared to conventional (100) oriented BDD layers including up to twice growth rate and 4-5 times higher boron incorporation efficiency [1]. Realization of power diamond devices, like vertical Schottky barrier diodes (VSBDs), necessitates fabrication of thick, heavily boron doped (concentration $>10^{20} \text{ cm}^{-3}$) monocrystalline substrates with low resistivity. In this contribution, we report on the development of high-quality (113)-oriented BDD substrates and layers whose properties have been verified through implementation in VSBDs.

Thick epitaxial BDD layers were grown in a AX5010 (Seki Diamond Systems) MW PECVD system on (113) oriented insulating diamond substrates produced from HPHT grown Ib synthetic crystals [2]. The layers were characterized by SEM, AFM, SIMS, Raman spectroscopy, Hall measurement, etc. The addition of nitrogen in the gas phase during the growth at high microwave power densities was optimized to reduce crystal defects and cracks (see Fig.1). After successful growth (see the growth condition in Tab.1), samples were polished into a round shape and the non-conducting HPHT substrate was removed by scaife polishing. The VSBDs were implemented analogously to the previously realized pseudo-vertical SBDs [3]. The polished side of the heavily BDD (113) oriented substrate ($N_A \sim 5 \times 10^{20} \text{ cm}^{-3}$) with a diameter of about 3 mm and thickness of 320 μm (see Fig.2) was first covered by BDD buffer layer and then 0.6 μm thick lightly boron doped drift region, oxygen terminated, and covered by evaporated Mo/Au Schottky contacts. The bottom ohmic contact was formed by Ti/Au bi-layer. I-V and C-V characteristics of the realized vSBDs were measured at temperatures ranging from 25 to 150 °C (see Fig.3).

Results show that an appropriate selection of nitrogen addition and growth conditions allows for the growth of smooth and crack-free free-standing (113)-oriented BDD layers with low resistivity. The VSBDs were realized on these substrates with a good yield, they exhibited low leakage ($J_R < 10^{-8} \text{ A/cm}^2 @ \text{RT}$) and high and temperature stable ON/OFF current ratio ($\sim 1e7$) regarding to the realized structure. Precise control of the drift region doping and avoiding donor contamination causing doping compensation is then necessary for receiving optimal I-V characteristics.

This work was supported by CSF project 20-11140S, TSRI-CTU JRS 09 and MEYS project No. SOLID21-CZ.02.1.01/0.0/0.0/16_019/ 0000760.

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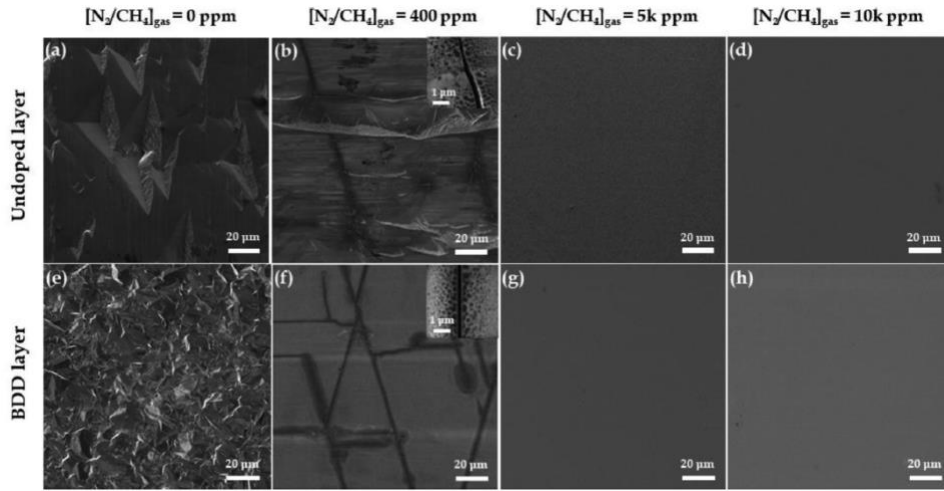


Fig. 1. SEM images of undoped diamond and BDD (113) epitaxial layers grown at different with different N_2/CH_4 ratio [2].

Table 1. MPCVD Growth Parameters

Layer	Pressure (mbar)	Microwave power (W)	Total gas flow (Sccm)	$[CH_4]$ (%)	B/C (ppm)	Deposition time (h)
P^{++} substrate	90	1300	500	2	400	100
P^- drift region	100	580	700	0.1	0	1.5

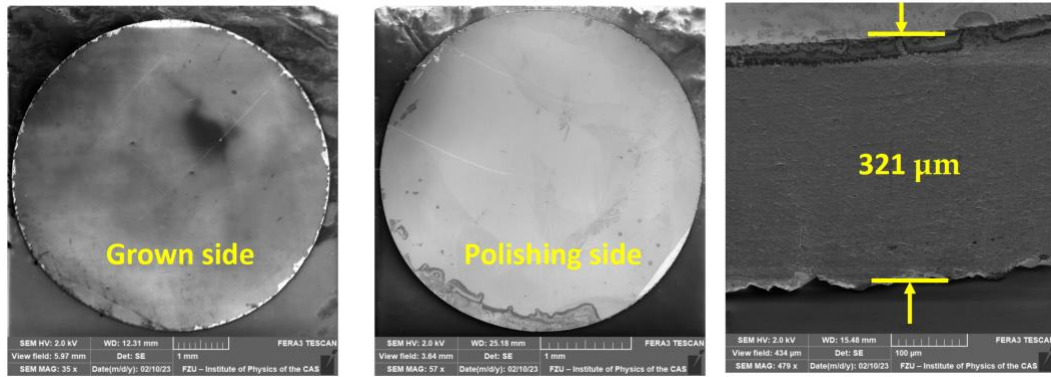


Fig. 2. SEM images of BDD (113) free-standing epitaxial layers: as grown top side (left), polished back side (center), and the cross-sectional view (right).

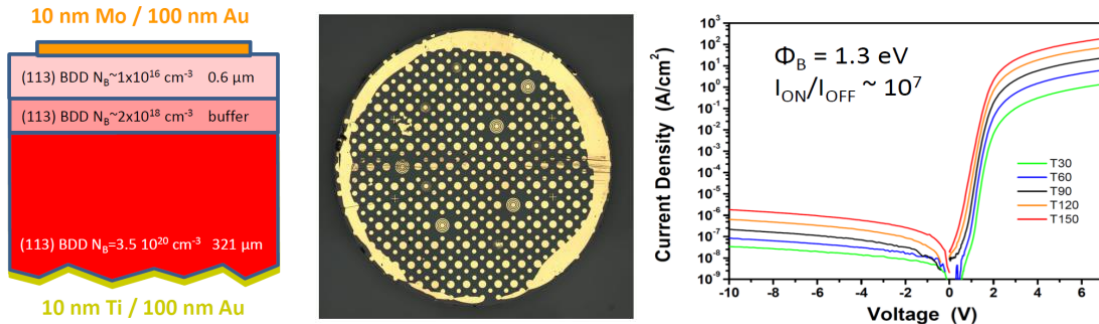


Fig. 3. The schematic cross section (left), top view on the realized chip (center), and I-V characteristics (right) of the vertical SBDs produced on the (113) oriented BDD.

Detection of nuclei for oxidation induced stacking faults

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Oxidation induced stacking faults (OISFs) act as strong recombination centers in silicon wafers degrading the performance of integrated devices. Using conventional detection methods, these defects become visible only after thermal processing; therefore, traditional inspection relies on defect etching to reveal them once they have grown during a controlled thermal oxidation step. Since this method is destructive, the wafer becomes unusable even if it is defect free. Consequently, it would be highly beneficial to have a method that does not need any thermal treatment and would be completely nondestructive.

Here we have studied if photoluminescence imaging (PLI) [1] could be utilized for early detection of OISF nuclei. The silicon wafers studied were 200 mm boron-doped with resistivity of 8 Ωcm and oxygen concentration of $6 \times 10^{17} \text{ cm}^{-3}$ and they were grown with parameters that are known to promote OISF formation. The wafers experienced a short dip in diluted HF prior to the measurement in order to passivate the dangling bonds at the surface and to increase the PL signal [2]. As reference measurements we used microwave photoconductance decay, X-ray diffraction imaging, and defect etching followed by optical microscopy and microdefect inspection tool.

First, we measured a wafer that had not undergone any annealing after the crystal growth. As expected, none of the reference measurements revealed any detectable defects on the wafer. However, PLI shows a clear ringlike pattern in such a wafer (Fig. 1a). Then the same wafer experienced a wet oxidation at 1100 °C and was remeasured. Now the same ring appears more strongly in the PL image (Fig. 1b), indicating that the initial ring likely corresponds to OISF nuclei. The same image shows that after oxidation, multiple rings become visible, with the outermost bright ring attributed to the so-called perfect silicon region [3]. The inner rings arise from varying densities of bulk micro defects (BMDs, oxygen precipitates) and an OISF ring, reflecting radial variations in oxygen content and intrinsic point defect distributions. Wright etching (Fig. 1c) reveals only stacking faults, so transmission electron microscopy would be required to confirm the nature of the additional rings seen in PLI. Finally, we also examined the correlation between the PL signal and BMD density using light scattering tomography.

To conclude, PLI allows fast, high resolution, full-wafer imaging of OISF nuclei without destructive sample preparation, i.e., no oxidation or any processing needed after crystal growth (excluding HF dip). This result allows wafer manufacturers to identify the wafers that are prone to OISF formation prior to device manufacturing.

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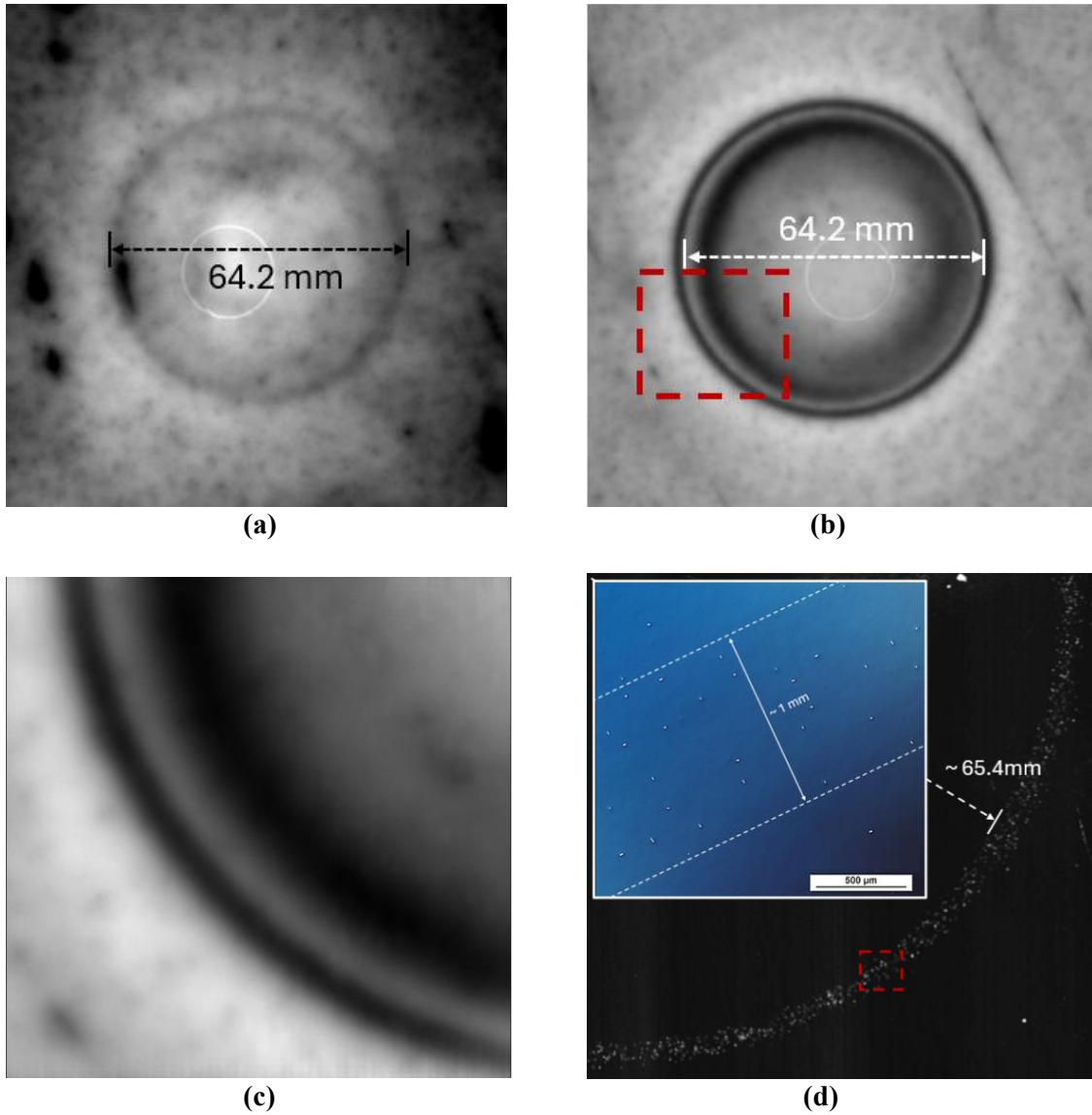


Fig. 1. PLI images: (a) immediately after crystal growth (no annealing); (b) and (c) after wet oxidation. The red square in (b) indicates the approximate area shown at higher magnification in (c). The white circle visible in the center of the PLI images in (a) and (b) is a measurement artefact caused by reflection from the coil on the measurement stage.

(d) Micro-defect inspection image of the same wafer after oxidation and Wright etching. The red square marks the approximate location of the optical microscope image shown in the inset. The width of the OISF ring varies from 1 mm to 2.3 mm. The stacking fault density measured on top of the OISF ring is $1.3 \times 10^2 \text{ cm}^{-2}$.

Elaboration of 200 mm GeSnOI via Bonded Etch-Back SOI process

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GeSn alloys are promising for mid-infrared optoelectronics, as Sn contents exceeding 8% combined with tensile strain induce a direct bandgap transition [1]. However, a step-graded Sn approach on a virtual Ge buffer [2] is required to reach high Sn contents and mitigate Sn segregation during growth. These graded layers, located immediately below the active layer, contain misfit dislocations that degrade optical confinement and device performance.

In this work, we present the first CMOS-compatible fabrication of 200 mm GeSnOI wafers with 14–16% of Sn [3], achieved via a bonded etch-back silicon-on-insulator (SOI) process. This approach removes the defective part of the graded Sn layers, yielding high-quality, nearly dislocation-free GeSn layers directly on insulator.

We also compare GeSn growth using germane (GeH₄) and digermane (Ge₂H₆) precursors, highlighting their impact on relaxation, composition and optical emission. As-grown and transferred GeSn layers are characterized using x-ray diffraction (XRD), Raman spectroscopy, photoluminescence (PL), atomic force microscopy (AFM), and transmission electron microscopy (TEM). Figure 1 shows the entire 200 mm GeSnOI wafer post transfer, while the TEM images confirm the high crystallinity of the transferred layers, demonstrating their potential for scalable, high-performance mid-infrared devices.

This work demonstrates the monolithic integration of GeSn-based photonic and electronic components onto 200 mm platforms.

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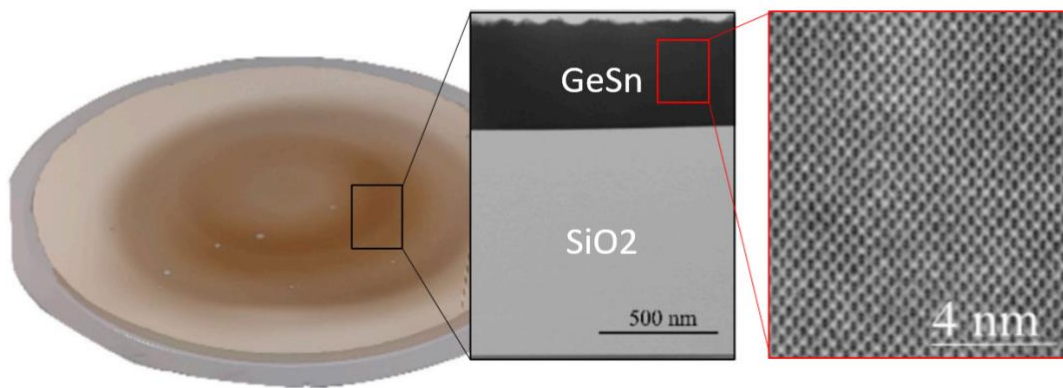


Fig. 1. Cross-sectional STEM and TEM images of a 200 mm GeSnOI wafer post transfer.

Acknowledgment: This work was supported by the European Union's Horizon 2020 LASTSTEP Project under grant agreement ID: 101070208, the IPCEI Microelectronics and Connectivity project. It was also supported by the French Public Authorities within the frame of France 2030.

Estimating recombination-active defect concentrations in silicon n^+p-p^+ structures via transfer learning from computer vision models

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This study proposes a machine learning framework for quantifying defect concentrations under limited data conditions [1]. Despite the widespread adoption of artificial intelligence in physics, its application to point defect characterization remains limited [2]. Reliable predictive modeling requires large labeled datasets. Simulations partially alleviate this need but may not fully represent physical systems, while exhaustive experiments remain impractical, particularly for semiconductor defect analysis. Transfer learning mitigates this constraint by adapting pretrained models to the target task.

This work investigates the use of pretrained computer vision (CV) models, originally optimized on large-scale datasets, for defect characterization. The approach converts electrophysical measurements governed by defect profiles into image representations compatible with vision architectures, enabling feature extraction and downstream defect analysis. Although CV methods are established for defect detection, existing applications primarily target macroscale defects via electroluminescence imaging [3].

The method was validated by quantifying iron in silicon n^+p-p^+ structures from short-circuit current kinetics measured after FeB dissociation. The training dataset comprised 25 synthetic curves computed for different iron concentrations or 20 experimental curves from samples with varying Fe content. After Savitzky-Golay smoothing, a continuous Morlet wavelet transform mapped the one-dimensional time series to two-dimensional spectrograms, where concentration-dependent variations in kinetic curves produced distinct features (see Fig.1). Feature extraction employed six pretrained CV architectures, yielding 1,000-433,640 features. These vectors were used to train regression models, including RF, SVR, GB, XGB, and DNN, on the aforementioned small datasets.

Fig.2 shows model performance on synthetic and experimental datasets. The most accurate predictions – mean percentage error below 6% for synthetic and 9% for experimental data – were obtained using EfficientNetB7 or NASNetLarge for wavelet images, combined with DNN or SVR. For experimental data, using class probabilities as features was most effective, while direct image features performed best for synthetic datasets.

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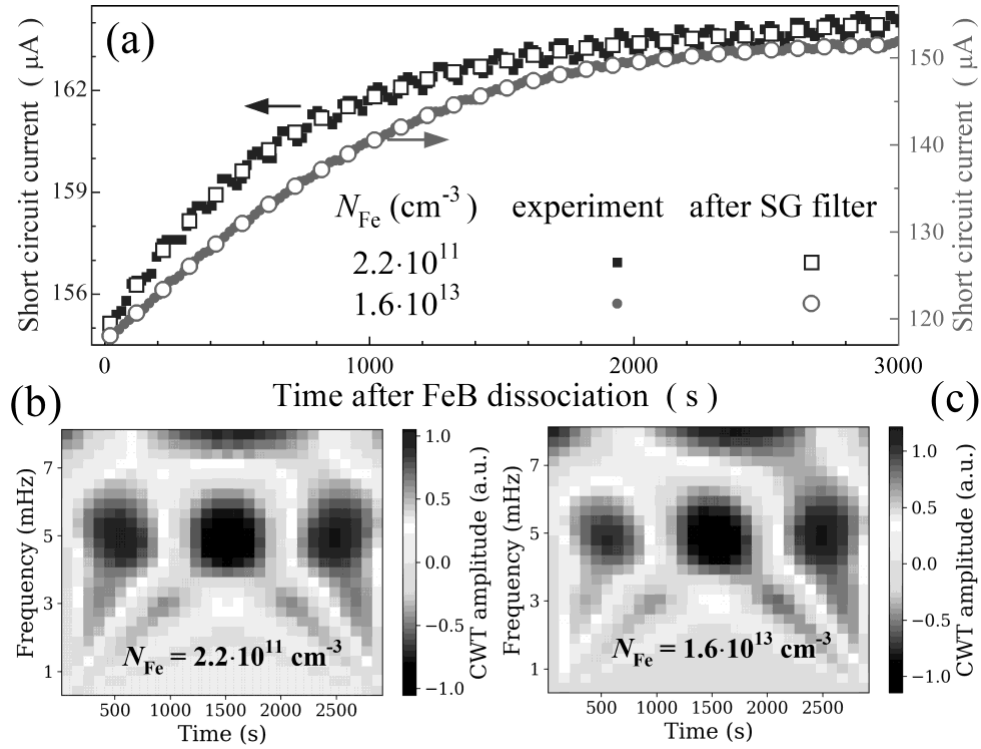


Fig. 1. (a) Short-circuit current kinetics for samples with iron concentration $2.2 \cdot 10^{11} \text{ cm}^{-3}$ (filled squares) and $1.6 \cdot 10^{13} \text{ cm}^{-3}$ (filled circles), with Savitzky–Golay–filtered curves (open symbols). (b, c) Representative wavelet spectrograms from the filtered data. Although the CV models analyzed full-color images, these are shown here in the format compliant with the abstract submission guidelines.

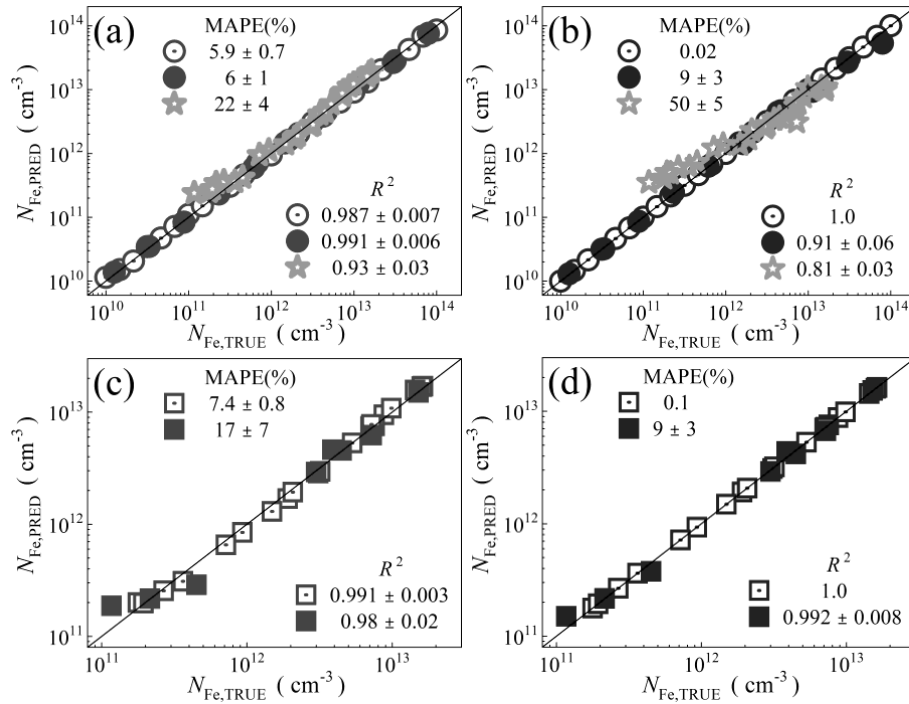


Fig. 2. Comparison of model predictions with ground truth. Models were trained on synthetic (a,b) or experimental (c,d) datasets using EfficientNetB7 with Deep Neural Network (a,c) and NASNetLarge with Support Vector Regression (b,d). Symbols indicate synthetic training (open circles) and testing (filled circles), experimental training (open squares) and testing (filled squares), and stars denote synthetic-trained models applied to experimental data. Mean absolute percentage error (MAPE) and coefficient of determination (R^2) are reported for each case.

Identification of the dominant trap states in mixed halide perovskite pellets

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Metal halide perovskites exhibit exceptional optoelectronic properties, in which defects play a central role in determining both device performance and long-term stability. In this work, the aim is to systematically improve the fundamental knowledge on defect states and its functional implications across lead-based perovskite pellets with varying chemical compositions, including MAPbI₃, MACsPbI₃, and mixed-halide formulations incorporating Br and Cl. Thick perovskite pellets integrated into polymer matrices are fabricated using a solvent-free mechanochemical synthesis followed by hot pressing, producing resilient and readily scalable architectures. The tailored chemical composition of the pellets enables a detailed investigation of dominant defect contributions, with interface-influenced ionic migration identified as the primary transport mechanism. Photo-Induced Current Transient Spectroscopy (PICTS) analysis, combined with temperature-dependent current–voltage measurements from 270 to 380 K, allow us to obtain the “finger prints” of the predominant traps. Quantitative extraction of defect activation energies and emission rates highlights the critical role of A-site cations (Cs⁺ and MA⁺) and halide composition in modulating ionic mobility and defect accumulation at charge-collecting interfaces. In addition to surface- and interface-sensitive analysis by interdigitated electrode configuration, top-bottom electrode architectures based on MAPbI₃ pellets provide insight into intrinsic bulk defect pathways and long-range ion transport as an X-Ray detector. The defect characteristics directly impact performance of device in terms of charge collection efficiency and stability. Overall, this study establishes clear correlations between elemental composition and ionic defect behavior, providing fundamental design guidelines for the development of next-generation perovskite-based X-ray detectors with improved stability and scalability.

Impact of Ionic Defects on Mesoporous Perovskite Solar Cells and X-Ray Detectors

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Mesoporous TiO₂/ZrO₂/Carbon stacks infiltrated with perovskite offer a cost-effective, sustainable architecture for both photovoltaic [1] and X-ray detector applications [2]. However, the migration of mobile ionic defects, ubiquitous in perovskites, remains a critical technological problem, causing hysteretic responses and performance losses. Addressing this challenge requires a synergistic approach, combining in-operando measurements with advanced transient optoelectrical simulations to understand the complex interplay between ionic and electronic charges. We present results [2-4] on mesoporous devices integrating inorganic CsPbI₃ or hybrid MAPbI₃ perovskites. Performance was evaluated for both solar energy harvesting (illuminating from the TiO₂ side) and X-ray detection (from the Carbon side). Transient optoelectrical simulations reveal that mobile ions govern device operation by accumulating at interfaces, modulating band bending and hindering charge extraction. Under certain conditions, mobile cations (such as I⁻ vacancies or MA⁺/Cs⁺ interstitials) enhance electrostatic screening near the electron transport layer, giving rise to a peculiar “bump” in the measured current-voltage characteristics, whose origin was debated in literature. Notably, CsPbI₃ exhibited suppressed cation mobility compared to MAPbI₃, resulting in minimal hysteresis and more stable steady-state photoconversion efficiency. In X-ray detection mode, the architecture demonstrated stable, self-powered operation up to 50 keV and fast response, sustaining a cumulative dose of 18.643 Gy at the high dose rate of 310 mGy_{air}/s without significant degradation. Analysis of the response signals allowed us to discern a fast response (ms) and slower (seconds) transient signals, assigning them to electronic trapping/detrapping and ionic transport, respectively. Overall, these insights into the ion-electron interplay are vital for the up-scaling and stabilization of perovskite-based optoelectronic devices.

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[3] *Solar RRL* **2024**, 2300944

[4] *ACS Appl. Energy Mater.* **2024**, 7, 12069

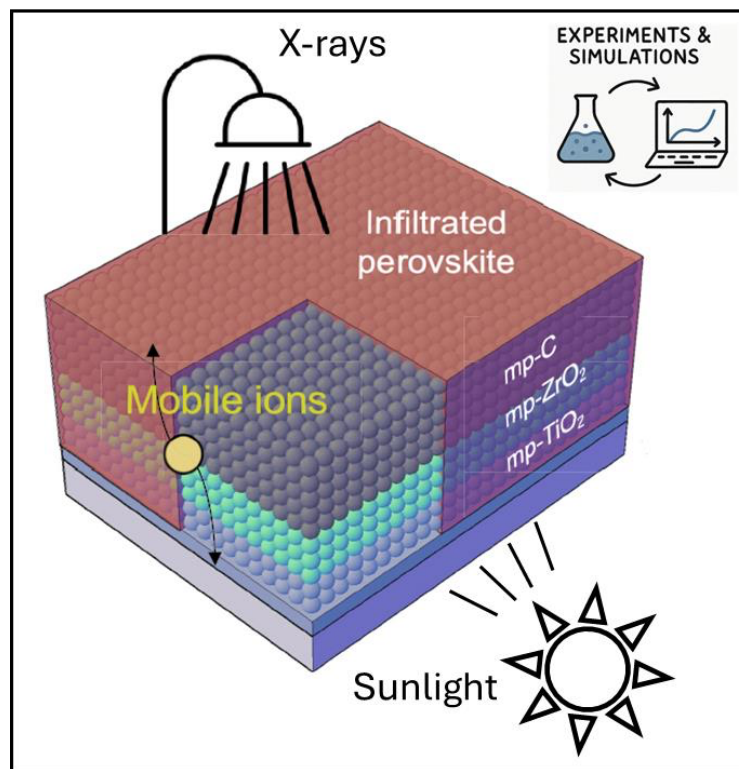


Fig. 1. Experiments and simulations unravel the impact of mobile ions on the performance of perovskite-based mesoporous devices operating as solar cells or X-ray detectors.

Lithium-free segmentable hyperpure germanium detector via Pulsed Laser Melting

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High-purity germanium (HPGe) γ -ray detectors require thin segmentable n+ contacts that remain stable during annealing for radiation-damage recovery [1,2]. Li-diffused contacts introduce dead layers of millimetric scale, limit segmentation, and are unstable during typical recovery treatments (~ 378 K for tens of hours). We present a lithium-free junction technology based on a Sb precursor deposited by magnetron sputtering followed by pulsed laser melting (PLM) diffusion treatment. PLM melts only a shallow Ge surface layer and incorporates dopants during rapid epitaxial regrowth, yielding an abrupt, ultra-thin n+ junction, while preserving the hyperpure bulk and enabling photolithographic segmentation.

We fabricated a 35×35 mm², 1.6 mm-thick planar detector with six strips plus a guard ring. ²⁴¹Am and ¹³³Ba spectroscopy showed standard-like photopeak resolution on multiple segments, while ⁶⁰Co transient signals demonstrated position sensitivity suitable for pulse-shape analysis. The segmented PLM junction remained stable after an annealing cycle representative of neutron-damage recovery [3].

Finally, the process was then scaled to 1-2 cm-thick crystals, refining contamination control, cleaning, gold-free photolithography, and mechanical chemical polishing. Reducing contact-induced stress and adding a thick Al layer raised the breakdown voltage above the depletion voltage, enabling thick, segmented, lithium-free HPGe detectors [1,2,3].

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[3] S. Bertoldo et al. *Mat. Sci. Semiconductor Processing*, **2025**, 200, 109967.

Monolithic GeSn Photodetectors Integrated on Silicon for Mid-Infrared Applications

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Efficient room-temperature mid-infrared photodetection is essential for numerous applications, such as environmental sensing, biomedical analysis or security technologies. Germanium–tin (GeSn) alloys are increasingly recognized as promising materials for lowering manufacturing costs and enabling large-scale integration, since they can be epitaxially grown on 200 and 300 mm Ge-buffered silicon wafers [1]. Their attractiveness comes from their full compatibility with CMOS processes and from the possibility of engineering the bandgap and make it direct by adjusting the Sn composition and the built-in strain.

Within the framework of the Horizon Europe LASTSTEP project, we evaluated various Sn contents, high-performance GeSn photodiodes monolithically fabricated on 200 mm silicon substrates (Fig. 1). For example, Ge_{0.846}Sn_{0.154} devices operated in photovoltaic regime and exhibited a room-temperature cut-off wavelength of 3.5 μm . At 3.3 μm , a maximum specific detectivity (D^*) of $3.8 \times 10^7 \text{ cm} \cdot \text{Hz}^{1/2} \cdot \text{W}^{-1}$ was measured, placing these results among the best reported for GeSn photodiodes in this wavelength range. Photodiodes were further validated through methane sensing experiments in a dedicated gas cell, demonstrating practical mid-wave infrared gas detection. In addition, we explored an alternative integration approach based on transferring GeSn heterostructures onto metallic back reflectors, while maintaining their structural and optoelectronic integrity. Such an architecture improved optical confinement and enhanced photon absorption without introducing additional crystalline defects. At 2.5 μm and 300 K, this strategy resulted in a threefold responsivity increase, with $D^* = 6.5 \times 10^8 \text{ cm} \cdot \text{Hz}^{1/2} \cdot \text{W}^{-1}$, a value which exceeds the typical performance reported for comparable Sn concentrations.

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Acknowledgment: This work was supported by the European Union's Horizon 2020 LASTSTEP Project under grant agreement ID: 101070208, the IPCEI Microelectronics and Connectivity project. It was also supported by the French Public Authorities within the frame of France 2030.

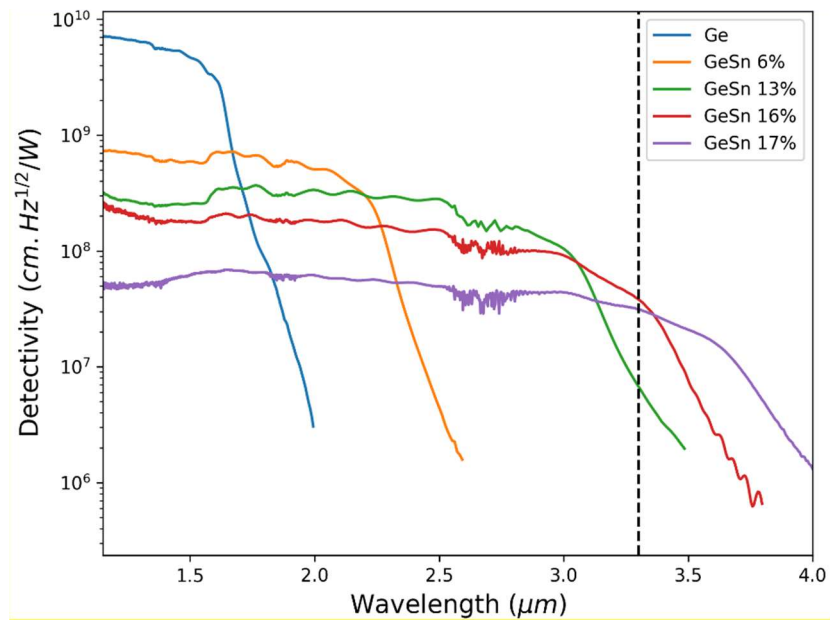


Fig. 1. Specific detectivity of LASTSTEP's GeSn photodetectors as a function of Sn content

Multiparametric Control of MAPbI₃ Growth via Low-Vacuum Proximity-Space Effusion

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Hybrid and inorganic halide perovskites have emerged as leading candidates for third-generation optoelectronics, particularly photovoltaics. In just over a decade, perovskite solar-cell efficiencies have exceeded 27%, while retaining the prospect of low-cost manufacturing and lightweight, flexible architectures. Application domains such as agrivoltaics, building-applied photovoltaics, and indoor power generation would particularly benefit from perovskite-based technologies. However, large-scale deployment is still limited by film-to-film reproducibility, long-term stability, and, crucially, manufacturing scalability. Vapour-based routes, although attractive for uniformity and solvent-free processing, typically remain low-throughput (often $\leq 10 \text{ nm min}^{-1}$)^{1,2} when high material quality is required, since faster deposition does not necessarily yield well-converted, low-defect films; conventional high-vacuum PVD further adds complexity and material losses due to long throw distances.

We address these constraints with Low-Vacuum Proximity-Space Effusion³ (LV-PSE; patent EP4284969(B1)⁴ granted on 2025-04-02), operating at $1\text{--}4 \times 10^{-2}$ mbar with source-substrate distances of a few centimetres, where chamber pressure and proximity become additional control variables. We demonstrate a two-step MAPbI₃ process based on an ordered PbI₂ template followed by MAI intercalation, achieving an overall deposition rate of 23 nm min^{-1} while preserving compositional control at each step and improving precursor utilisation (reduced waste by 30–50% versus HV-PVD). Temperature and vapour pressure regulate the adsorption-desorption balance during MAI uptake, whereas short throw distance enhances local flux and enables rate tuning via pressure modulation, providing a practical throughput-quality trade-off. Molecular-dynamics simulations using machine-learned interatomic potentials capture early PbI₂ lattice rearrangement and MAI diffusion, supporting a transient amorphisation preceding MAPbI₃ crystallisation.

Overall, the work identifies PbI₂ template order and coupled pressure-temperature control as key levers for high-rate, scalable vapour deposition of high-quality films for high-volume manufacturing of perovskite devices across a broad range of application domains.

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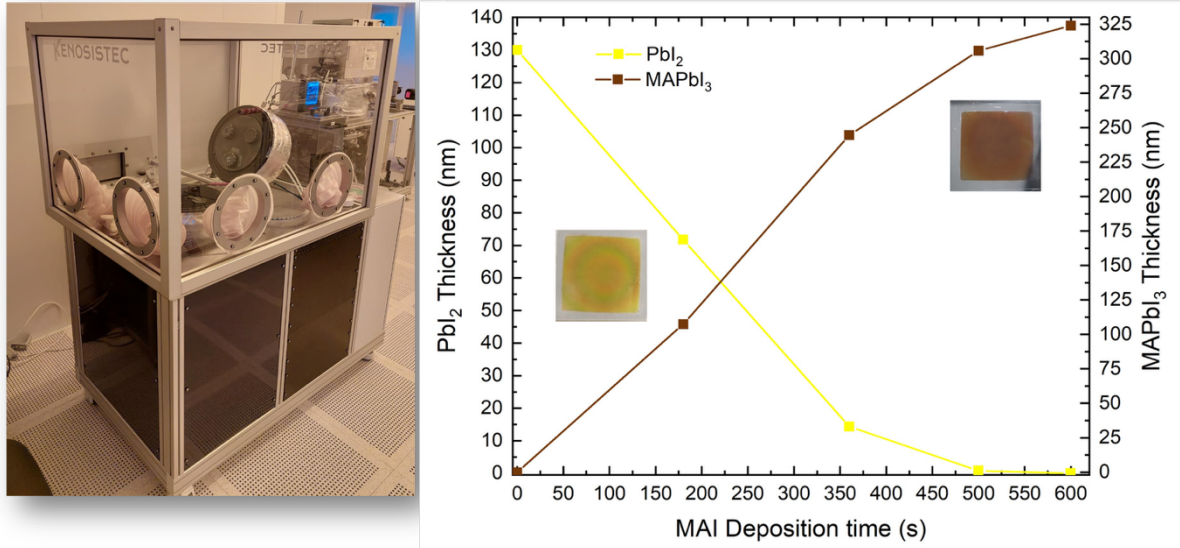


Fig. 1. LV-PSE system and PbI_2 - MAPbI_3 interplay during in-situ two-step growth

Non-destructive light scattering-based bulk micro defect detection in silicon wafers

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Light Scattering Tomography (LST) technique is widely used in wafer quality control. It detects Bulk Micro Defects (BMDs) in silicon wafers, which need to be cleaved in half for the measurement. The method applies dark field detection by separating the light detection part from the illumination. The scattered light produced by BMDs is collected via the cleaved surface, while the illumination is applied via the front surface of the sample.

This work is subject to patent protection; therefore, only high-level methodology and representative results are presented. [1]

There has always been a great interest to avoid the necessity of the cleavage of the samples. Therefore, Semilab has developed a non-destructive, light scattering-based, bulk micro defect detecting system. It is called Line Scanning Microscope (LSM). The basic idea has come from an earlier development at Semilab. [2, 3] Building on this concept, we implemented a non-destructive configuration where illumination and detection are applied from the front surface of the wafer, eliminating the need for cleaving (Fig. 1)

The system employs line-shaped illumination and dark-field detection to image scattering from bulk micro defects at a selected depth (Fig. 2). Defect maps are acquired via scanning; the depth selectivity is achieved by a proprietary optical filtering approach integrated into the detection path. [1]

To efficiently obtain depth distribution information, an XZ acquisition mode is used that enables deriving depth profiles from a single measurement (Fig. 3). This improves throughput while maintaining non-destructive operation. An example XZ image is shown in Fig. 4, indicating measurement conditions at different image positions.

LST requires perpendicular cleavage for the measurement. Si<110> samples can be cleaved this way but not as reliable as standard Si<100>, while Si<111> cannot be cleaved perpendicularly. LSM is an ultimate solution for any orientation Si materials because it does not require cleavage.

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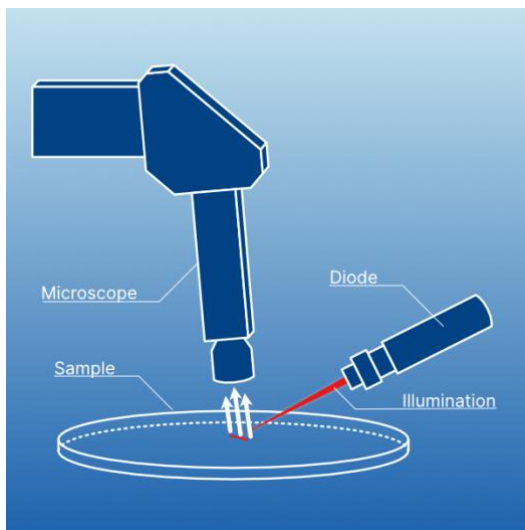


Fig. 1. Layout of illumination and detection unit of LSM.

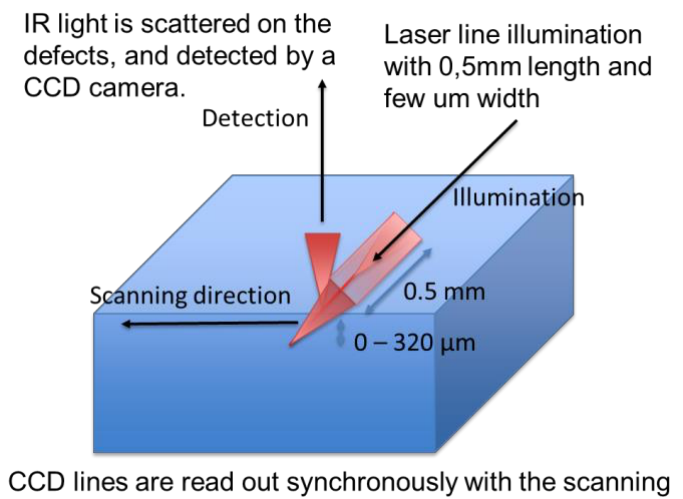


Fig. 2. Illumination line and scattered signal by a defect collected by the detection unit.

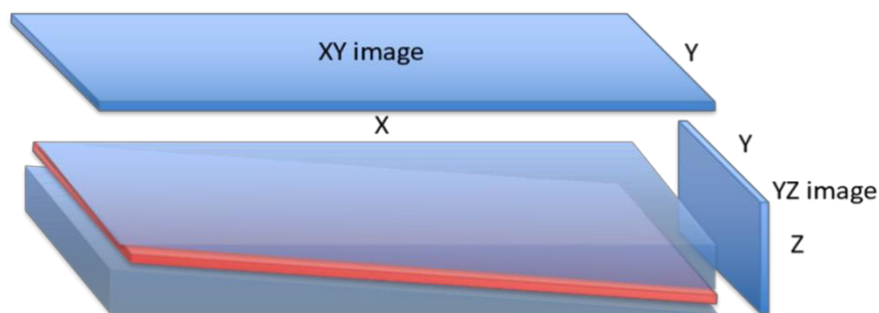


Fig. 3. XZ image orientation and its projections.

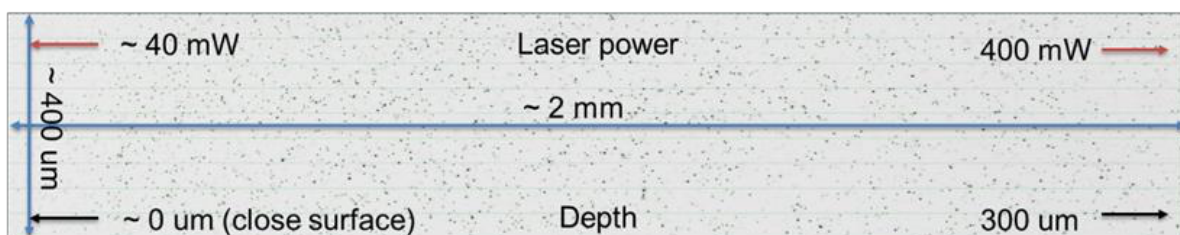


Fig. 4. An example XZ measurement.

Novel method to measure the temperature-dependent minority carrier lifetime of crystalline silicon wafers for solar cell applications

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The temperature dependence of minority carrier lifetime in crystalline silicon is a critical parameter in the characterization and optimization of photovoltaic materials and semiconductor devices. Carrier lifetime strongly influences device efficiency, recombination behavior, and overall material quality. While established techniques allow accurate lifetime measurements at room temperature, reliable characterization over a controlled temperature range remains technically challenging, particularly for bulk samples such as wafers, bricks, and ingots. Therefore, developing robust and electrically stable methods for temperature-dependent lifetime measurements is essential for both research and industrial applications.

This study presents a novel experimental approach for measuring the temperature-dependent minority carrier lifetime of crystalline silicon wafers, bricks, and ingots. The setup integrates a BCT-300 lifetime measurement system (Sinton Instruments) with a Peltier element regulated by an external temperature controller. To provide electrical insulation between the silicon sample and the Peltier module, a 5 mm thick quartz plate is positioned between them. The method was evaluated across a temperature range of 10–75 °C. The tested materials included six silicon bricks—four monocrystalline and two multicrystalline (mc-Si)—with thicknesses ranging from 1 to 2.5 cm, as well as ten wafers: two mc-Si wafers (194 μm and 260 μm thick) and eight monocrystalline wafers with thicknesses between 160 and 980 μm . Experimental results demonstrate that the proposed setup reliably measures temperature-dependent minority carrier lifetimes exceeding 1 μs within the investigated temperature interval. For most samples, the observed temperature dependence is consistent with predictions from the Shockley–Read–Hall recombination model under low-level injection conditions.

Optical Characterisation of Colour Centres in Nitride Layers

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Colour centres in wide-bandgap semiconductors, such as AlN and GaN, have attracted widespread interest due to their potential applications in scalable quantum technologies, particularly under room temperature conditions. These point defects have been shown to emit single photons across a broad spectral range, from the visible in both AlN and GaN to the telecommunication wavelength range in GaN, as reported in previous studies [1–6].

In this work, we have investigated various nitride layers to identify colour centres that are suitable for quantum applications. AlN films were deposited via sputter deposition at different temperatures on either sapphire or silicon substrates. Micro-photoluminescence (PL) spectroscopy employing sub-bandgap excitation was used to probe defect-related optical signatures. Confocal micro-PL mapping with a spatial resolution of 500 nm enables the localisation of individual radiative defects. However, the sputter-deposited layers exhibit a high defect concentration. Thus, photon statistic measurements were rather challenging. To address this issue, we investigated layers of comparably higher crystalline quality and reduced impurity contamination. AlN grown by metal-organic chemical vapour deposition (MOCVD) and GaN grown by high temperature vapour phase epitaxy (HTVPE) [7] using micro-PL, which yields a lower concentration of single defects. Our ongoing research focuses on assessing their single-photon behaviour.

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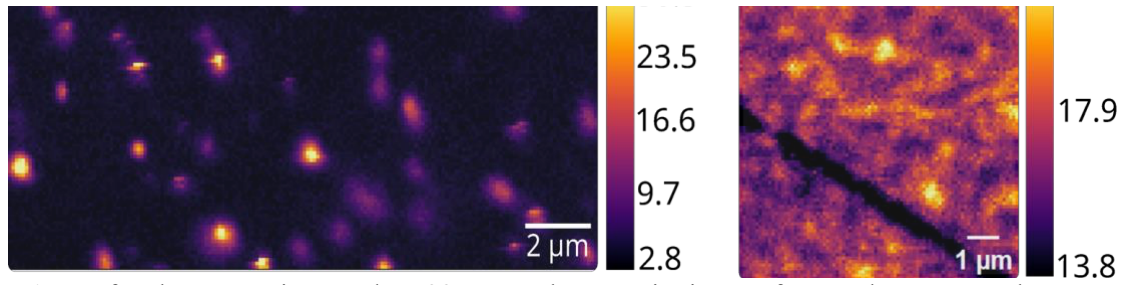


Fig. 1. Confocal PL mappings under 532 nm cw laser excitation. Left: GaN layer grown by HTVPE. Right: AlN layer sputter-deposited at 500 °C. Both layers are grown on sapphire substrate.

Origin and evolution of basal dislocations in HVPE grown GaN

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GaN bulk crystals of high crystalline quality are highly demanded as native substrates for the fabrication of vertical power electronic devices to avoid high densities of dislocations resulting from the use of foreign substrates and to minimize associated issues such as high leakage currents. Due to the possibility of realising high growth rates ($>100 \mu\text{m/h}$), these GaN crystals are usually grown by hydride vapour phase epitaxy (HVPE). Unfortunately, again the usual necessity of using foreign substrates like e.g. sapphire [1] generates dislocations, remaining strain and associated lattice bow in the grown bulk crystal [2]. Hence, it appears a challenge to achieve crystals of good crystalline quality.

In order to better understand the mechanism behind strain evolution during HVPE growth, we have investigated both, the evolution of strain and that of dislocation density of a highly strained HVPE test crystal of several millimetre thickness.

The threading dislocation (TD) density was determined by etch pit counting on the growth surface, whereas the evolution of the dislocation density inside the crystal was characterised by cathodoluminescence (CL) at cross-sections parallel to the growth direction. Dislocation types were further studied by transmission electron microscopy in order to identify Burger's vector and hence the direction of local strain. In addition, confocal micro-Raman spectroscopy at room temperature was applied to ascertain the overall residual strain.

The obtained data provide evidence that strain evolution in the bulk crystal is not only controlled by TD inclination [3], but also - progressively with increasing crystal thickness - by the formation of additional basal plane dislocations. Their formation correlates with the strain field originating from a developing lattice bow and the occurrence of macro-steps at the growth surface. Reasons for their formation are discussed in the context of dislocation types and their ability to reduce strain.

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Oxygen diffusion in Aluminium-Nitride

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Oxygen, as an abundant impurity, plays a significant role in group-III nitride semiconductors, strongly influencing their electrical properties [1]. When incorporated on nitrogen sites, oxygen acts as a shallow donor in gallium nitride (GaN) [2,3]. Alloying with aluminium generally decreases the free charge carrier density owing to the formation of compensation centers [4]. In aluminum nitride (AlN), oxygen substituting for nitrogen is discussed to form a deep, negatively charged center in the upper half of the band gap, which reduces n-type doping efficiency [5]. Although oxygen diffusion in III-nitrides has been recognized, quantitative assessments of particularly the bulk diffusion in GaN and AlN have remained limited [6,7].

We investigate the diffusion behaviour of oxygen in bulk AlN at 1600°C and 1700°C, using an Al oxide coating layer as oxygen source. Dynamic secondary ion mass spectrometry (D-SIMS) and time-of-flight secondary ion mass spectrometry (ToF-SIMS) was applied for accurate profiling of the oxygen concentration across the Al₂O₃/AlN interface. Initial tailing and limited dynamic range of ToF-SIMS measurements due to oxygen redeposition was addressed by employing an optimized dual-beam sputtering strategy with staged crater resizing. Additional artifacts in the chemical profiling arise from surface roughening and localized phase transitions from amorphous Al₂O₃ to partially crystalline Al_xO_y induced by the high-temperature annealing. Eliminating all these factors reveals that a limited thermal diffusion of oxygen into AlN occurs indicating an oxygen diffusion coefficient below $1.8 \times 10^{-16} \text{ cm}^2\text{s}^{-1}$ under these conditions [8].

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Photo-elastic Characterization of InP Wafers

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Single-crystalline InP is a well-known material in semiconductor technology, first developed for solar cells in extraterrestrial applications, and later was utilized for manufacturing devices for photonic and automotive applications, starting in the 1980s and experiencing rapid growth thereafter [1]. The progress of these technologies depends significantly on the availability of substrates with sufficient size. Recently, the processes have still been carried out using wafers with diameters of 2 - 4 inches [2]. However, upscaling to 6 inches is already well underway. These activities are supported by various characterization methods. The preferred methods should ideally be fast, capable of imaging and non-destructive.

Scanning Infrared Depolarization (SIRD) is an instrumentation which has been developed and applied for a long time for quality control and process monitoring of Si wafers under industrial conditions [3] with special emphasis on the recognition of defects and the evaluation of residual stress states. The system is continuously tailored for other materials and technologies. Its application to GaAs has also been described in several reports [4] and recently it has been further demonstrated for SiC [5] and AlN [6]. To our knowledge, reports on InP from other groups date back more than 20 years [7, 8].

SIRD exploits the phenomenon of optical birefringence, which is caused by the anisotropy of the refractive index, either natively (intrinsic) or induced by stress. The birefringence changes the polarization of the near-infrared laser beam that scans the sample, which results in a map of depolarization.

If depolarization is induced by stress, the map can be converted to shear stress by applying the stress-optic law. For this conversion, the photo-elastic constant C_s must be known. C_s varies depending on the material and crystallographic direction. Especially, there has been a lack of experimental data for the case of InP. Hence, C_s was determined for the corresponding crystallographic directions using a special calibration procedure. These values are compared with theoretical and experimental data from the literature for Si, GaAs, InP and SiC, respectively.

The new values of C_s were then applied to the characterization of 6 inch InP wafers by utilizing a procedure called Multi-Polarization Analysis (MPA), which allows imaging of the magnitude and direction of residual stress fields.

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Photo electrical characterization of the interface states in dielectric/AlGa_N/Ga_N structures

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The properties of GaN, such as the wide bandgap, the high breakdown field, and the polarization-induced high mobility two-dimensional electron gas at the AlGa_N/Ga_N hetero-interface, result in GaN-based high-electron mobility transistors with excellent performance. A suitable gate insulator that can form a robust interface with GaN is still under investigation. It is of fundamental importance to know and manage the surface- and buffer-related trapping phenomena that may limit the dynamic performance of GaN transistors.[1,2].

By photo assisted high-frequency capacitance-voltage (CV) characterization, it is possible to measure the total interface state density throughout the bandgap.[3]. In addition, to fully investigate the interface properties, the threshold voltage shifts due to charge trapping increasing the accumulation applied voltage can be monitored following the transient voltage shift caused by interface trapping effect and the retentive voltage shift which can be attributed to border traps.[4]

In this work, passivation thin films (Al₂O₃ and/or AlN) were grown on AlGa_N in GaN/AlGa_N based capacitor test structures. To investigate the interface properties, the density of the interface states has been characterized by means of photo assisted high-frequency CV characterization using monochromatic lights with photon energies up to 3.2 eV [3]. Using incremental (step 0.1 eV) photon energies, the interface charge difference in the energy range was measured. This approach can quantify the distribution of the interface states in the upper part of the band gap above the charge neutrality level (acceptor like states). The border traps have been investigated by applying an incremental positive voltage and monitoring the CV curves shift and hysteresis. [4]

The characterization of the interface and border traps allows a comprehensive characterization of the passivation oxide/semiconductor interface using different processes and combination of the passivation oxides. The data provide useful information about the interface of these systems that can be related to electrical properties.

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Photoluminescence spectroscopy study on hydride vapour phase epitaxy grown GaN:Mn using metal-organic precursor doping approach

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Semi-insulating substrates play a crucial role in high electron mobility transistors (HEMT) for 6G communication and power applications. For GaN-based HEMTs, SiC, sapphire, Si or GaN itself can be suitable semi-insulating substrate materials. Growing GaN-based HEMTs on semi-insulating GaN (homoepitaxy) should minimize the stress of the epitaxial layer and thus, thicker epitaxial layers can be achieved.

Semi-insulating GaN can be fabricated by transition metal (TM) doping [1], such as Zn, Fe, Mn or Cr. Among these TMs, doping with Mn in GaN introduces an acceptor level at about 1.8 eV above the valence band. [2] The most common growth method for bulk GaN is hydride vapour phase epitaxy (HVPE) for which growth rates of up to 300 μm per hour can be realized. [3,4] One possible approach to achieve Mn-doping is having a separate line in the HVPE reactor where the metallic Mn is overflowed by HCl. In this work, we used a metal-organic precursor (Bis(methylcyclopentadienyl)manganese – (MCp₂)Mn) and control the gas flow by a bubbler to growth bulk GaN:Mn crystals in a HVPE reactor.

Photoluminescence (PL) spectroscopy has been widely used to investigate defects in semiconductor materials. In this study, we employed extensive PL investigations, such as room-temperature and low-temperature PL as well as power-dependent PL. Moreover, above-bandgap, below-bandgap, and resonant excitation conditions were realized. Besides Mn-related PL features, the PL results also reveal the presence of C, Fe, and Cr impurity in the GaN:Mn, which may originate from the dopant precursor and reactor. Furthermore, we observed the screening of electron-phonon coupling of the Mn³⁺ internal transition at low temperature by comparison of both above and below bandgap excitation. Power-dependent PL measurements under resonant excitation conditions suggest that other impurities may act as recombination centres and compete for the relaxation of photogenerated charge carriers with Mn.

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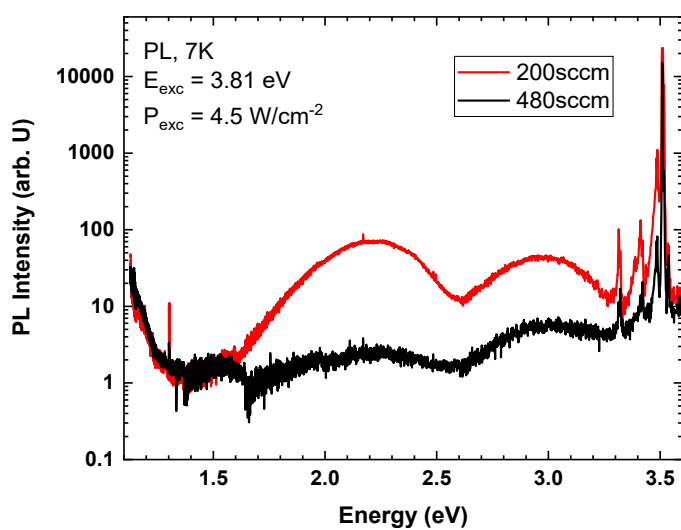


Fig. 1. Low-temperature PL spectra under above-bandgap excitation (325 nm) on GaN:Mn with two different Mn precursor gas flows.

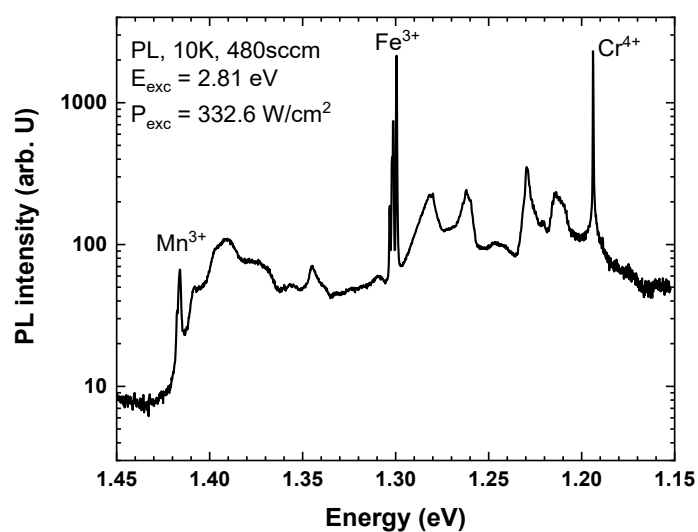


Fig. 2. Low-temperature PL spectrum of the spectral range dominated by internal TM transitions under below-bandgap excitation (442 nm) on GaN:Mn.

Response Surface Modelling for a Vertical GaN HVPE Reactor within a Constrained Design Space

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Understanding, modelling and optimising complex systems remains a major obstacle in many real-world applications. Design of Experiments (DoE) is a well-established statistical method for systematically investigating high-dimensional parameter spaces of such systems while minimising experimental effort. However, even with DoE, the number of experiments required for practical application can be far too resource-intensive, particularly when individual trials are time-consuming or costly. This limitation is especially acute in Hydride Vapor Phase Epitaxy (HVPE), a key method for the growth of GaN bulk crystals. To address these challenges, this contribution presents a systematic workflow that integrates DoE with physics-based simulations of mass transport and growth kinetics in HVPE, followed by metamodeling [1].

The proposed methodology first calibrates the physical simulation by a set of real growth experiments. Subsequently, a DoE is applied to strategically sample the parameter space, generating simulation-based datasets that serve as surrogates for physical experiments. By leveraging D-optimal and Central Composite Inscribed (CCI) designs, the DOE accounts for experimental boundary conditions inherent to HVPE reactors, ensuring physically meaningful parameter combinations. These datasets are then analysed using metamodeling techniques, which construct data-driven, interpretable models of system responses (e.g., growth rate, precursor efficiency) as functions of process parameters. The metamodel provides a simplified mathematical representation of the HVPE process, enabling the identification of correlations, optimal operating conditions, and hidden dependencies that would otherwise remain undetected. This approach drastically reduces the number of physical experiments.

By combining experimentally validated simulations with DOE and metamodeling, this study demonstrates a scalable and efficient method for optimising complex processes. The results offer valuable insights into the HVPE growth of GaN, paving the way for improved crystal quality and process efficiency in terms of precursor, energy, and time usage – while significantly reducing experimental effort.

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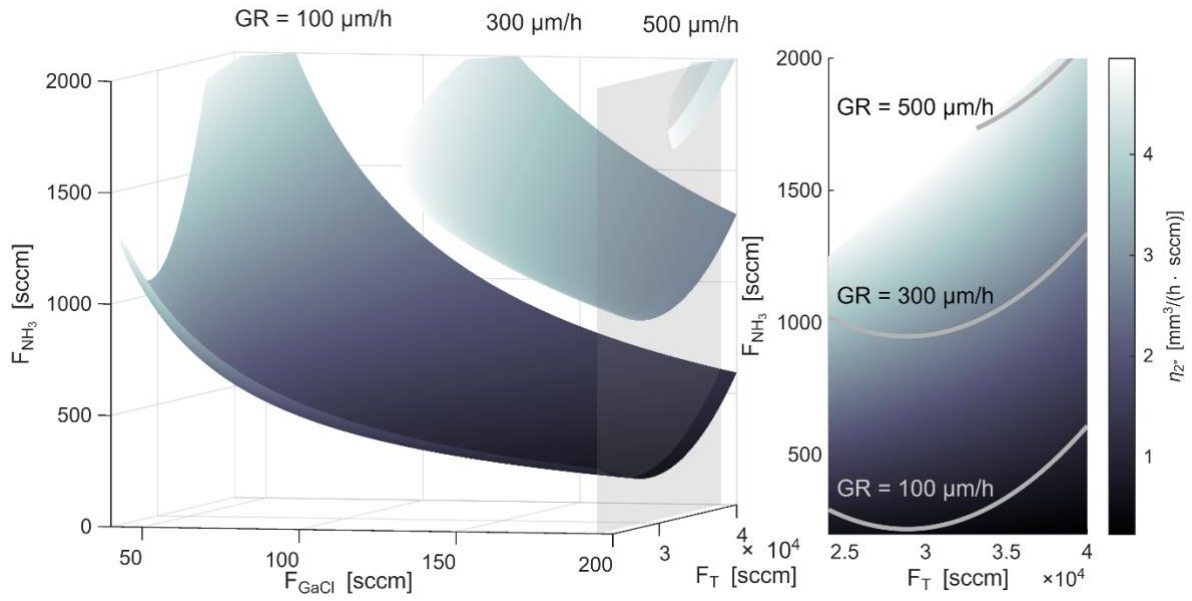


Fig. 1. Visualisation of the metamodel predictions for GaN growth:

(Left) Isosurfaces representing constant growth rates (GR) of 100, 300, and 500 $\mu\text{m/h}$ within the 3D parameter space of total flow (F_T), NH_3 flow (F_{NH_3}), and GaCl flow (F_{GaCl}), shown at a fixed H_2 ratio of 30%. The colour on the surfaces indicates the Ga precursor efficiency (η_{Ga}).

(Right) A 2D slice of the parameter space showing Ga precursor efficiency (colour plot) in the $F_T - F_{\text{NH}_3}$ plane at a fixed GaCl flow of 195 sccm. This plane is indicated by the grey slice in the left panel. The light grey lines represent the intersections of the constant growth rate isosurfaces from the left panel.

Strain-controlled directness and confinement margins in CGeSn/(Si)GeSn MQW emitters on (001) Ge/Si

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GeSn/(Si)GeSn multiple-quantum-well (MQW) active regions on (001) Ge virtual substrates are critical for on-chip mid-infrared laser integration. Achieving stable Γ -valley directness against the fluctuations inherent in epitaxial growth remains a central challenge. We analyze two reference architectures: HS-1, consisting of 30-nm wells and 20-nm barriers, and HS-2, with 15-nm wells and 15-nm barriers [1]. Composition and strain states were extracted via STEM-HAADF and atom-probe tomography. Using 8x8 k-p theory for Γ -derived subbands [2] and anisotropic effective-mass modeling for L-valleys [3], we determined conduction-band offsets and the directness metric $\Delta E(L-\Gamma)$ as functions of Sn/Si fractions and strain.

Scaling well thickness reveals a fundamental trade-off. Reducing the width from 30 to 15 nm blue-shifts the Γ_1 -HH1 transition from ~ 0.45 to ~ 0.50 eV at 5 K, but also narrows $\Delta E(L-\Gamma)$ from 34–41 meV to approximately 10 meV. With a thermal energy scale of $kT \approx 26$ meV at 300 K, the thin-well design operates with a sub-thermal margin. This makes the system highly susceptible to $\Gamma \rightarrow L$ carrier redistribution. The composition crossover point shifts from 14.9 at.% Sn in HS-1 to 15.4 at.% Sn in HS-2, proving that the directness threshold is a function of well geometry rather than composition alone.

Confinement robustness is governed by the barrier compositions. In Si-free GeSn barriers, increasing tin or relaxing strain drives offsets toward inversion, with HS-1 failing first. Introducing ~ 5 at.% Si suppresses this collapse [4]. This addition maintains positive offsets and preserves the directness margin against growth fluctuations. These results define quantitative design rules linking well stoichiometry and barrier Si content to ensure performance in next-generation MQW epitaxy within the LASTSTEP Horizon Europe framework.

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Study of Defect Physics in Zirconia MIM Capacitors

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Introduction

Zirconia (ZrOx) plays a pivotal role in advanced semiconductor memory devices [1]. Thus, comprehending defect dynamics is imperative, as they represent the primary driver of device failure. We comparatively investigate as-deposited (AD), post-deposition (PDA) & post-metal annealed (PMA) ZrOx. PDA exhibits suppressed temperature (T) sensitivity in both time-dependent dielectric breakdown (TDDB) and current-voltage (IV) data. Additionally, noise spectroscopy uncovers a distinct defect generation mechanism for PDA. We provide a granular overview of ZrOx defect physics, in light of its thermal history.

Experimental

We study 100² μm² plasma-enhanced atomic layer deposited (PEALD) 5 nm ZrOx metal-insulator-metal (MIM), with TiN electrodes. Annealing is done in N₂, at 550 °C, for 60 s.

Discussion of Results

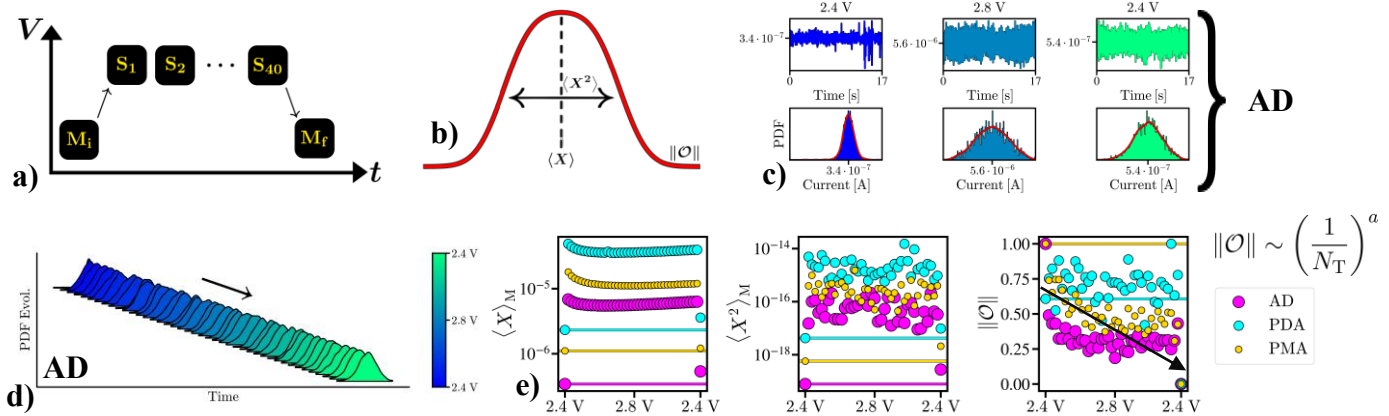
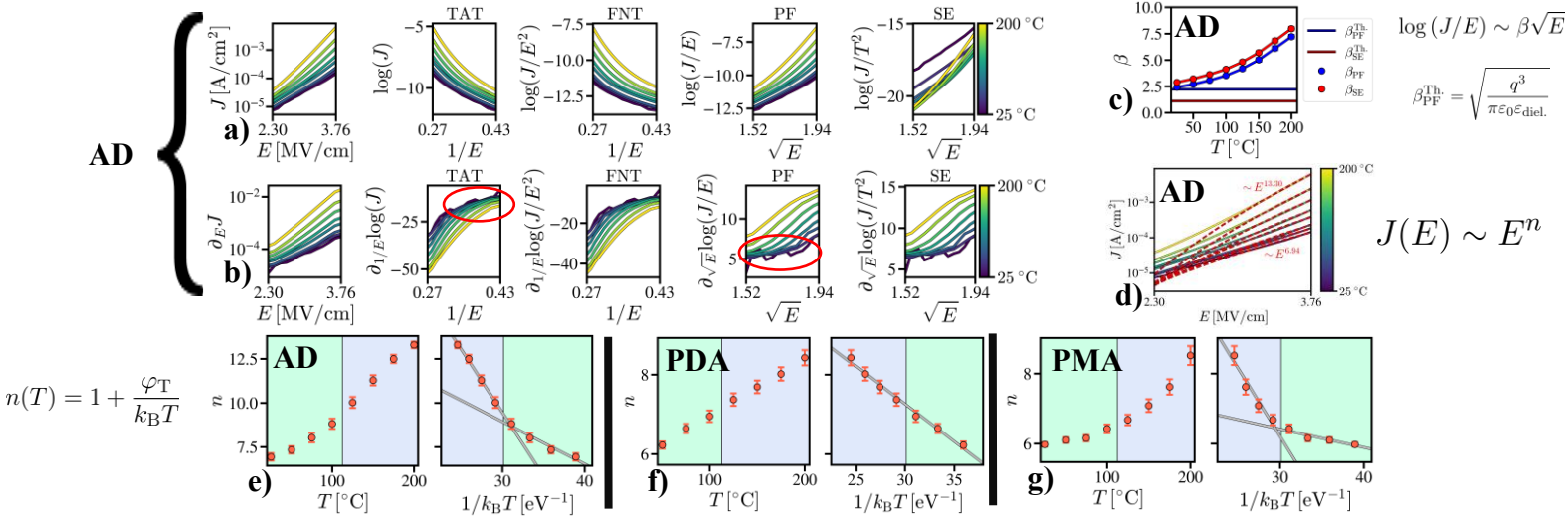
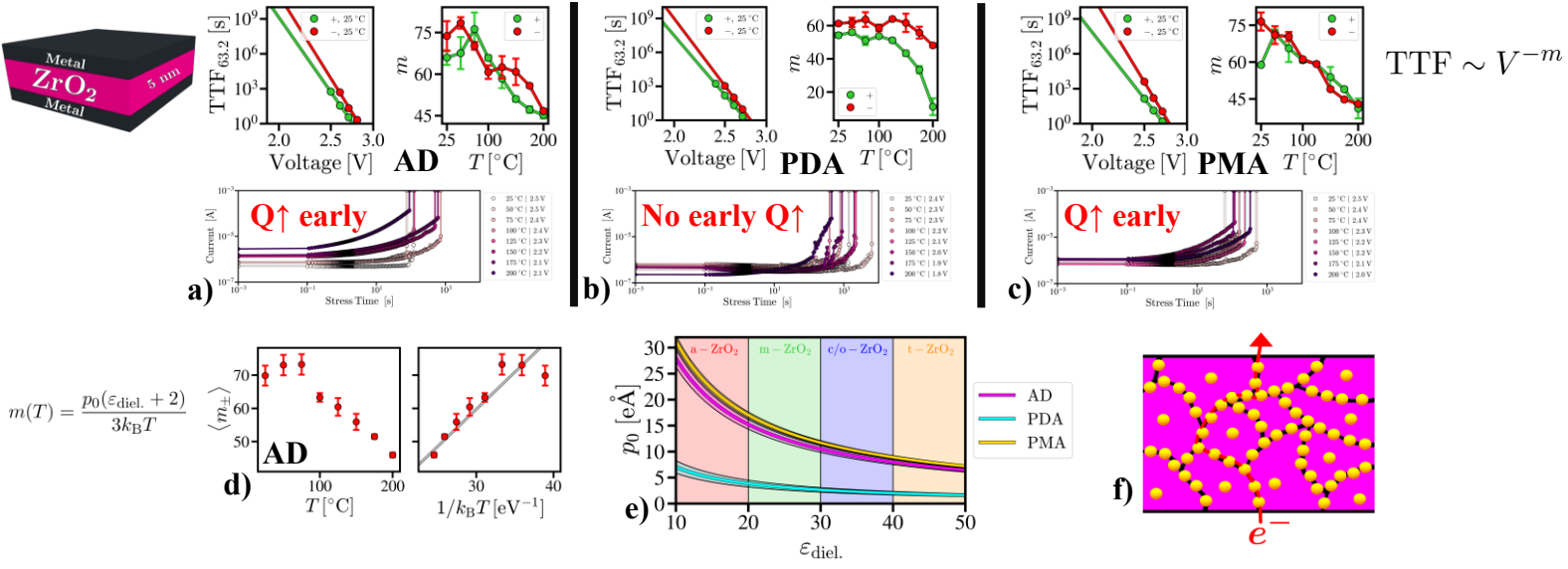
TDDB. The lifetime data (Figs. 1a-b-c) indicate PDA exhibiting a weaker T-dependence and a notable absence of early charges, in contrast to AD/PMA. PDA is a routine method to enhance the permittivity and induce crystallization [2], the latter concomitant with defect-dense grain boundaries (GBs) (Fig. 1f). Using the Lorentz relation [3] (Fig. 1d), we derive a (qualitative) link between the dipole moment and the permittivity (Fig. 1e): for bond rupture at the same field, the dipole moment scales inversely with the permittivity. **IV.** Trap-assisted tunnelling (TAT) and/or Poole-Frenkel (PF) emission are frequently reported for ZrOx [4, 5]. However, both models fail to align with our IV data (Figs. 2a-b-c). The leakage is solely accounted for by space-charge limited conduction (SCLC) [6] (Fig. 2d), corroborating the hypothesis of exclusive GB transport. For PDA, there is no dual T-regime for the SCLC exponent, implying uniform electronic transport physics across all T (Figs. 2e-f-g). The bond-breaking energy (~0.60 eV) is not contingent upon the thermal history. Conversely, PDA hosts shallower defects (~0.19 eV) than AD (~0.72 eV) & PMA (~0.39 eV). **Noise.** To elucidate defect generation, we execute a measure-stress-measure (MSM) protocol, with sense 2.4 V & stress 2.8 V (Fig. 3a). Building on prior research [7, 8], we employ higher-order moments as a defect-sensitive probe (Figs. 3b-c-d). This is exemplified by the first two moments' time evolution (Fig. 3e), remaining rather uninformative. The fourth moment, however, reveals a remarkable signature: AD/PMA obey the central limit theorem (CLT), wherein the noise decreases over time, owing to defect generation at constant voltage; for PDA, there is no such attenuation. This constancy is reminiscent of the PDA's TDDB time traces. We attribute this finding to the superior crystallization of PDA, relative to AD/PMA. Very defect-dense GBs do not appear to alter the stochastic nature of the ZrOx noise data.

Concluding Remarks

We present a comparative analysis of AD-PDA-PMA ZrOx. The pronounced T-dependence of TDDB, and the presence of dual T-regimes for AD/PMA, are absent in PDA. Instead, PDA defects appear T-insensitive, where the noise is non-conform the CLT. Our findings are consistent with Oxygen out-diffusion from ZrOx during uncapped PDA annealing, which is suppressed for AD/PMA, where TiN functions as a chemical & mechanical barrier [1, 2].

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Synthesis of artificial graphene in the AlGa_N/Ga_N heterostructure through block copolymer self-assembly

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Artificial graphene (AG) could represent an innovative system for creating quantum metamaterials and exploring novel electronic phenomena, since it may exhibit graphene-like properties, with the possibility of tuning parameters [1]. A simple fabrication method is nanopatterning the two-dimensional electron gas (2DEG) in semiconductor heterostructures [2–3]. AlGa_N/Ga_N heterostructures are a promising platform due to their relevance in high-frequency and high-power electronics.

This study investigates nanopatterning of the AlGa_N/Ga_N heterojunction using a mesoporous polystyrene mask with hexagonal pores. The AlGa_N layer was etched by reactive ion etching (RIE) with CHF₃+Ar or Ar. SEM shows uniform patterns for both chemistries, and cross-sectional TEM confirms that etch depth in Ar is controllable by adjusting RIE time.

Sheet resistance (R_s) and Hall effect measurements in the Van der Pauw configuration were performed at temperatures from 5 to 300K under a magnetic field ranging between –0.8 and 0.8T. Transport measurements reveal a difference between the two chemistries: samples treated with CHF₃+Ar show sheet resistance (R_s) and mobility (μ) trends similar to those observed in the unetched sample, although the electron density (n_e) increases at higher temperatures suggesting the presence of thermally activated impurities at room temperature. Interestingly, at low-temperature, an increase of the n_e values with RIE times compared to unetched samples is observed. Conversely, the sample processed with pure Ar exhibits n_e values equivalent to the one measured in the unetched sample but significantly higher R_s , with a low-temperature increase absent in the unetched sample. The effects of the various RIE chemistries on the transport properties of 2DEG will be compared and analyzed to identify the most promising approach for the synthesis of AG in AlGa_N/Ga_N heterostructures. The authors thank F. Cazzaniga and F. Somaini (STMicron Electronics, Agrate-Brianza, Italy).

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Synthesis of supersaturated GeSn alloys on Ge and Ge-on-Si by sputter deposition and nanosecond pulsed laser melting

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Over the last two decades, GeSn alloys have attracted considerable attention owing to their potential to achieve a direct bandgap at Sn concentrations above ~8 at.%, enabling the development of Si-compatible mid-infrared photonic devices. However, the low solid solubility of Sn in Ge remains a major challenge for the fabrication of high-quality layers with high Sn content.

Here, we report the fabrication of supersaturated GeSn alloys with Sn concentrations up to 20 at.% on Ge and Ge-on-Si substrates using a novel ex-situ two-step approach. First, a thin Sn film (<50 nm) is deposited on Ge(100) and Ge-on-Si substrates by DC magnetron sputtering. Nanosecond pulsed laser melting (PLM) then induces melting of the near-surface region, enabling rapid Sn diffusion and incorporation into the regrown Ge lattice. Owing to the strongly out-of-equilibrium nature of PLM, Sn concentrations well above the equilibrium solid solubility are achieved [1,2].

Secondary ion mass spectrometry (SIMS) depth profiles reveal box-like Sn distributions near the surface, confirming the formation of uniform GeSn regions. By adjusting the initial Sn thickness and the PLM parameters (laser energy density and number of pulses), both the thickness and the Sn content of the alloyed region can be finely tuned. Transmission electron microscopy (TEM) highlights Sn segregation along threading dislocations originating from misfit dislocations at the GeSn/Ge interface. The results indicate that the substitutional Sn fraction correlates with regrowth velocity: lower laser energy densities promote substitutional incorporation, whereas higher energies reduce it. An additional low-energy pulse (300–400 mJ/cm²) effectively restores substitutional Sn in samples initially treated at higher energy density (800 mJ/cm²). Reciprocal space maps reveal tensile strain arising from thermal expansion mismatch, which lowers the Sn threshold for the indirect-to-direct bandgap transition.

This approach provides a viable route to thick, uniform, supersaturated GeSn layers for advanced electronic and mid-infrared photonic devices.

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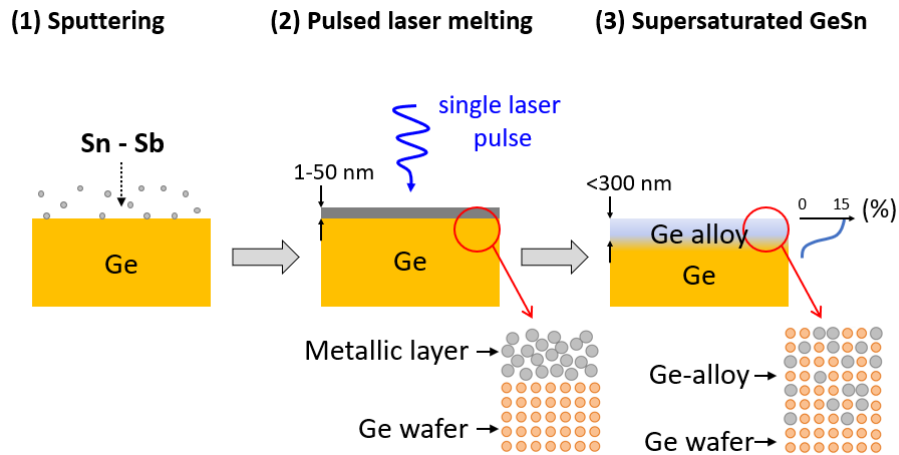


Fig. 1. Schematic illustration of the GeSn fabrication process based on sputtering deposition and pulsed laser melting.

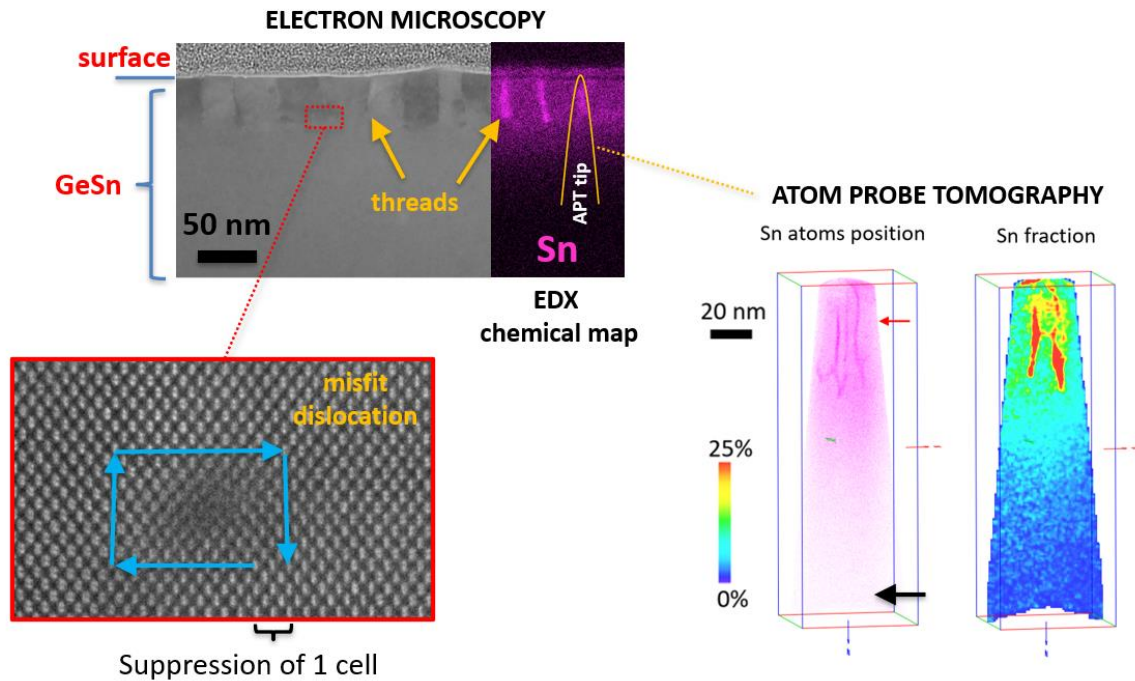


Fig. 2. TEM micrograph and APT 3D reconstruction of the GeSn sample, illustrating the material structure and local Sn distribution.

Towards Scalable Flexible Kesterite-based solar cells: Addressing Bulk and Interface Defects through Drop-on-Demand Inkjet Printing

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Cu₂ZnSn(S,Se)₄ (CZTSSe) kesterites are emerging chalcogenide absorbers for photovoltaics, offering tuneable bandgaps (1.0–1.6 eV) and high absorption coefficients. These materials can be grown on both rigid and flexible substrates, standing as promising candidates for Integrated Photovoltaics. However, their multinary nature leads to complex formation pathways and a high density of detrimental defects, including secondary phases, grain boundaries, voids and point-level defects that limit device performance.

Solution-based methods currently represent the most effective approach for CZTSSe synthesis. Among widely used techniques such as blade coating, spray pyrolysis, and dip coating, spin coating has historically yielded the highest efficiencies. However, the resulting film quality remains intrinsically linked to processing conditions highlighting the importance to develop synthetic strategies that allow the formation of high-quality absorber layers. Moreover, the spin coating technology's small-area limitations and large precursor waste still hinder the kesterite solar cells' scalability. In contrast, drop-on-demand inkjet printing is a promising and industrially appealing solution-based technique suitable for processing large areas. In this work, we address the scalability and defect-related limitations of kesterites by comparing traditional spin-coating with inkjet printing on flexible substrate.

The resulting devices exhibit parameters' enhancement over our spin-coated references, with a champion efficiency of 10.4%. Structural, morphological, and optoelectronic analyses confirm the superior quality of the inkjet-deposited absorber. However, recent studies confirm two main defective spots in the cell architecture, namely the bulk and the p-n junction interface. In the first, point defects are responsible of the V_{OC} deficit well-known for these materials, while the second represents the main low FF issue. Moreover, the CdS buffer layer conventionally coupled with CZTSSe, shows a detrimental cliff-like effect. Solving these defect-related issues, together with the scalable deposition by inkjet printing, would enhance the kesterite solar cells parameters allowing for their large-scale application in lightweight flexible integrated next-generation PV.

Controlling formation of single photon emitting colour centres in MOVPE of gallium nitride

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Point defects in gallium nitride (GaN) have recently emerged as a promising platform for room-temperature single-photon generation, exhibiting high emission rates and robust optical properties. GaN also benefits from well-established fabrication processes due to its widespread use in applications such as solid-state lighting and high power and high frequency electronics. Whilst wafers of bulk GaN are increasingly widely available, the material is still most commonly grown heteroepitaxially, and the use of silicon substrates allows for production of up to 300 mm diameter wafers. Meanwhile, GaN single photon emitters offer linearly polarized emission, Debye-Waller factors of approximately 50%, and the possibility of microwave control of optically addressable spin states. Overall, the combination of a relatively mature materials system and promising single photon emitter properties offer real potential for the development of scalable quantum technologies based on GaN.

However, the nature of the single photon emitting defects in GaN is unknown, and it has proved difficult to control their density or location. Early studies suggested that the emitters might consist of a point defect residing inside or next to a stacking fault (SF) [1], but attempts to engineer structures with deliberately included SFs to promote emitter formation met with little success [2]. For nitrides grown on sapphire, evidence has accumulated that the majority of emitters form close to the nitride/sapphire interface [3]. This location does not facilitate the fabrication of devices containing emitters, since it renders it difficult to position doped layers or elements of optical cavities below the emitter in the epitaxial stack.

However, the insight that emitters may form in the highly defective region at the GaN/sapphire interface has inspired efforts to try and reproduce the relevant growth conditions at a more convenient location: part way through the epitaxial stack in GaN-on-silicon material [4]. Following growth of Al(Ga)N layers required to control strain in GaN-on-silicon, and the growth of an initial GaN buffer, the GaN surface was treated with silane (SiH₄) and ammonia (NH₃) for 720 s to form a thin layer of SiN_x like that created during the initial nitridation step in GaN/sapphire growth. Thereafter a thin GaN layer was deposited at low temperature, and the sample was then annealed in ammonia at 1020 °C. This process resulted in the formation of a disordered array of GaN islands, the locations of which correlated with the locations of quantum emitters. A similar sample was capped with a further 3 µm of GaN, to increase the stability of quantum light emission by preventing reactions with air and surface charges. The capped structures contained defects which demonstrated bright single photon emission at room temperature, but which could be removed by etching away just over 3 µm of GaN, demonstrating that the emitters had formed at the intended depth. This is an important step towards control of quantum emitter locations in GaN-on-silicon.

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Photo-induced emission hopping of bright and regularly occurring native quantum emitters in AlN grown by molecular beam epitaxy

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Bright, stable and reproducible quantum emitters are essential for the development of photon-based quantum information processing or sensing. Aluminium Nitride (AlN) is an advantageous solid-state system for it possesses a very large bandgap of about 6,1 eV, is technology relevant and benefits from the availability of large substrates of high quality [1]. Besides, several theoretical works report on defects in AlN as candidates for solid-state qubits, as in [2]. In 2020, single quantum emitters consisting of point defects were reported in AlN, with emitters among the brightest reported to date. These centres show broad diversity of spectral emissions and shapes [3,4], yet are of still unknown nature and lack reproducibility. Very recently, several groups started to use femtosecond laser writing and ion implantation to investigate the production of intrinsic and impurity related defects. Here, we investigate an AlN layer grown on sapphire by molecular beam epitaxy (MBE) [5]. The growth mechanism of MBE might enable the formation of specific native point defects compared to other growth methods such as metal-organic chemical vapour deposition (MOVCD) used in [3,4]. We present a spectroscopic study of the native defect centres, without post-treatment after the growth. Amongst the wide diversity of bright ZPL emissions observed here, we highlight the presence of regularly occurring defect centres with a set of discrete ZPL between 700 nm and 720 nm which seem to share the same origin. The centres are capable to emit single photons at rates reaching up to 2,2 MHz at saturation. We report on their properties such as polarisation diagrams and $g^{(2)}(\tau)$ functions. Furthermore, we investigate in detail the photo-induced hopping of the ZPL emission of several centres, which reveal a complex behaviour, suggesting configuration changes. Finally, we discuss the possible origin of these centres, especially regarding the *ab initio* calculation of the antisite $N_{Al}V_N$ intrinsic defect expected to have an optical transition at 713,6 nm [3], and discuss perspectives for future investigations.

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Non-destructive visualization of the threading dislocation content in PVT-grown bulk AlN on wafer scale

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Aluminum nitride (AlN) substrates grown by physical vapor transport are commercially available in sizes up to 100 mm in diameter. The quality of epitaxial layers and the performance of electronic and optoelectronic devices are expected to depend on the defect content of the substrate, especially in terms of the threading dislocation density (TDD). While it is possible to determine the TDD of AlN substrates by defect selective etching (DSE), a robust, non-destructive characterization technique on wafer scale is still lacking. In our work we extend laboratory-based monochromatic X-ray topography (XRT) that has been successfully used to visualize the screw-type threading dislocation (TSD) content in silicon carbide on wafer scale [1] by combining it with photoluminescence (PL) to get an even more detailed picture of the overall dislocation content in AlN.

TSDs are efficiently identified by single XRT measurements in backscattering geometry. To rapidly generate full-wafer TSD density maps even under varying contrast conditions and the presence of other defects, we employ a deep-learning based object detection model trained on various, manually annotated XRT images. Edge-type threading dislocations (TEDs) can be visualized by XRT using different diffraction conditions and in principle even the determination of the direction of the Burgers vector is possible. However, this approach is limited by long acquisition times, low dislocation contrast under asymmetric diffraction conditions and a relatively low spatial resolution due to overlapping strain fields of closely aligned TEDs. In contrast, full-wafer PL-mappings reveal optically active spots that coincide with TED positions as independently verified by DSE. The PL-signal originates either from the dislocation cores themselves, from scattering effects or from decorating point defects and is under further investigation. The results obtained by combining XRT and PL measurements coincide with those obtained by DSE, which shows distinct etch pit morphologies for different threading dislocation types [2]. Together, these two methods provide an efficient, non-destructive way towards a quantitative dislocation characterization in bulk AlN substrates.

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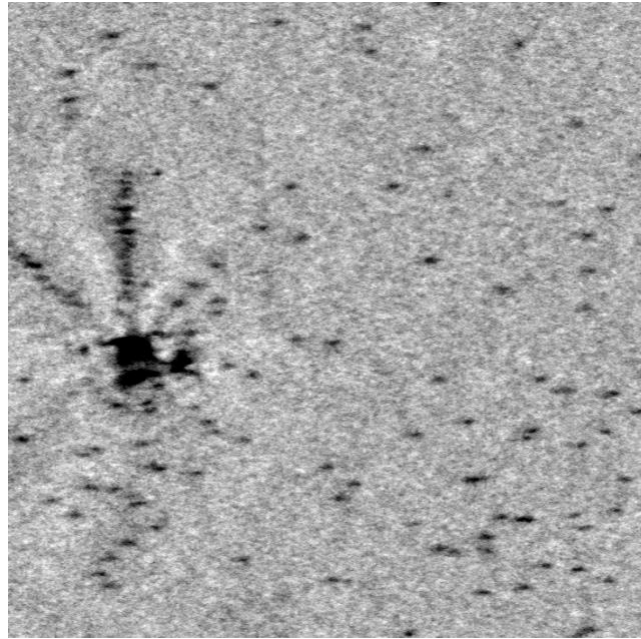


Fig. 1. Screw type threading dislocations (TSDs), measured by XRT in backscattering geometry with the diffraction vector $g = (0004)$.

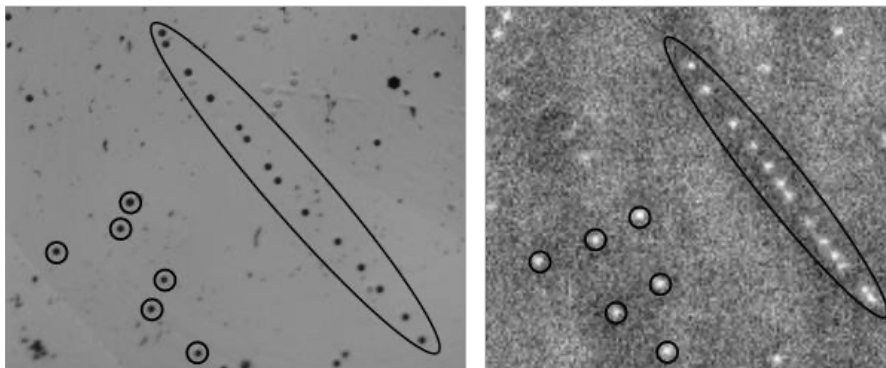


Fig. 2. PL-signal (right) originating from the positions of edge-type threading dislocations (TEDs), verified by comparison to a microscope image of etch pits after DSE (left). The slight mismatch between the positions is because the etch pits are visible on the Al-polar side while the PL measurement was performed with the N-polar side facing upwards. For dislocations with a slightly tilted line vector this results in a small positional shift between the two sides.

Plasma enhanced Atomic Layer Etching on Nitrides and SiC for high power and photonic application

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Atomic Layer Etching (ALE) is an enabling technology for next-generation electronic and photonic devices, providing highly controllable, low-damage material removal beyond the limits of conventional reactive ion etching (RIE). In this work, we demonstrate advanced plasma ALE processes for both AlGaIn/GaN and silicon carbide (SiC), addressing key challenges in device fabrication, reproducibility, and sustainability.

For AlGaIn/GaN HEMTs, plasma-based ALE using cyclic Cl₂ surface modification and low-energy Ar ion removal enables precise gate and ohmic contact recess etching with excellent etch-per-cycle (EPC) control. We show that process reproducibility is strongly influenced by chamber wall contamination, where chlorine-related species desorb during the removal step and disturb self-limitation. Dedicated chamber cleaning and conditioning procedures, supported by in-situ optical emission spectroscopy, are demonstrated to be essential for stable and repeatable ALE performance. Furthermore, modified ALE schemes minimizing or eliminating purge steps reduce total process time by more than 60% while maintaining low EPC (~0.2 nm/cycle) and low surface roughness (~0.3 nm) [1]. Device fabrication confirms linear threshold voltage tuning and reduced ohmic contact resistance below 0.2 Ωmm [2].

In parallel, we present an adapted ALE process for SiC, a promising platform for integrated photonics and power electronics [3]. Compared to conventional RIE, ALE enables damage-free, surface smoothening, and reduction of background radiation from defect states such as silicon vacancies [4]. These results highlight ALE as a versatile and unifying process technology for integrated electronic and photonic devices based on wide-bandgap materials.

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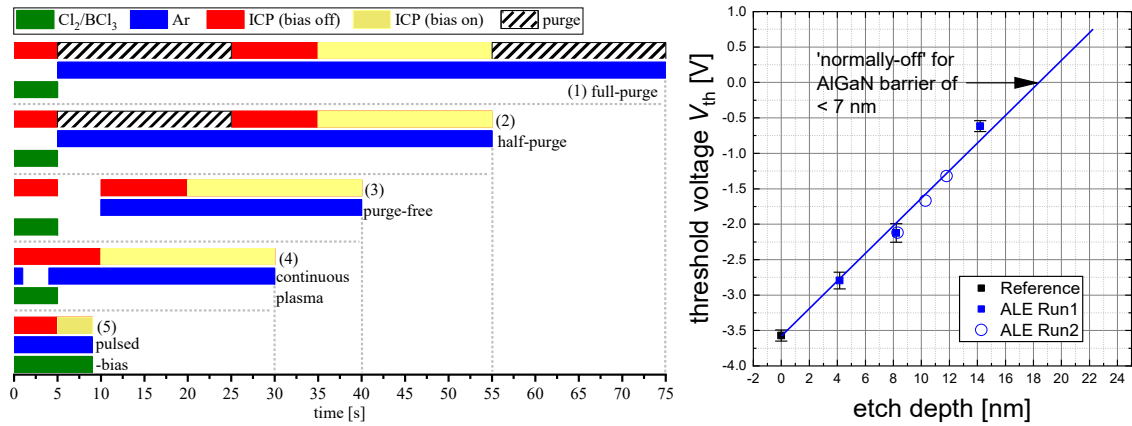


Fig 1. (a) Cycle sequence over time for the five different ALE modes. (b) Threshold voltage V_{th} extracted from step in gate capacitance. V_{th} increases linearly with etch depth

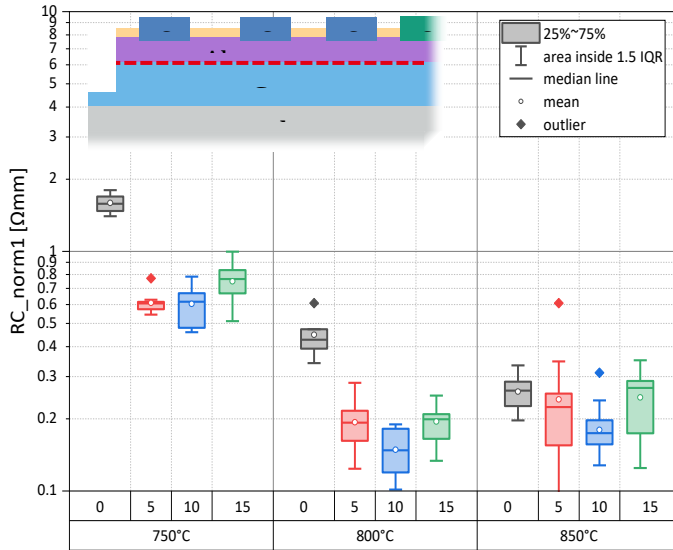


Fig 2. Results of electrical characterization of recessed ohmic contacts. Reducing the contact resistance for 750 °C, 800 °C and 850 °C annealing temperature with visible trend and optimum is achieved at 10 nm recess etch.

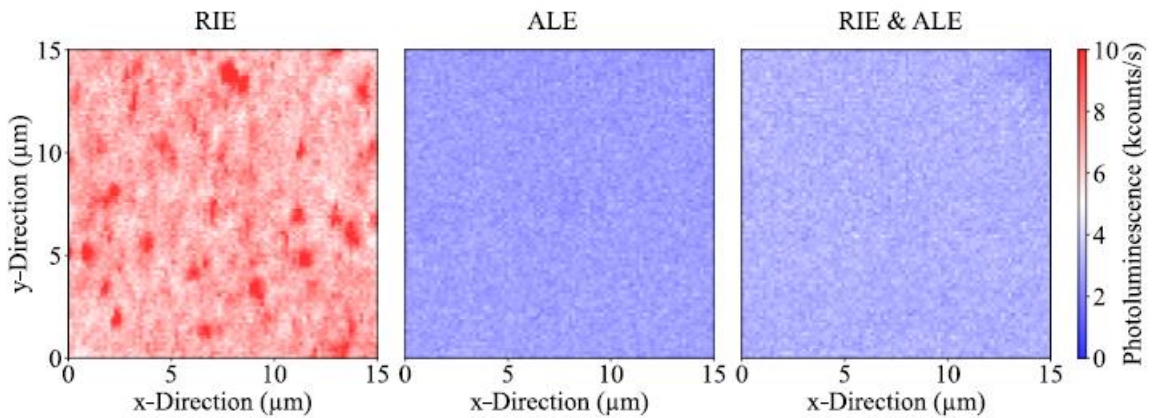


Fig 3. Comparison of three Photoluminescence Measurements of V_{Si} Maps of the differently dry etched samples. RIE induces significant surface damage on 4H-SiC, manifested as a bright background and point defects, whereas ALE produces defect-free surfaces and can fully remove RIE-induced damage, yielding indistinguishable surface quality compared to sole ALE processing.

Metal-Halide Perovskites and Their “Magic” Defects

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Metal-halide perovskites (MHPs) have emerged over the past decade as a remarkable class of semiconductors, enabling versatile and efficient optoelectronic devices, most notably solar cells with efficiencies exceeding 25% in single junction. Unlike conventional covalent semiconductors such as Si or GaAs, MHPs are relatively soft and dynamics ionic solids with a highly polarizable lattice and a complex nanoscale structural landscape. These characteristics give rise to somewhat unusual defect physics. In this talk, I will discuss several properties that, in my view, make perovskites quite different from conventional semiconductors.

One striking feature of MHPs is their apparent defect tolerance, manifested by the relatively high photoluminescence yields and excellent photovoltaic performance that can be achieved even in materials prepared by low-temperature solution processing, where high defect densities would normally be expected. A commonly invoked explanation is that defects are indeed present but somehow do not introduce efficient non-radiative recombination pathways.

At the same time, MHP materials and devices are well known for their stability challenges, which remain a major obstacle to large-scale technological deployment. This instability is closely related to the softness of the lattice and the mobility of ionic species, which enable the formation, transformation, and annihilation of defect states. However, in many cases the degradation of optoelectronic properties is at least partially reversible and is often referred to as *self-healing*. These phenomena reflect the dynamic nature of the lattice and the presence of reversible chemical reactions within the material. From this perspective, defects in MHPs can be viewed as metastable entities whose type and concentration adapt to environmental conditions such as illumination, bias, or temperature, resembling a chemical equilibrium. This metastability is one of the reasons for the apparent defect tolerance of these materials.

I will illustrate these concepts using photoluminescence spectroscopy and microscopy of films and individual nano and microcrystals of MHPs, which provide highly sensitive probes of defect activity and carrier recombination dynamics.[1–5]

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Unravel the contribution of Bulk and Surface States in 2D-layered Perovskite by means of Photocurrent Spectroscopies

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Metal halide perovskites (MHPs) have emerged as highly promising materials for optoelectronic applications, including solar cells, LEDs, lasers, and X-ray detectors, owing to excellent photoactive properties and solution processability. However, 3D MHPs, despite their outstanding performance, are limited by ion migration and environmental instability.[1] Low-dimensional perovskites have therefore gained attention due to their improved structural stability, enhanced resistivity, and reduced ion mobility, making them suitable for stable devices. Nonetheless, the presence of electronic trap states, which hinder charge transport and affect long-term stability, remains a critical challenge.

Photo-Induced Current Transient Spectroscopy (PICTS) is employed to investigate defect states in 2D-like perovskite. Unlike conventional capacitance-based techniques, PICTS probes photocurrent transients, making it particularly suitable for highly resistive materials. The results demonstrate that PICTS effectively identifies electronic defect states in (PEA)₂PbBr₄, benefiting from its reduced ion mobility. Conversely, in MAPbBr₃, photocurrent transients are strongly influenced by ion migration, complicating defect analysis.[2] PICTS measurements performed on high-resistive ($\sim 10^{12} \Omega$) millimetre-sized single crystals of (PEA)₂PbBr₄ revealed three reproducible trap states. Arrhenius analysis determined their activation energies, with one level (~ 0.34 eV) attributed to bromine interstitials. Importantly, the defect signatures remained stable under repeated thermal cycling, prolonged optical biasing, high X-ray doses, and over one year.[3]

Further, to unravel the bulk and surface contributions to photocurrent generation, the bulk and surface defective states are studied with a combination of PICTS and TSC (Thermally Stimulated Current) to explain the different carrier transient dynamics observed in (PEA)₂PbBr₄ with a guard ring electrode configuration. With PICTS, the three known trap states are located either in the bulk or at the surface. From TSC spectra, a much higher trap density on the surface compared to the bulk is obtained. Moreover, the appearance of an additional low-temperature trap was observed with TSC.

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Atomistic Engineering of Nucleation and Defect-Mediated Phase Stability in MAPI Perovskites: An AI-Driven Computational Framework

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Lead iodide perovskites have emerged as transformative materials for next-generation photovoltaics, achieving efficiencies beyond 25%. However, their full-scale industrial integration through scalable vacuum-based deposition is challenged by complex nucleation pathways and the recurring instability of photoactive phases [1]. In particular, the transition between photoactive black phases and the non-photoactive yellow δ -phase remains a critical bottleneck, often mediated by intrinsic stoichiometric defects. Understanding the atomistic triggers of these transitions is paramount for engineering durable and efficient devices [2]. This study introduces a multi-scale computational framework designed to resolve the atomistic mechanisms of methylammonium lead iodide (MAPbI₃) nucleation and phase competition. Force fields have proven to be essential tools for studying properties of materials at different length and time scales. Recently, driven by higher data availability and powerful high performance computers, a new class of precise and efficient interatomic potentials, such as machine learning interatomic potentials (MLIPs), emerged [3]. This approach marks a paradigm shift, replacing physics-based functional forms of potentials with highly complex mathematical forms based on neural networks. These networks, trained on reference ab-initio datasets, can reproduce high-level quantum mechanical calculations with negligible errors, achieving accuracies comparable to experimental uncertainties. Our findings focus on the early stages of the MAPbI₃ nucleation from its methylammonium iodide (MAI) and PbI₂ precursors. The pivotal role of MAI vacancies in guiding the phase transformation landscape has been also investigated. By mapping the free energy surface using GPU-accelerated HPC resources, we identify kinetic stabilization routes to trap metastable photoactive phases. This research highlights the synergy between machine learning and semiconductor defect physics, offering a predictive theoretical roadmap for the synthesis of high-performance, phase-stable perovskite optoelectronics.

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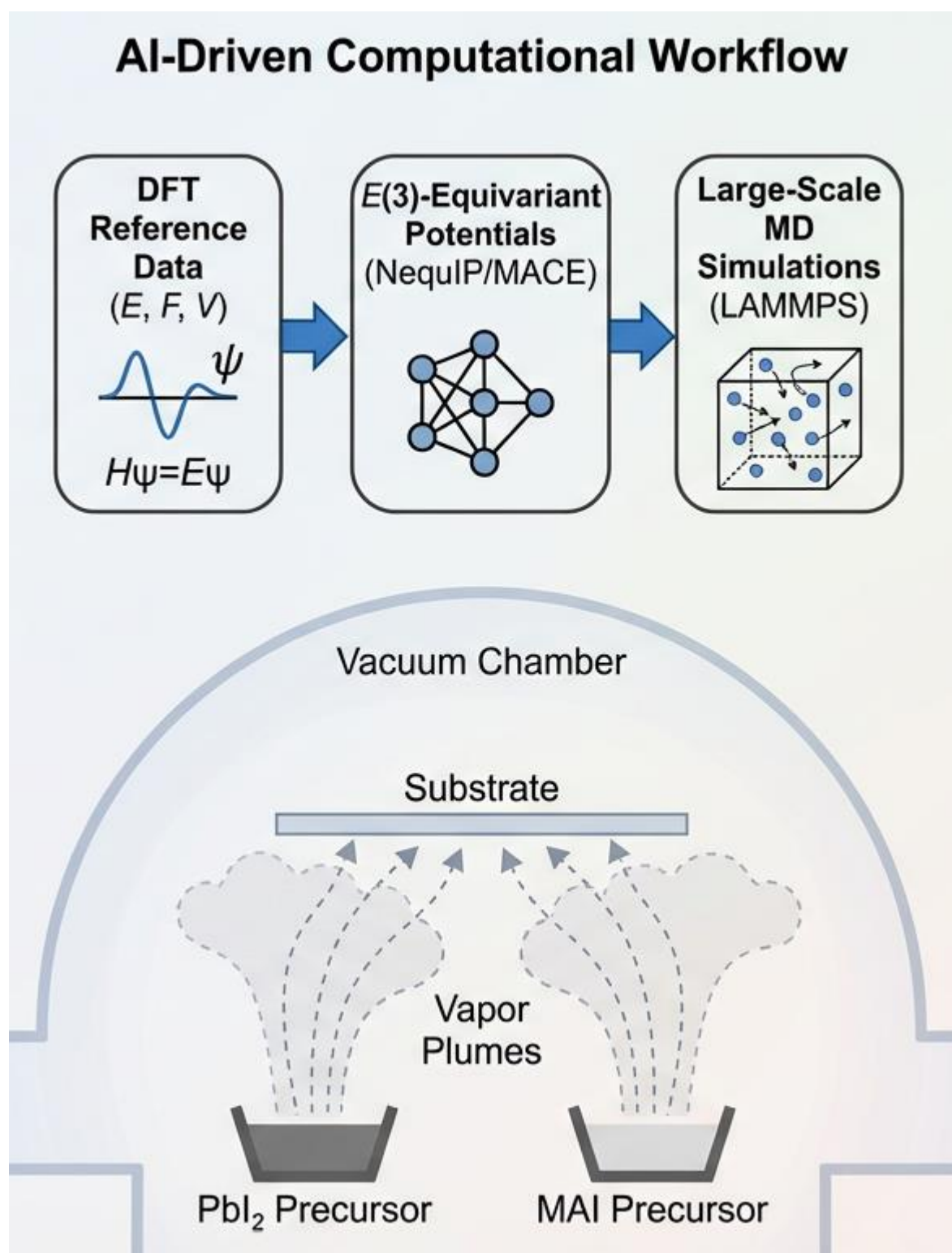


Fig. 1. AI-driven computational workflow and schematic of the vacuum-based deposition process.

Evaluating Structural Stability and Optoelectronic Properties of Lead-Free Metal Halide Perovskite Thin Films

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Lead-based metal halide perovskites have gained unprecedented attention in materials science due to their tunable optoelectronic properties and the ability to be processed into thin films using simple, low-cost techniques. Besides, lead-free counterparts have lately been considered promising alternatives to address the fundamental limitations (mainly, toxicity) of lead-based compounds. Tin- and bismuth-based perovskites have suitable optical properties and reduce health and environmental hazards. In this scenario, this study focuses on the growth, optimization, and fundamental characterization of thin films of CsSnI₃, MASnI₃, and MA₃Bi₂I₉. Chemical compositions and process parameters' impact on material quality and morphology have been investigated; structural and morphological analyses (XRD, SEM, and EDX) have been performed to examine how A-site and B-site cation substitutions affect the crystal lattice; optical characterizations enabled a direct correlation between material composition and crystallinity. Furthermore, managing defect formation and structural quality in these materials is essential to control their optoelectronic properties. While controlling defect density (and, so, tuning the resulting properties) proved relatively straightforward for the caesium- and bismuth-based perovskites, processing MASnI₃ presented significant challenges. A further optimization was required to control the rapid crystallization and nucleation kinetics for this specific composition. By managing growth dynamics, we successfully achieved MASnI₃ thin films with controllable defectivity and improved microstructural quality. These findings provide insights into the thin-film engineering of lead-free metal halide perovskites, guiding future processing strategies for advanced semiconductor applications.

Diffusion and Defect Reactions in Semiconductors: Progress and Challenges

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Germanium served as the primary material for semiconductor devices in the 1940s and 1950s before being superseded by silicon. Consequently, scientific research shifted toward silicon, focusing on the characterization of dissolved foreign atoms to control electrical conductivity and enable device miniaturization. While solid-state physics textbooks from the 1980s suggested that micrometer-scale doping inhomogeneities posed an objective limit to miniaturization (see e.g. [1]), decades of research into the diffusion of self- and foreign atoms have since enabled the fabrication of silicon-based structures in the nanometer range. This progress has been driven by the development of atomistic models that enable predictive diffusion simulations in silicon (see e.g. [2-4]). Unfortunately, these findings regarding silicon cannot be extrapolated to other semiconductor materials. As a result of the demand for the integration of germanium into silicon technology, interest in diffusion in this semiconductor was reignited in the 1990s and 2000s (see e.g. [5-9]). Indeed, a direct comparison of the experimental results reveals fundamental differences in the atomic diffusion mechanisms between silicon and germanium.

In this talk, results of experiments on self- and foreign-atom diffusion in silicon and germanium are presented in order to highlight the differences in the underlying diffusion-reaction mechanisms. Furthermore, an introduction to the mathematical description of diffusion in semiconductors is given to demonstrate that, whilst the diffusion mechanisms differ depending on the material, the mathematical formalism remains universally applicable. Finally, I highlight the relevant model parameters, the determination of which could form the focus of challenging experimental work, with a view to enabling predictive diffusion simulations for other semiconductor materials as well.

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Diffusion of p-type dopants in Germanium

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Due to the technological relevance of germanium (Ge) and Ge-rich SiGe alloys, the diffusion behaviour of n- and p-type dopants is of fundamental significance. The diffusion and doping behaviour of n-type dopants such as phosphorus (P), arsenic (As), and antimony (Sb) in Ge under intrinsic and extrinsic doping conditions is described by the vacancy mechanism, in which the substitutionally dissolved singly positively charged dopant atom A^+ with $A \in \{P, As, Sb\}$ is formed together with a doubly negatively charged vacancy V^{2-} through the dissociation of a singly negatively charged dopant-vacancy pair AV^- . In addition, a defect reaction leading to the formation of neutral dopant-vacancy complexes $(A_2V)^0$ is responsible for the deactivation of n-type dopants at high doping concentrations [1].

While the atomic mechanisms of diffusion of n-type dopants are well described, the mechanisms of diffusion of p-type dopants such as boron (B), aluminium (Al), gallium (Ga), and indium (In) are less well understood. The diffusion of B is several orders of magnitude lower than the diffusion of other p-type dopants (Al, Ga, In), and it remains unclear whether the vacancy or interstitialcy mechanism determines B diffusion in thermal equilibrium [2,3]. The diffusion coefficients of Al, Ga, and In are of the same order of magnitude, and it is assumed that the vacancy mechanism determines their diffusion, as this is very similar to the self-diffusion of Ge, which is dominated by vacancies [4,5]. The vacancy mechanism has been confirmed for In. Within a factor of two, the diffusion of In is the same under intrinsic and extrinsic doping conditions. This implies an identical charge state of the singly negatively charged substitutional dopant In_s^- and the mobile In-vacancy complex $(InV)^-$ [6]. Density functional theory calculations on the diffusion of Al and Ga diffusion in Ge show that the enthalpy of diffusion is similar to that of In. To clarify this question, additional experiments on the diffusion of Ga in Ge were carried out, the results of which are presented in this paper.

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Shallow junction formation in silicon by laser annealing of phosphorus end-terminated polymers

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Alternative approaches for Si doping have been explored to overcome the limitations of conventional techniques.[1-4] Precision polymer doping enables accurate control of the surface grafting density of P containing molecules [5,6] and efficient dopant drive-in by conventional thermal treatments, achieving high activation rate ($\eta_a > 80\%$).[7] In this work, we combine this approach with pulsed laser melting (PLM) to form abrupt P junctions in Si substrates. Polystyrene P-terminated homopolymers are grafted onto deglazed Si substrates to form a brush layer.[4-6] Drive-in is performed by PLM using 22 ns pulses of a KrF ultraviolet laser ($\lambda = 248$ nm) with energy densities of 500-900 mJ/cm². Calibrated ToF-SIMS P depth profiles upon 4 laser pulses at different energy densities (**Fig.1**) reveal clear box-like P profiles with extremely sharp junctions. Sheet resistance and Hall measurements in van der Pauw configuration demonstrate effective dopant activation ($\eta_a > 60\%$). Penetration depth and total P dose injected into the Si substrate (**Fig.2**) show a minimum energy density of 700 mJ/cm² required to activate the process. Above this threshold, depth linearly increases with energy density, while the total dose remains constant. Interestingly, only ~40% of P available in the source is injected, suggesting a release mechanism limited by trapping phenomena at the Si surface.[3] To investigate this phenomenon, we simulate the full PLM kinetics with both phase-field and atomistic approaches extending the features of the model for P injection events.[8] Good agreement is obtained only when surface P trapping events are included. This effect is amplified by the presence of SiO₂, that introduces ~3.0 eV P solubility barriers. This work establishes polymeric precision doping combined with pulsed laser melting, as an effective strategy for the incorporation of active P atoms to form abrupt Si junctions with concentrations up to 1×10^{19} atoms/cm³ and depths of ~25 nm.

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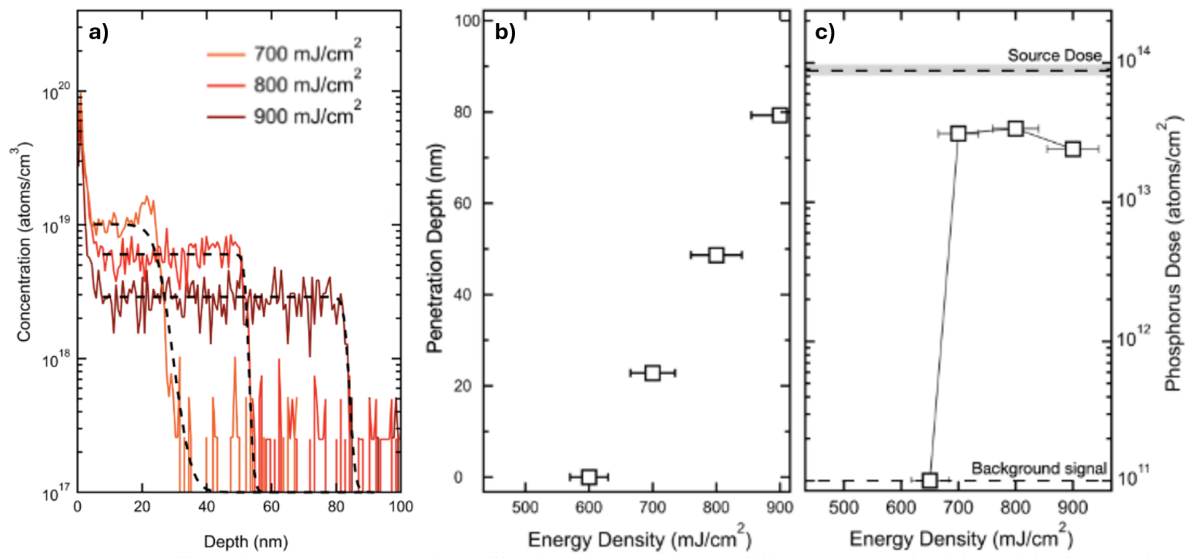


Figure 1. (a) Calibrated ToF-SIMS P depth profiles in Si upon PLM at different energy densities of the laser pulses. Penetration depth of P atoms (b) and total P dose injected (c) in the Si substrate as a function of the energy density of the laser pulses used during the drive-in process.

Modulation Acceptor Doping of Silicon: Induced defects in SiO₂ for hole generation in impurity-free Si

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Conventional impurity doping of nanostructured Si volumes, e.g. nanowires or nanosheets as used gate-all-around (GAA) FETs, suffers from various impediments such as: (i) deteriorated charge carrier mobility due to ionized impurity scattering resulting in slower switching speeds and increased heat dissipation, (ii) random dopant fluctuations (RDF), (iii) nano-size effects massively decreasing doping efficiencies due to dielectric mismatch, quantum confinement, etc. Moreover, conventional impurity doping is not cryo-compatible because charge carriers freeze out, unless degenerate doping levels beyond Mott's semiconductor-metal transition are considered.

Although it is inevitable to control the charge carrier type and density in Si for any device application, it is *not* mandatory to incorporate dopants into the semiconductor volume itself. Here, we present a method that allows to relocate acceptor dopants from substitutional sites in the Si or SiGe lattice into an adjacent SiO₂ layer [1]. Modulation Acceptor Doping (MAD) uses unoccupied acceptor states generated by specific trivalent acceptor impurities incorporated in SiO₂ with energy levels below the Si valence band edge. A direct and permanent ionization of these acceptor states is realized by electron-tunneling from the adjacent Si, which creates holes as majority charge carriers [2], as schematically shown in Fig. 1. This p-type doping method provides higher hole mobilities (see table in Fig. 2(a)), self-adjusts its ionization density via an inter-MA Coulomb blockade (which removes RDF), is not significantly affected by nano-size effects, and cannot be frozen out by cryogenic temperatures (see Fig. 2(b)).

In this presentation, different modulation acceptor elements [3], as predicted by density functional theory (DFT), are compared, both by the oxide fixed charge (C-V measurements) and hole sheet density (Hall-effect). Finally, selected applications of MAD to transistor test devices are pointed out, e.g. back-gated junctionless Si nanowire transistors [4] and SiGe Schottky barrier field-effect transistors (SBFETs) [5].

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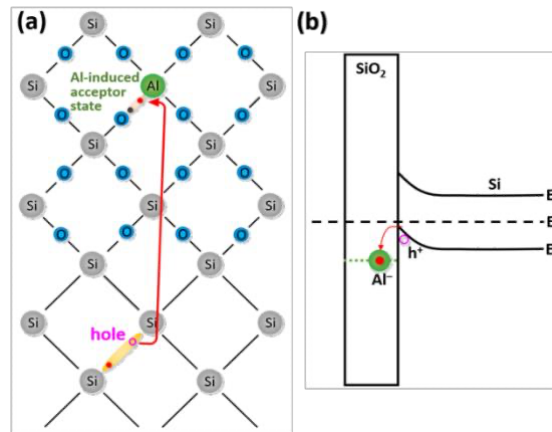


Fig. 1. Modulation Acceptor Doping (MAD) of Si by Al-induced acceptor states in SiO₂. (a) Schematic of the electron transfer process (note that the apparent crystallinity of the SiO₂ is just a simplification for the illustration, in reality the SiO₂ is amorphous). (b) Schematic band structure showing the energy level of the Al-induced acceptor state and the hole generation. Figures from [6].

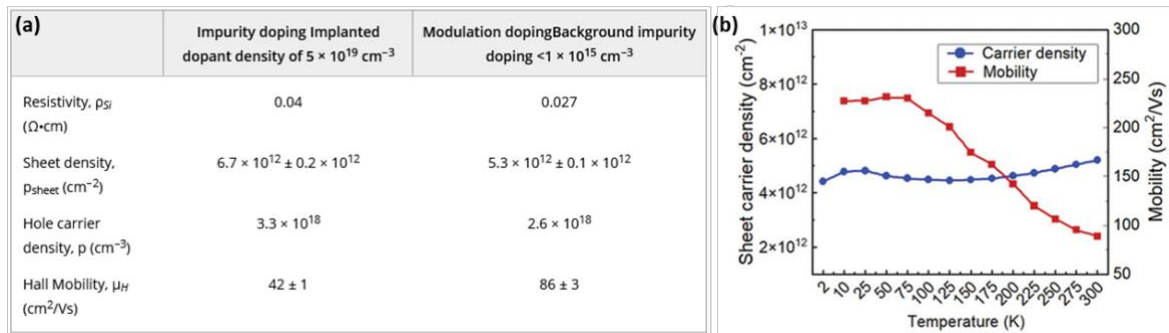


Fig. 2. Temperature-dependent Hall-measurement results: (a) Compared to a B-implanted reference sample (left column) with a similar charge carrier density, the hole mobility of MAD (right column) is twice as high due to the absence of ionized impurity scattering. (b) The hole density formed by MAD (circle symbols) is not frozen out at liquid helium temperatures. Figures from [2].

Beyond the Statistical Indeterminism of Ion Implantation: Toward Deterministic Nanoscale Doping and Defect Engineering

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Ion implantation has been a cornerstone technology for decades in the controlled doping of semiconductors and in surface modification of materials. Its strength lies in the precise control of ion species, energy, and dose. However, intrinsic structural limitations become increasingly evident as device dimensions shrink to the nano-scale or when atomic level deterministic control is required. The first limitation is statistical in nature which results in spatial uncertainty in the final position of dopants or defects, which becomes critical in applications requiring single-atom precision, such as quantum devices or engineered defect centers. In extreme conditions of fluence (below 10^{12} ions/cm²) processes become increasingly dominated by Poisson statistics, and the intrinsic non-determinism of ion–solid interactions is amplified [1-5]. Consequently, the variability from site to site increases, undermining reproducibility and device uniformity. Alternative approaches, like Focused-Ion-Beam (FIB) systems, demonstrate remarkable control at the single-defect level, but remain fundamentally serial and limited to small areas, making them unsuitable for scalable wafer-level fabrication.

These considerations suggest that optimization of conventional implantation parameters is insufficient. A revision of the implantation methodology is therefore required. We introduce a nanoscale electrostatically assisted implantation approach combining an insulating nanoaperture layer with a tunable surface potential grid. The electrostatic field generates localized potential wells that attract and funnel incoming ions toward predefined sites. The method does not eliminate the statistical nature of ion arrival; rather, it modifies the capture probability within each aperture Fig.1. By increasing ion collection efficiency, the approach reduces relative variance and improves control over the effective number of ions per nanoscale site under ultra-low fluence conditions. With joined modelling and experimental results, we demonstrate this hybrid geometric–electrostatic strategy provides a scalable parallel pathway toward enhanced determinism in nanoscale defect engineering, overcoming limitations of conventional implantation without relying on serial techniques such as FIB.

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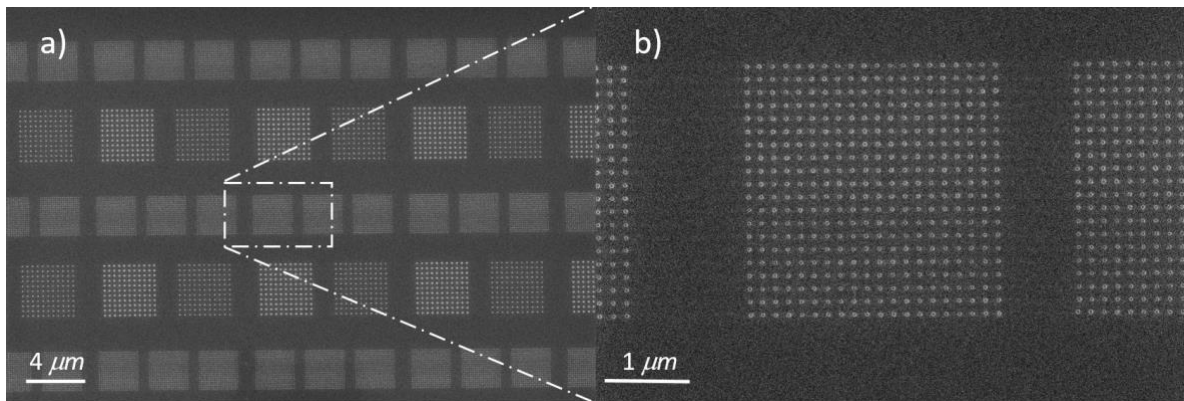


Fig. 1 SEM micrograph of a PMMA mask fabricated by electron beam lithography (EBL) for nanoscale ion implantation and defect engineering. (a) Large-area view of the patterned mask showing periodic implantation regions. (b) Magnified inset highlighting the nanoaperture array defining spatially localized implantation sites.

Dopant atom engineering quantum dot single-electron transistors and memory in silicon

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Dopant atoms in silicon provide a promising route towards the nanofabrication of quantum dot (QD) single-electron transistors (SETs) operating at room-temperature (RT) [1-3], where charge is precisely controlled at the one-electron level. The ability to manipulate single electron storage, transfer and switching in these devices raises the possibility of an ultra-low power, integrated quantum nanoelectronics in silicon, scaled to the ultimate, single-atom, one electron per bit, limit. The associated reduction in energy consumption, potentially to the atto-watt per device level [4], directly addresses major ongoing problems of exponential increases in the energy consumption besetting present-day data processing systems.

This paper discusses diverse examples of dopant atom QD devices, both for RT nanoelectronic applications, and more fundamental, single particle energy and entropy transfer experiments. Our devices exploit single-electron charging and Coulomb blockade of conduction in few nanometre scale QDs, formed by phosphorous (P) dopant atoms embedded within sub-10 nm point-contacts (Fig. 1(a)) [1-2]. Dopant atoms within either a few nanometre scale Si channel, or within SiO₂ regions, create deep QD potential wells, ~ 0.1 eV or more in depth, $\gg k_B T = 26$ meV at RT. RT single-electron charging and quantum confinement effects then occur, associated with the QD energy states, and control electron transfer across the point-contact. Figure 1(b) shows a scanning electron micrograph, and RT drain-source current I_{ds} vs. gate (V_{gs}) and drain (V_{ds}) voltage (c-d), in a QD SET [1,2]. We have also investigated 2-SET RT single-electron memory cells (e), where one SET controls charge transfer onto a memory node, and a second SET senses this with single-electron precision. Finally, the ability to manipulate electrons precisely is exploited in investigations of single-particle entropy and energy transfer, e.g., measurements of the minimum Landauer entropy of information, $S = k_B \ln 2$ [5], and ‘Maxwell’s Demon’ heat cycles [6].

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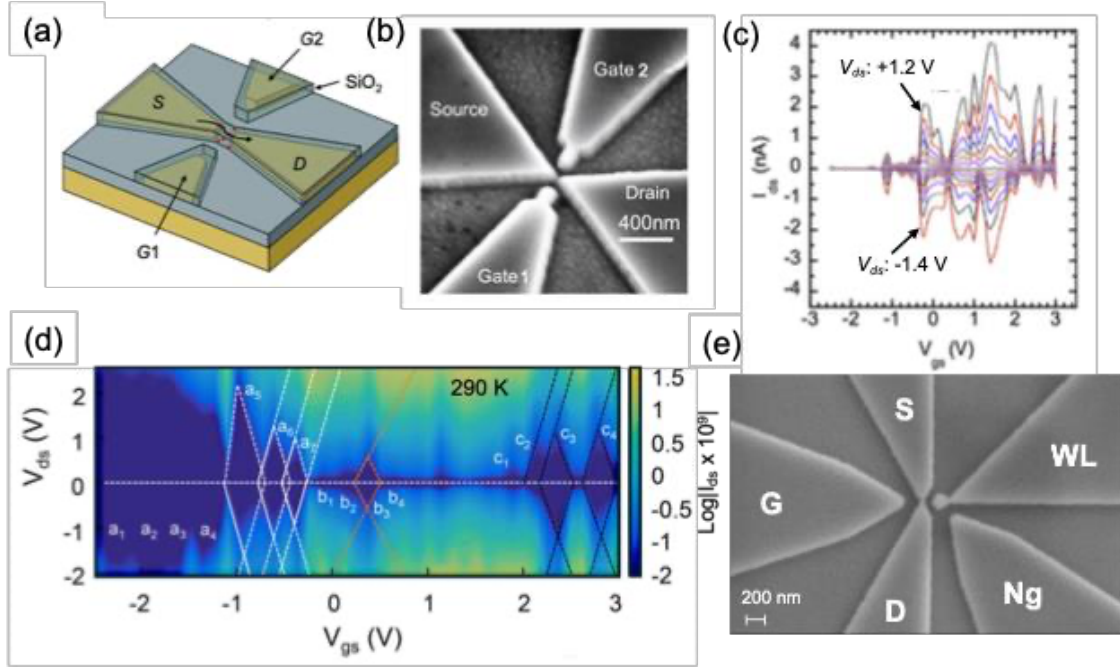


Fig. 1. RT dopant atom QD SET and memory devices. (a) QD SET schematic diagram. The device uses P dopant atom QDs within a point-contact nanochannel, located between source (S) and drain (D) electrodes. Gates G1,2 electrostatically control current. (b) QD SET scanning electron micrograph. (c) Single-electron oscillations in I_{ds} vs. V_{gs} , at different V_{ds} all at RT = 290 K). (d) Coulomb diamond charge stability regions in I_{ds} vs. V_{gs} , V_{ds} characteristics at RT. (e) 2-SET single-electron memory cell. Charge is transferred from word-line WL onto the circular memory node across a point-contact ‘control SET’, and detected by a sense SET (left half of image).

Tuning Kondo effect via two-dimensional confinement in highly doped silicon-on-insulator

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The relentless miniaturization of semiconductor devices necessitates a fundamental understanding of quantum transport phenomena that emerge at the nanoscale. While highly doped bulk Si typically behaves as a degenerate semiconductor with metallic transport, Silicon-on-Insulator (SOI) substrates introduces a dimensionality constraint and provides an effective landscape for exploring enhanced electronic and many-body interactions.[1]

This work reports on the observation of unexpected transport phenomena in ultrathin highly doped SOI films ($H_{SOI} < 25$ nm) revealing a distinct upturn of the resistivity (ρ) at low temperatures that was not observed in the same temperature range in similarly doped bulk Si (**Fig.1a**). This behavior is significantly affected by progressive 2D confinement which moves the resistivity minimum towards relatively high temperatures ($T_{min} \sim 30$ K).[2] This resistivity upturn is tentatively ascribed to the Kondo exchange interaction between conduction electrons and magnetic spins of diluted localized P ions.[3] Experimental data are well described by the Kondo fitting function, and the Kondo ρ_K contribution collapses onto a universal curve for all samples, a typical hallmark of this phenomenon (**Fig.1b**).[5]

To verify the dimensionality of the system, we performed magnetotransport measurements to investigate quantum Weak Localization (WL, **Fig.2**). Analysis of the magnetoresistance cusps and extraction of the phase coherence length ($l\phi$) using the Hikami-Larkin-Nagaoka (HLN) framework confirms progressive 2D confinement, with values significantly exceeding H_{SOI} . Crucially, the 2D confinement not only amplifies electron-electron interactions but also allows for the modulation of the Kondo temperature T_K toward higher and exploitable temperatures.

These results establish highly doped SOI as a controllable platform for engineering many-body interactions in Si. By demonstrating confinement-driven modulation of T_K , these findings provide key insights into spin stability and coherence mechanisms, with direct implications for Si-based quantum computation and spintronic devices.

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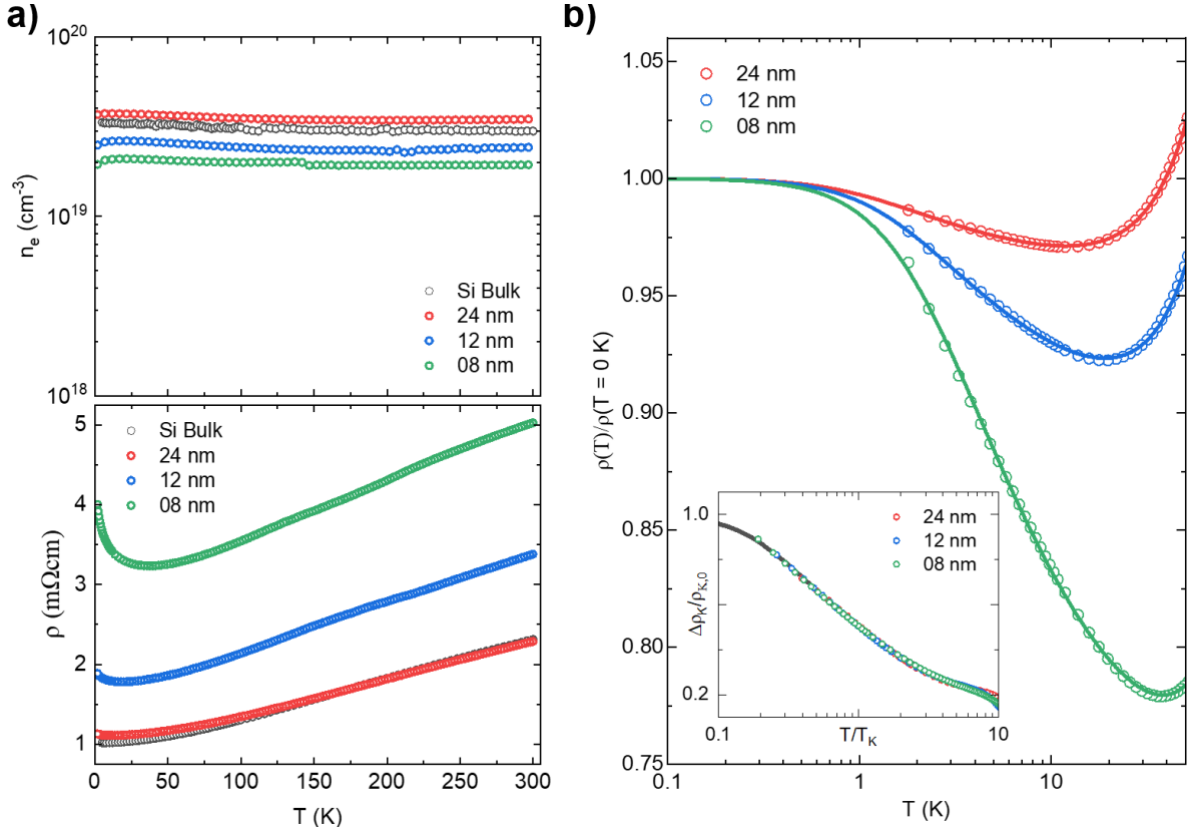


Fig. 1. (a) Low T carrier concentration (n_e , top) and resistivity (ρ , bottom) obtained on SOI samples with doping concentration $n_D = (4.6 \pm 0.5) \times 10^{19} \text{ cm}^{-3}$ and different H_{SOI} . (b) Low T normalized resistivity and corresponding fitting curve (line). In the inset, normalized Kondo resistivity plotted as a function of T/T_K for the SOI samples compared to the universal curve (black line).

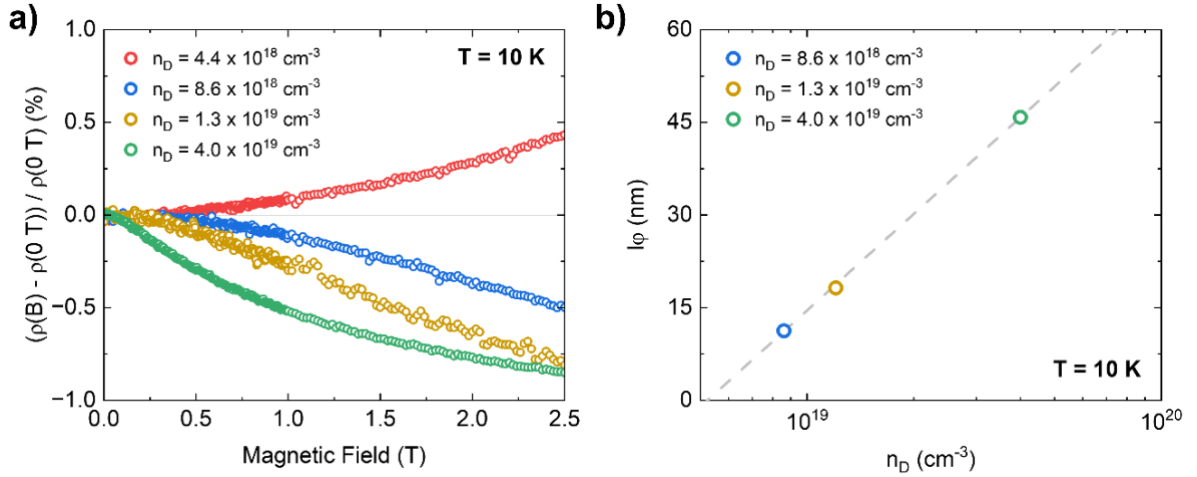


Fig. 2. (a) Magnetoresistance of SOI samples with $H_{SOI} = 23.5 \pm 0.6$ and different n_D ($T = 10 \text{ K}$). (b) Coherence length l_ϕ extracted from the HLN fitting function.

Engineering 1DEG system in pure silicon

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Confinement of the electron gas along one spatial dimension (1DEG) is of high interest for fundamental studies of quantum transport. Numerous practical applications, in quantum computing, spintronics, high-electron-mobility transistors, and further miniaturisation of electronic circuits can be considered as well [1]. The recent approach in engineering 1DEG systems is based on the application of 1D interfaces in 2DEG systems (see [2] and references therein). This approach requires integrating layers of various materials into the system and poses a challenge for device engineering. It would be advantageous if 1DEG systems could be formed within pure silicon without incorporating any other elements [3]. It was proposed that dislocation networks (DNs) formed by direct Si wafer bonding could serve as suitable objects for forming 1DEG systems [4–6]. Unfortunately, the poor reproducibility of the DN structures in bonded wafers probably prevented further studies. We discuss the possibility of applying rod-like defects (RLD) in Si as systems capable of forming 1DEG. Electromagnetic [7] and optical [8] properties of RLD in Si, and their comparison with those of dislocations, will be presented. The structure and formation mechanism [9] of RLDs will be considered to suggest possibilities of their controllable and reproducible incorporation in Si layers. In the case of successful fulfilment, especially in the ^{28}Si layers, it will be possible to obtain an exceptional 1DEG systems (see the Table).

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Table. 1DEG systems in Si and GaAs

1DEG Systems	Magnetic noise	Coherence time (seconds)	Control method	Industry readiness
^{28}Si [3]	Near zero	1-2	Electric & magnetic	High (CMOS)
Natural Si [3]	High (^{29}Si)	10^{-3} - 10^{-4}		
GaAs [10]	Very high	10^{-7} - 10^{-9}	Mostly magnetic	Low

Exploring quantum effects and structural interplays in graphene-derived functional materials for sensing and beyond

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Graphene-derived functional materials stand at the forefront of modern nanoscience, captivating researchers with their exceptional electronic mobility, pronounced surface reactivity, and extraordinary tunability for advanced electronic, sensing, and emerging quantum technologies [1]. Among them, graphene oxide (GO) emerges as a remarkably versatile platform, whose rich landscape of oxygen functional groups enables facile processability, precise functionalization, and seamless integration into electronic devices [2,3].

In recent work, we provide a realistic description of this complex substrate by introducing high levels of oxygen functionalization, associated to engineered defectivity, that reproduce experimentally measured proportions among distinct functional groups. This approach reveals a remarkable richness of defects, structural configurations, and, most importantly, tunable quantum confinement regimes (*e.g.* Fig. 1a), particularly in connection with advanced physical processes [4].

Intrigued by the material potential, we developed a functionally enhanced Field-Effect Transistor (FET) sensor and exposed it to target proteins representing key biomarkers of Alzheimer's disease. The device exhibits a surprisingly selective and sensitive response (*i.e.* Fig. 1b) [5]. Supported by multiscale modelling, combining machine-learning interatomic potentials with Kubo-Greenwood electrical susceptibility derived from ab-initio calculations, we demonstrate that the sensor sensitivity arises from competing structural and quantum confinement effects that produce opposite electrical responses (*i.e.* Fig. 1b-c). These electrical responses are quantitatively reproduced by modelling and are activated by the electrostatic nature of the interacting macromolecules.

Overall, our findings introduce new concepts for exploiting functional graphene-derived materials across sensing, flexible electronics, valleytronics, and related disciplines.

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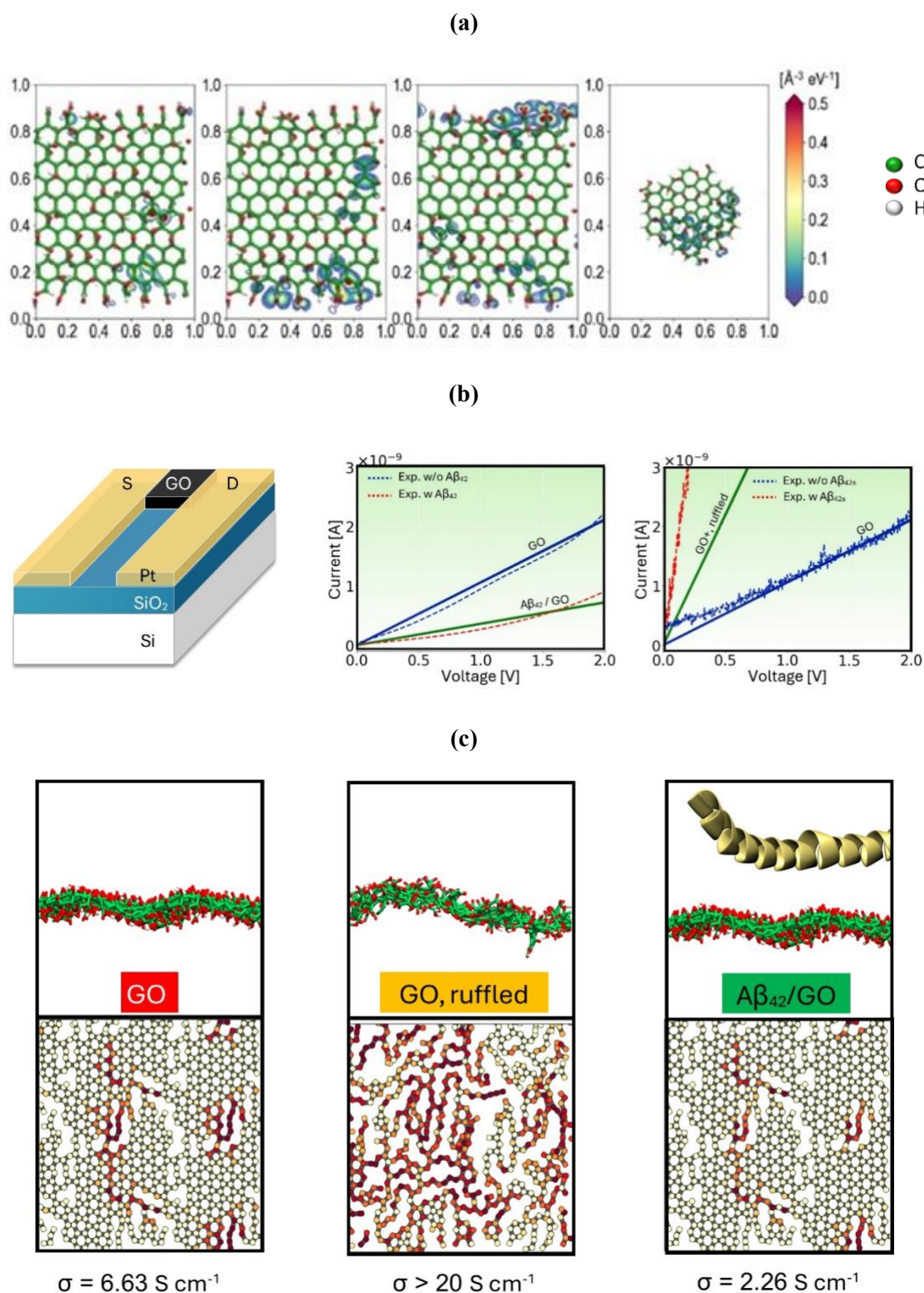


Fig. 1. (a) Richness of electrical, quantum-confined conductive states found in GO nanostructures; (b) sensor schematics and differentiated electrical responses, comparing simulated (solid lines) and experimental (dashed lines) device characteristics; (c) modelling of conductivity variation in GO arising from different structural configurations and protein-induced quantum confinement, along with the associated conductive states.

Sputter deposition and pulsed laser crystallisation of MoS₂ films

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The integration of transition metal dichalcogenides ^[1] (TMDs) into devices for nanoelectronics, optics, and sensing requires the development of a material growth method that is cheap, scalable, and compatible with the processes used in the semiconductor industry. An unconventional bottom-up approach is the use of Pulsed Laser Annealing (PLA) to crystallize amorphous TMDs deposited through sputtering ^[2,3]. The main advantage of this technique lies in the controlled and ultra-rapid thermal treatment confined to the surface of the sample. This work reports the results and subsequent considerations obtained from the PLA of amorphous MoS₂ films. More in detail, an excimer UV laser is used with wavelength of 248 nm and pulse duration of 22 ns to induce the crystallization of MoS₂ films with thicknesses in the range of 2 nm to 10 nm deposited on SiO₂/Si substrates. Therefore, the spatial and temporal confinement of laser annealing keeps the Si/SiO₂ substrate temperature well below the back-end-of-line temperature limit of Si CMOS technology (770 K) ^[3]. A variety of characterization techniques, such as Raman, AFM, RBS, XRD are employed to study the properties of the nanocrystalline films fabricated with an extensive range of deposition conditions and laser processing parameters. These results allow the investigation and optimization of the crystallization mechanism, a necessary step to improve material quality and to reduce MoS₂ film thickness down to a single or a few monolayers. Finally, this synthesis method presents interesting possibilities to selectively crystallize and as a future perspective also to dope MoS₂ layers, to speed up the integration of large-area 2D-materials with Si-based devices.

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Laboratory Photoluminescence imaging apparatus for identifying crystallographic defects in silicon

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Since 2017, a photoluminescence imaging apparatus ^[1,2] has been available on the market to identify crystallographic defects in silicon and locate them with micrometric precision during in-line inspection. The instrument integrates optical, electronic, and mechanical components, including a green excitation laser, infrared detection via an IR camera, and an automated stage. Photoluminescence emitted from defect bands ($\lambda > 1300$ nm) is isolated using optical filters, enabling detection of otherwise weak signals that are obscured by silicon's band-to-band emission at 1100 nm. This equipment has offered a significant improvement for process development and process control.^[3]

Now, a laboratory version of the tool is available thanks to joint work between my group at STMicroelectronics and the supplier of the in-line tool, opening the possibility of failure analysis and a deep characterization of the crystal defects.

In this talk, we present interesting results from laboratory characterization of crystallographic defects using micro-PL combined with various techniques, such as preferential defect etching, TEM, and SEM-ECCI, to compare the results of micro-PL with other imaging techniques. Moreover, data acquired from micro-PL imaging using polarization filters suggest the possibility of distinguishing defect types based on their emission polarization. A significant portion of the crystal defects emits linearly polarized light. In figure 1 an example of crystal defects generated by high-dose boron implantation shows that many defects are visible only with horizontal or vertical polarization filter. TEM analysis shows that this type of polarized defects consists of dislocation loop, whereas the unpolarized defects are stacking fault.

Importantly, the PL-based approach demonstrates higher sensitivity, revealing smaller and more numerous defects than chemical etching, which is the most widely used laboratory technique to measure, for example, the denuded zone in silicon substrates.

Other notable capabilities of the laboratory tool include the possibility to examine the cross-section of a silicon sample or to observe a silicon device from the back after substrate thinning, thus avoiding the observation obstacle caused by metallization.

In summary, the integration of advanced photoluminescence imaging with complementary techniques marks a significant step forward in the precise identification and characterization of silicon crystal defects, paving the way for enhanced process control and innovative failure analysis in semiconductor manufacturing.

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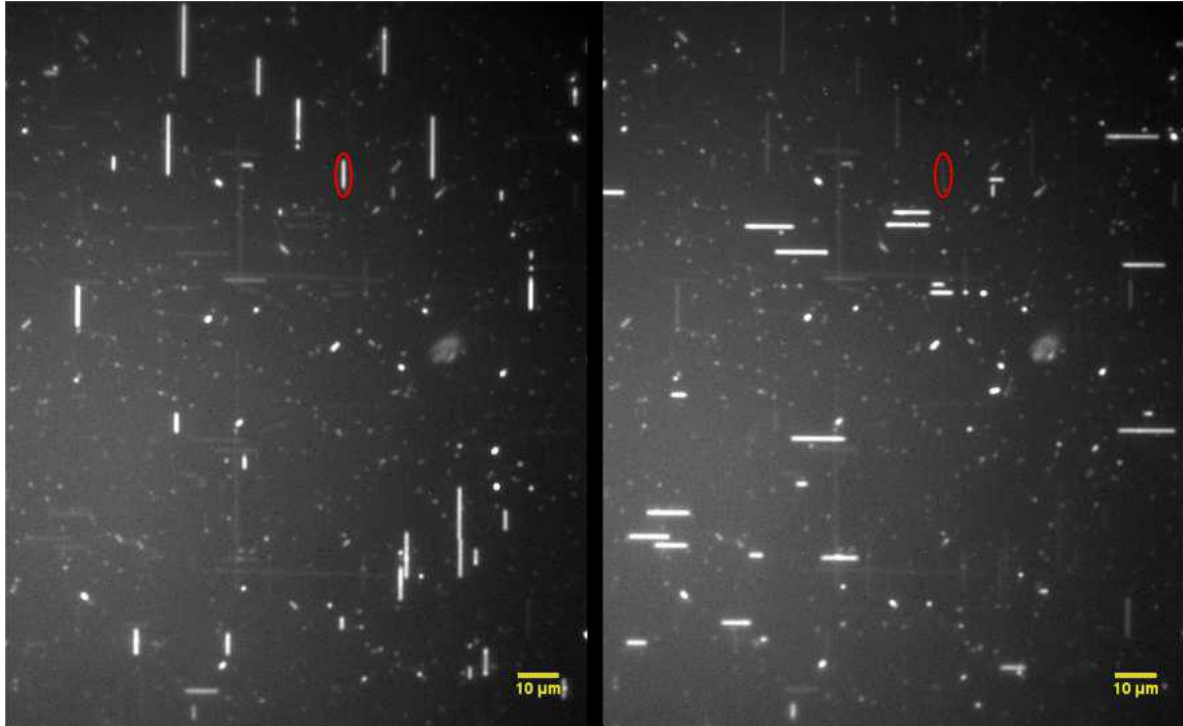


Fig. 1. Micro-PL image of crystal defects generated by a high-dose boron implantation. On the left is used the 1300 long pass vertical polarization filter, on the right the horizontal one.

A charge decoupling method to infer bulk recombination in high quality silicon wafers

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The bulk lifetime τ_{bulk} of high-quality silicon wafers is becoming increasingly critical as solar-cell efficiencies surpass 27%. This growing importance creates a strong need for direct measurement of τ_{bulk} . In this work, we present a non-destructive approach—termed the *Charge Decoupling Method*—that enables the extraction of τ_{bulk} in high-quality wafers [1]. The technique is straightforward, requiring only an atomic-layer-deposited (ALD) aluminium oxide (Al_2O_3) layer [2], or any film with a high fixed charge density (e.g., $>|10^{12}| \text{ q cm}^{-2}$), together with corona charging [3].

By monitoring the decay of the effective lifetime as the net negative charge is progressively neutralised through sequential deposition of positive corona charge, we can analyse the resulting curve—analogue to the fill factor of a solar cell—to determine both the injection-dependent τ_{bulk} and the surface recombination velocity S . To experimentally validate the method, we apply it to Al_2O_3 -passivated, Czochralski-grown, $5 \Omega \cdot \text{cm}$, n -type silicon wafers. The extracted parameters include a τ_{bulk} of approximately 30 ms and a corresponding S of 0.2 cms^{-1} at an injection level of $\sim 10^{15} \text{ cm}^{-3}$. However, τ_{bulk} can be resolved over a large range injection range, thus revealing hidden recombination active defects that cannot be resolved by other techniques.

Mathematically, we show that the charge decoupling method depends solely on the ratio of surface to bulk recombination when the fixed charge density in the dielectric film is $>|10^{12}| \text{ q cm}^{-2}$. As a result, it is inherently independent of doping type, resistivity, fixed charge density, wafer thickness, interface defect density, and the injection dependence of the bulk lifetime.

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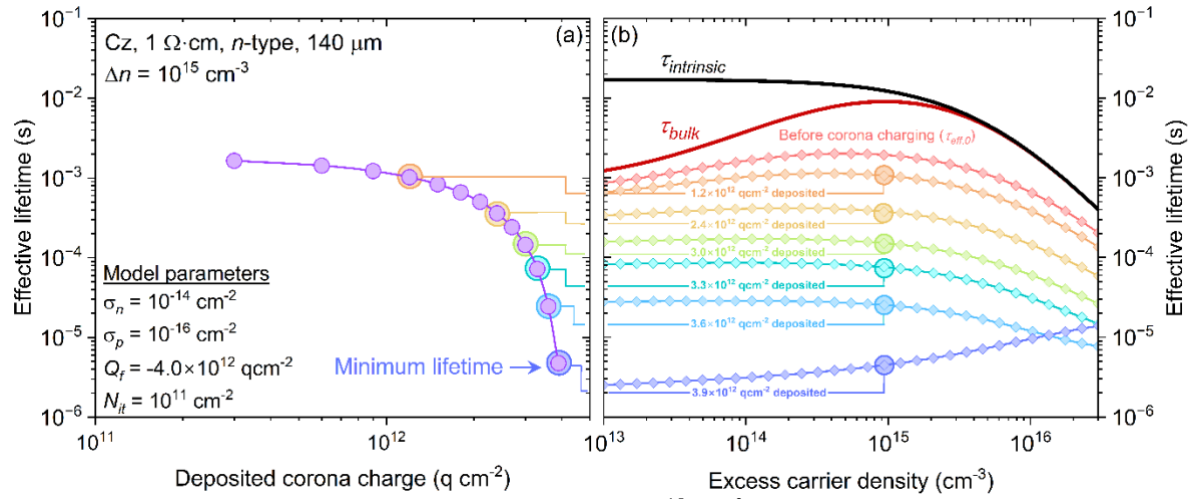


Fig. 1. (a) modelled corona charge curve at $\Delta n = 10^{15} \text{ cm}^{-3}$ and (b) the corresponding injection dependent lifetime curves. The amount of positive corona charge deposited per cycle has been set to $3.0 \times 10^{11} \text{ q cm}^{-2}$. For clarity, we have not plotted every effective lifetime curve in (b).

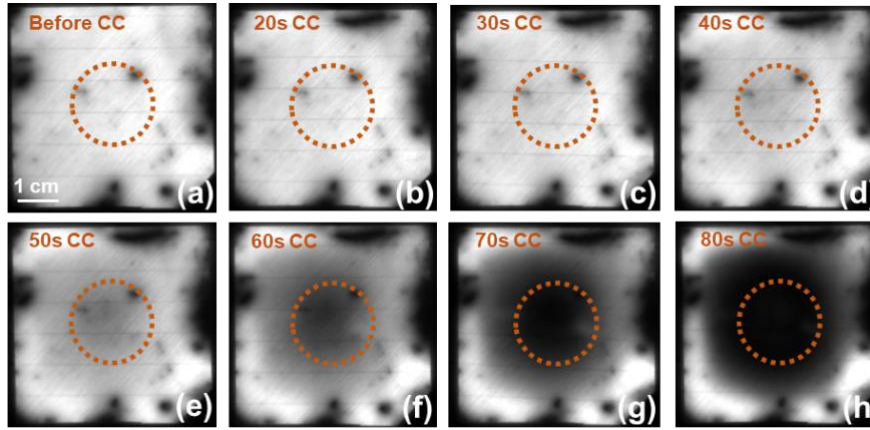


Fig. 2. (a)–(h) photoluminescence images showing the spatial uniformity of the deposited corona charge (CC). For clarity we have plotted every second image. The orange dashed circles in the images represent the area over which the effective lifetime is measured.

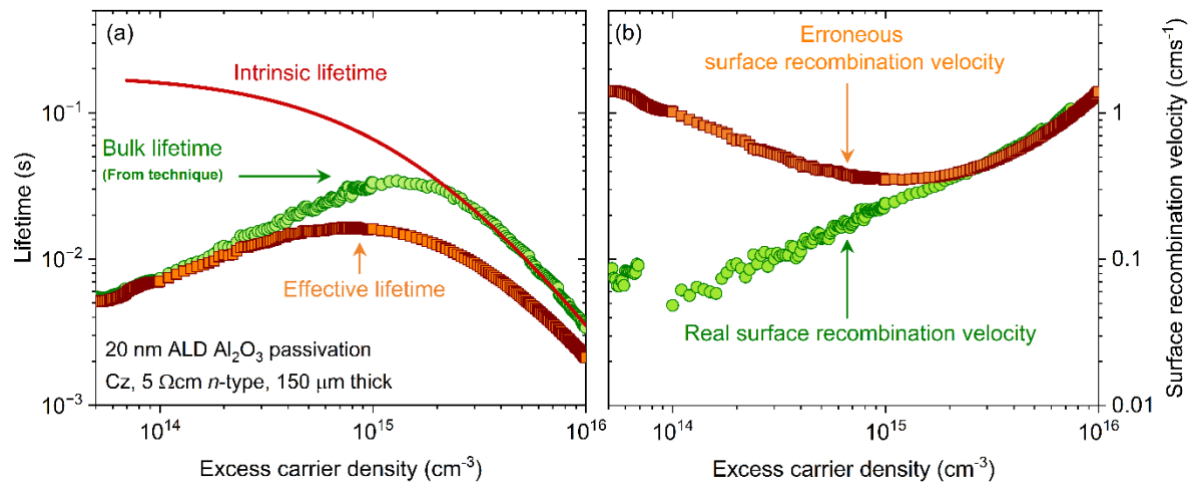


Fig. 3. (a) measured injection dependent effective lifetime of 20 nm Al_2O_3 passivated Cz, 5 $\Omega \cdot \text{cm}$, n -type, 150 μm silicon (orange squares), the injection dependent bulk lifetime using the corona decoupling method (green circles) and the intrinsic lifetime (red line). (b) the corresponding injection dependent S with (green circles) and without (orange squares) knowing the true bulk lifetime.

Beyond Conventional DLTS: Direct Observation of Isotope Shifts in Deep-Level Emission Using Laplace DLTS

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Hydrogen is one of the most ubiquitous and electrically active impurities in semiconductors, yet its direct identification in defect complexes remains challenging. In this study, we present the first application of high-resolution Laplace deep-level transient spectroscopy (DLTS) for the discrimination of hydrogen isotopes in defect complexes, opening a new pathway for defect identification in semiconductors.

By systematically comparing n-type silicon samples treated with H-plasma and D-plasma, we demonstrate that Laplace DLTS can resolve subtle shifts in the electrical properties of the carbon–oxygen–hydrogen (C-O-H) complex upon isotope substitution. A clear shift of the Laplace DLTS peaks was observed for the C-O-D complex compared to C-O-H, providing direct evidence that the detected deep level originates from a hydrogen-containing defect rather than from intrinsic or oxygen-related centres. This isotope labelling approach, well established in infrared and Raman spectroscopy, is here extended for the first time to electrical characterization techniques. The depth profiles of the defects and the electric field dependence of their emission rates are also analysed.

In addition, we analyse the depth profiles of shallow donors obtained from capacitance-voltage (CV) measurements. A significant increase in shallow donor concentration was observed toward the surface in both H-plasma- and D-plasma-treated samples. The origin of this behaviour is discussed in terms of hydrogen (deuterium) diffusion and interaction with native defects in the near-surface region.

This work establishes Laplace DLTS as a powerful new tool for isotope-selective defect spectroscopy, bridging the gap between optical and electrical characterization methods. The demonstrated capability to distinguish between H- and D-containing complexes will allow the identification of defect constituents in silicon and other technologically relevant semiconductors, where hydrogen-related defects play a critical role in determining carrier concentration and electrical compensation.

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Defect Profiling in AlInGaP Alloys via MOS Impedance Spectroscopy

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Although large-area AlGaInP LEDs exhibit internal quantum efficiencies exceeding 90%, a severe efficiency reduction occurs when the device dimensions are scaled below 100 μm [1]. This “size effect” is attributed to defects generated near the mesa sidewalls during fabrication and passivation [1,2]. The atomic origin and energetic distribution of these defects remain unclear. This work reports on the electrically active defects detected in n-doped $(\text{Al}_x\text{Ga}_{1-x})_{0.5}\text{In}_{0.5}\text{P}$ ($x = 0, 0.5, 0.8, 1$) alloys by applying multi-frequency admittance spectroscopy [3] on AlGaInP/Al₂O₃ MOS capacitors test structures (Fig. 1). All compositions exhibit a common electrical behaviour (Fig. 2). The high-frequency capacitance (i.e., at 1M Hz) saturates below the flat-band capacitance ($C_{\text{FB}} \approx 0.003 \text{ F/m}^2$), indicating a persistent depletion layer caused by a strong surface potential pinning [4]. The frequency dispersion observed at lower frequencies is consistent with Al₂O₃ border traps [5]. However, the density of these traps alone is insufficient to explain the experimentally observed surface-potential pinning. This discrepancy suggests the presence of an additional trap state with very slow dynamics, thus affecting the device electrostatics (i.e., the surface potential pinning) while not contributing appreciably to the AC response. The experimental results were reproduced by physics-based TCAD simulations (Fig. 2). Robust fits, reproducing both the frequency and temperature dependences, required traps with thermal ionization energies (E_{THS}) in the 0.1-0.35 eV range, extending in the first 5 nm of the AlGaInP (Fig. 3). Interestingly, these values correspond to an energy level located approximately 0.35 eV below the vacuum level across all alloy compositions (Fig. 4). Preliminary density functional theory (DFT) calculations indicate that intrinsic vacancies introduce multiple charge transition levels in the GaInP bandgap. Phosphorus vacancy defects introduce a shallow charge transition level (+1/-1) that is compatible with the identified pinning trap level.

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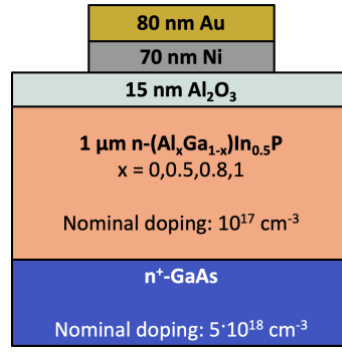


Fig. 1. The MOS test structure used to investigate the defects in AlGaInP alloys.

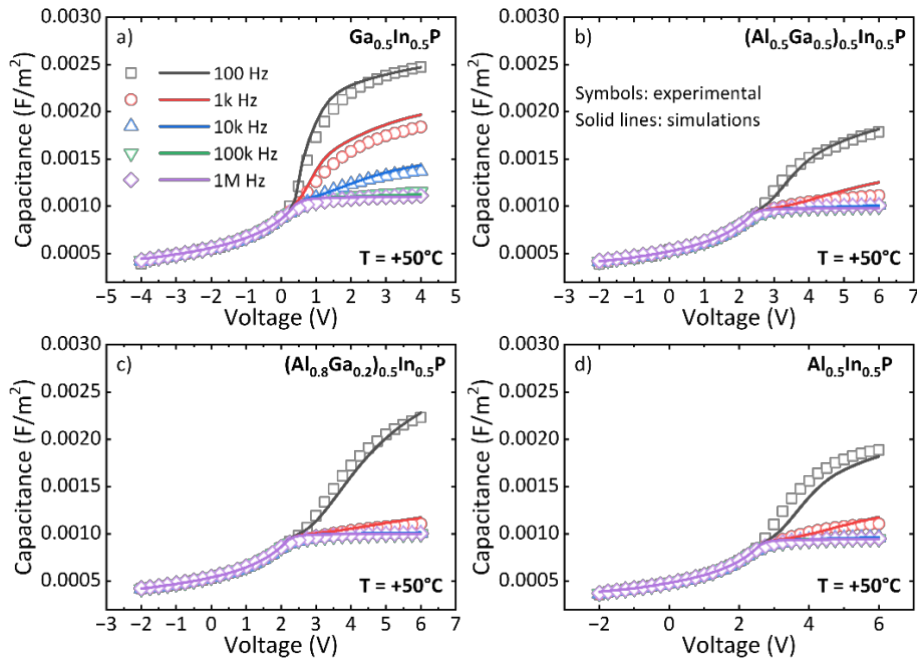


Fig. 2. Experimental (symbols) and simulated (solid lines) CVs of the studied MOS capacitors with different AlGaInP alloys. a) $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$; b) $(\text{Al}_{0.5}\text{Ga}_{0.5})_{0.5}\text{In}_{0.5}\text{P}$; c) $(\text{Al}_{0.8}\text{Ga}_{0.2})_{0.5}\text{In}_{0.5}\text{P}$; d) $\text{Al}_{0.5}\text{In}_{0.5}\text{P}$.

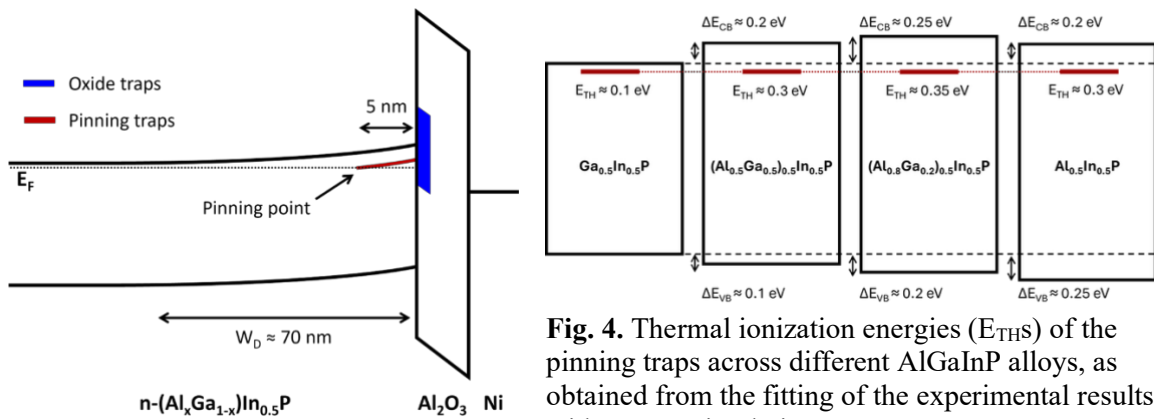


Fig. 3. Trap distributions used for reproducing the experimental results from the AlGaInP MOS capacitors. The band diagram depicts the pinned condition occurring at positive bias.

Fig. 4. Thermal ionization energies (E_{TH}) of the pinning traps across different AlGaInP alloys, as obtained from the fitting of the experimental results with TCAD simulations.

3D chemical mapping of dopant distribution in epitaxially grown heavily doped Si:P and SiGe:B using atom probe tomography

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Epitaxially grown strained Si:P and SiGe:B have become a subject of interest for advanced metal-oxide semiconductor (CMOS) technology. In contrast to the established technique of ion implantation, in-situ doped epitaxy enables more uniform and sharper dopant distribution, and also pushes the boundaries of their solid solubility limits inside Silicon and Silicon-Germanium. Heavily doped Si:P structure formed by epitaxy is expected to have P-rich interstitial clusters, which can dissociate and release additional active carriers into the matrix during annealing [1, 2]. However, in the formation of CMOS devices junctions, the final dopant distribution plays a major role in device's performance and has to be carefully controlled and understood. In this work, we use atom probe tomography (APT), to identify and localize dopants in semiconductors in 3D. APT is the only technique capable of achieving both of those objectives simultaneously [3]. We analyse the composition of tensile-strained Si:P and compressively strained SiGe:B at different concentrations and annealing temperatures. In addition, we also estimate the heterogeneity of the distribution of dopants for heavily doped samples to relate it to their activation. These results are then compared to secondary ion mass-spectrometry (SIMS) profiles as well as electrical conductivity and strain measurements. We provide APT results of Si:P which show the homogeneous distribution of P at $\leq 4.75 \times 10^{21}$ at/cm³, grown in the 600°C-700°C range, which highlights the increase in solid solubility limit of P in Si for epitaxially grown Si:P compared to the implanted one [4]. As for SiGe:B grown at 600-650°C, we localize and quantify the clusters formed for an atomic B concentration of 2.9×10^{20} at/cm³.

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Acknowledgments

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Hydrogen Migration in ALD-Grown Dielectrics for Silicon Surface Passivation

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Metal oxide dielectric thin films grown by atomic layer deposition (ALD) are widely used in microelectronics and photovoltaics. One application is surface passivation which reduces charge carrier recombination that otherwise limits silicon solar cell efficiency, with ALD-grown Al₂O₃ now used in >60% of cells [1]. Understanding mechanisms underpinning this passivation has attracted considerable interest, with particular focus on the role of post-deposition treatments. ALD-grown dielectrics are typically deposited at relatively low temperatures (~200°C), and subsequently annealed to “activate” the passivation [2, 3] with Al₂O₃ and HfO₂ offering excellent passivation. These films contain hydrogen which is incorporated during film growth from the H/OH-terminated substrate and/or growth reactants. It is speculated that hydrogen in ALD-grown metal-oxide layers is involved in activation of surface passivation, although detecting hydrogen is notoriously difficult, with techniques such as SIMS hindered by low detection sensitivity and high background levels.

To study the role hydrogen plays in passivation by ALD-grown Al₂O₃ and HfO₂, we use time-of-flight elastic recoil detection analysis (ToF-ERDA). This technique uses a high-energy (e.g., 14.6 MeV ¹²⁷I⁸⁺ or 12 MeV ⁶³Cu⁶⁺) ion beam at a near-glancing angle on a dielectric-passivated sample, causing atoms to be forward recoiled [4]. Recoiled atoms pass-through two-timing foils before entering a gas ionization chamber where the species is determined. Data on time-of-flight *versus* energy of recoiled atoms (**Fig 1 a, d**) provide depth-dependent elemental profiles, including hydrogen (**Fig 1 b, e**). Importantly, we correlate ToF-ERDA with photoconductance decay lifetime measurements (**Fig 2**) on the same sample set. This enables us to compare hydrogen concentration with surface passivation levels, with the latter separated into field-effect and chemical contributions via the use of corona charging.

ToF-ERDA reveals average hydrogen concentrations of ~1.2 at.%, in both Al₂O₃ and HfO₂ are unchanged from as-deposited to 500 °C, suggesting hydrogen is not responsible for “activating” passivation. As passivation starts to reduce with annealing >550 °C, average hydrogen concentration reduces to ~0.5 and ~0.7 at.% for Al₂O₃ and HfO₂, respectively, with no detectable increase in hydrogen in the silicon. We observe no strong correlation between hydrogen concentration within the film bulk and chemical passivation levels. In both cases, the dielectric film can be considered two regions (near surface and near interface) with differing hydrogen concentrations in each. For Al₂O₃, below the “activation” temperature, hydrogen concentrations are greater near surface than near interface, a trend which is reversed when annealing above the optimal temperature (**Fig 1 c**), whilst at all annealing temperatures hydrogen concentrations are greater near surface for HfO₂ (**Fig 1 f**). For both Al₂O₃ and HfO₂, ToF-ERDA results show that hydrogen out-diffusion from ALD-grown films is a factor to consider in understanding reduced passivation at higher processing temperatures.

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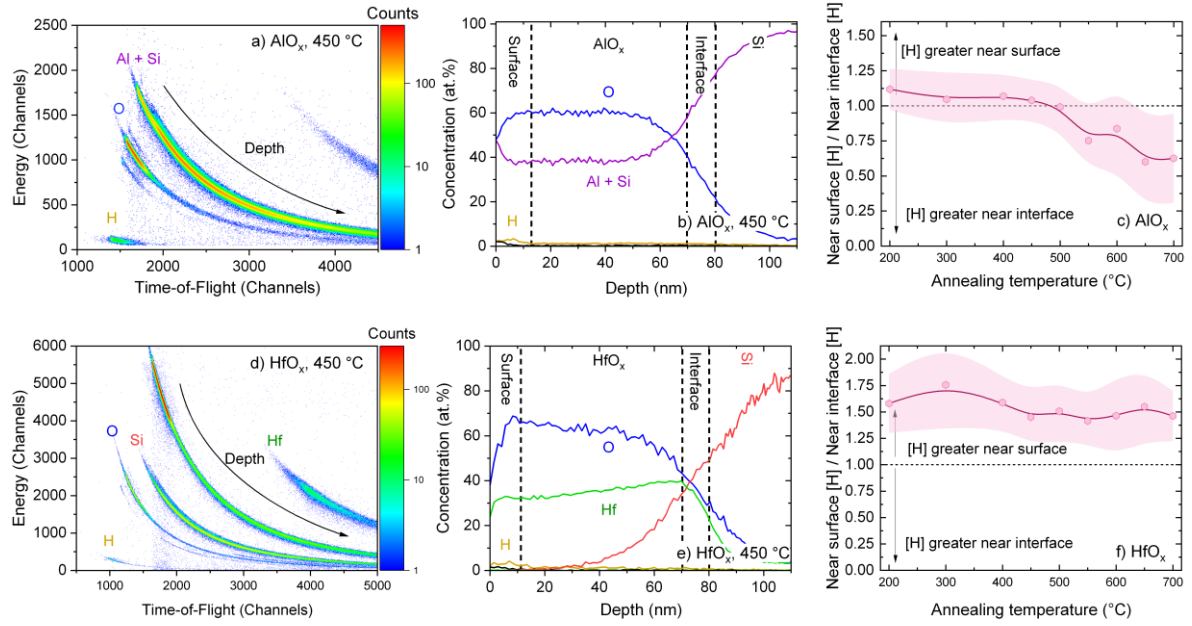


Fig 1: ToF-ERD histograms (a, d), elemental depth profiles (b, e) for 75 nm Al_2O_3 and 75 nm HfO_2 on Si, respectively, annealed at 450°C . (c, f) Relative hydrogen concentrations near-surface and near-interface for Al_2O_3 and HfO_2 on Si, as a function of annealing temperature. Shaded regions in (c, f) correspond to the relative uncertainty.

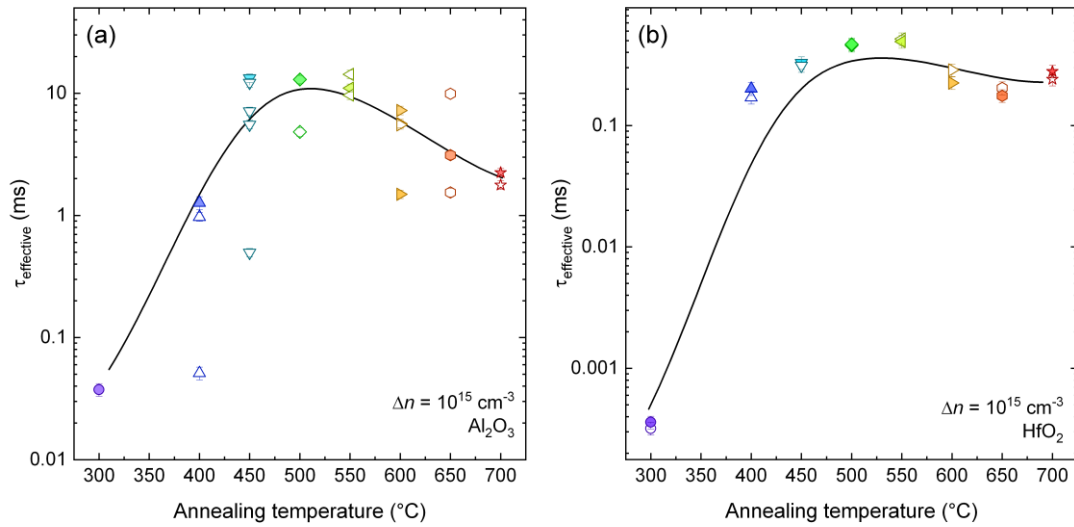


Fig 2: Effective lifetime data (extracted at $\Delta n = 10^{15} \text{ cm}^{-3}$) for $400 \mu\text{m}$ 3-5 Ωcm n-type Si coated with $\sim 70 \text{ nm}$ of (a) Al_2O_3 and (b) HfO_2 , as a function of annealing temperature. For both Al_2O_3 and HfO_2 , annealing at ~ 400 - 500°C is required to “activate” the passivation. Solid data points correspond to samples subsequently measured with ToF-ERDA, and open symbols correspond to additional samples used for lifetime characterisation. The solid line serves as a guide to the eye.

Investigation of Pinholes Opening in Silicon Solar Cell Passivated Contacts Induced by Pulsed Laser Annealing

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Tunnel oxide passivating contacts (TOPCon) represent a leading architecture for high-efficiency crystalline silicon (c-Si) solar cells, featuring a poly-Si/SiO_x/c-Si junction where an ultrathin (< 2 nm) SiO_x tunnelling layer ensures surface passivation and a heavily doped polycrystalline silicon layer provides selective carrier transport. Conventional fabrication relies on high-temperature annealing to recrystallize amorphous silicon, activate dopants, and induce the formation of nanoscale SiO_x pinholes that serve as complementary pathway for vertical charge transport [1]. Maximizing TOPCon efficiency thus requires high electrical activation of dopants within the poly-Si layer while balancing pinhole formation and preserving passivation. However, conventional annealing processes cause strong diffusion and segregation of p-type dopants at the SiO_x interface, degrading passivation and limiting device performance [2], which results particularly critical for the full development of bifacial and interdigitated back contact TOPCon solar cells. A promising solution is pulsed laser melting (PLM) which has been recently demonstrated to be capable of locally recrystallizing silicon, activating dopants beyond solid solubility limits while minimizing dopant segregation [3]. Our early studies on textured surfaces indicate that PLM can selectively affect pyramid tips, forming controlled nanoscale pinholes and, correspondingly, create conductive pathways, as revealed by scanning electron microscopy (SEM) after TMAH pinhole size-enhancement (figure 1a), transmission electron microscopy (TEM) (figure 1b) and atomic force microscope (AFM) morphological and electrical analysis (figure 2). In this work we systematically assess PLM process conditions, in terms of laser energy density and number of pulses, for the development of advanced TOPCon devices. We examine the effects of PLM on dopant activation in poly-Si, the integrity of the SiO_x layer, and the distribution of pinholes on textured surfaces.

Further studies may establish PLM as a replacement for conventional annealing, enabling next-generation TOPCon solar cells with enhanced performance and reduced costs, supporting the advancement of high-efficiency crystalline silicon photovoltaics.

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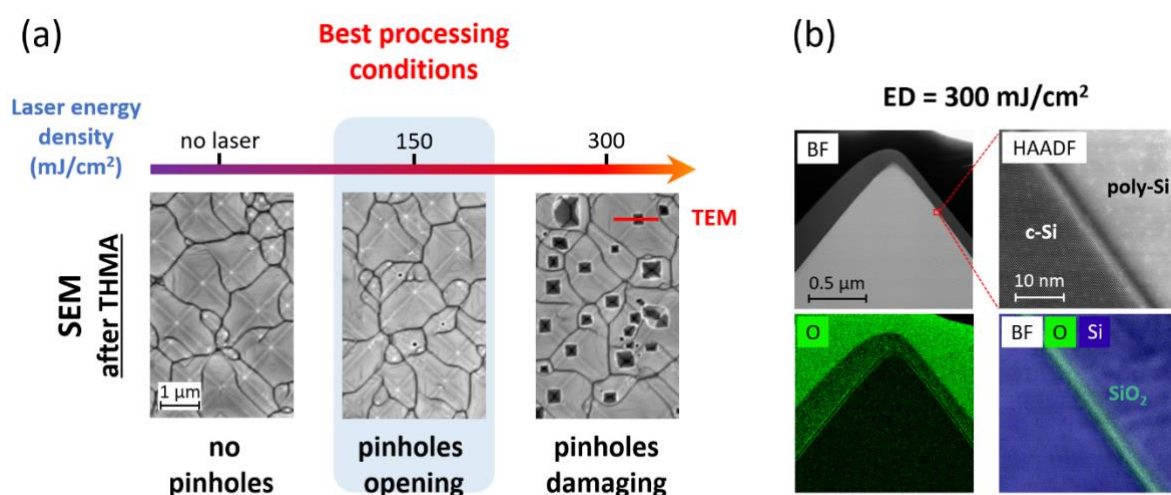


Fig. 1. (a) SEM images after TMAH etching acquired before laser annealing and laser annealed with a single pulse at 150 and 300 mJ/cm². Pinholes through the SiO_x layer appears a black squares. (b) Bright-field transmission electron microscopy (BF-TEM) and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images of a sample laser-processed at ED = 300 mJ/cm², along with EDS composition maps showing oxygen (green) and silicon (blue).

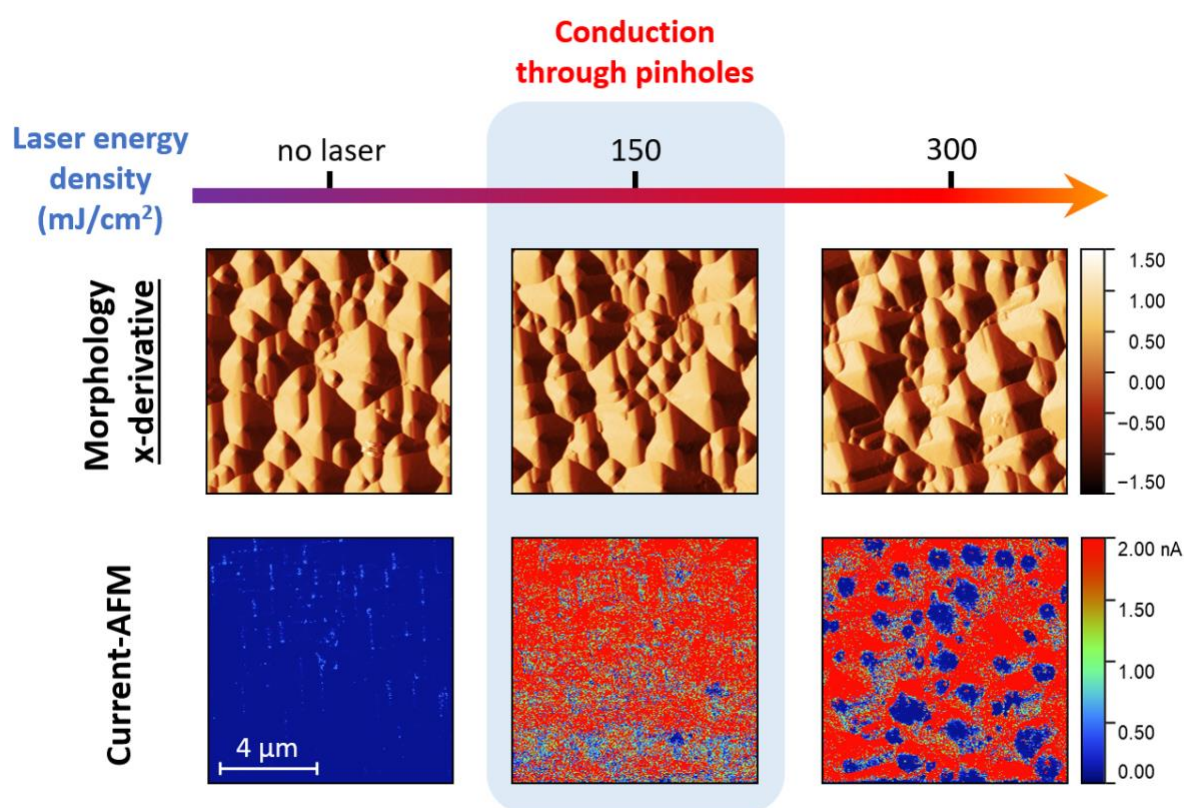


Fig. 2. c-AFM morphology maps (z-axis derivative along the scanning direction) and current maps before laser annealing and laser annealed with a single pulse at 150 and 300 mJ/cm².

Impact of metallic contamination and gettering in bipolar technologies

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Abstract

The electrical performance and reliability of 55nm bipolar devices for analogic and RF applications can be significantly altered by metallic contamination. Devices fabricated on 300mm Czochralski (Cz) p-type Si substrates are very sensitive to defect engineering, impacting the recombination lifetime of carriers and electrical breakdown [1]. This paper tackles defect engineering in a complex integration scheme with a series of ion implantation dopings and activation anneals to fabricate the so-called buried bricks. The redhibitory impact of metallic complexes formed during those process steps is evidenced on p-type Cz substrates using a combination of complementary and innovative techniques. We show that the material properties such as oxygen content tailoring the Bulk Micro Defect (BMD) distribution (favoring gettering if their concentration is right) is not a random-choice. It is notably influenced by interrelated process steps and by patterning [2]. Using interferometry Pattern Wafer Geometry (PWG), a non-controlled precipitation mechanism causing Si plastic deformation, leading to dislocations (Fig. 1), is evidenced. The presence of interstitial defects and dislocations gliding all the way to the edges of the Si wafer is illustrated using complementary cross-sectional Photoluminescence (En-Vision) and Light-Scattering Tomography (LST) techniques (Fig. 2). Transmission Electron Microscopy (TEM) enabled us to confirm afterwards the formation and dissolution of metallic precipitates resulting from diffusion and segregation with dopants [3]. We propose a competing mechanism lying on a precipitate dissolution after successive anneals and etchings, suppressing any efficient substrate oxygen precipitation. To overcome this lack of beneficial BMDs, we have developed at incoming steps a specific anneal treatment to favor internal gettering. These result point out the challenge of defect engineering in p- substrates used in 300mm advanced technologies.

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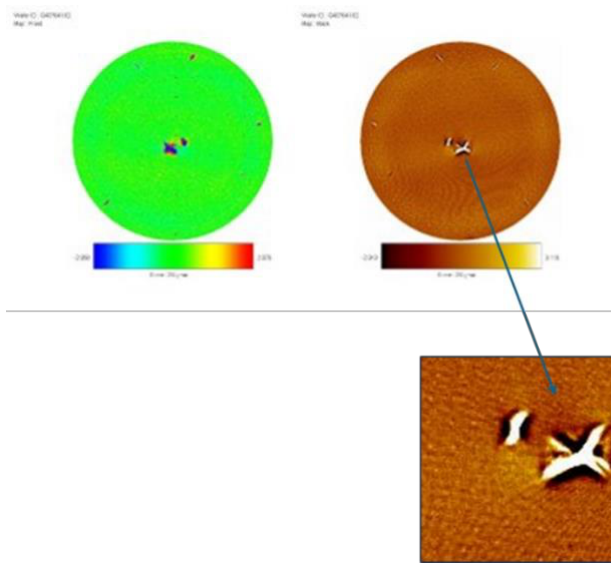


Fig. 1. PWG image of precipitates at the center of a 300mm Cz Si wafer

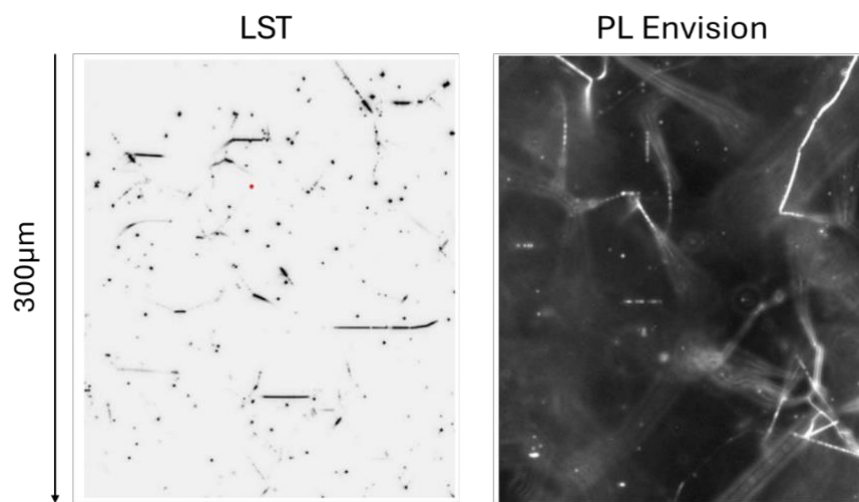


Fig. 2. LST (left) and PL (right) images showing the presence of dislocations at the wafer center.

Atomic structures and stability of large-sized vacancy clusters and finite-size extended interstitial defects in silicon: A neural-network potential and first-principles study

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Large-diameter Si wafers used for semiconductor applications are typically manufactured from Si single crystals grown by the Czochralski (CZ) method. In growing CZ-Si crystals, intrinsic vacancies (V) and interstitials (I) are inevitably introduced from the melt/solid interface at thermal equilibrium concentrations of $\approx 10^{14}$ /cm³ [1]. After pair recombination of V and I , excess V or I agglomerate to form secondary defects such as V -clusters (void defects) and I -clusters [2]. Self-interstitials are also created during ion implantation, subsequently forming I -clusters and extended interstitial defects (EIDs). Both void defects and EIDs are known to cause harmful effects on device performance. Thus the fundamental knowledge about their formation mechanism at the micro-, meso- and macroscales is essential to fabricate high-quality Si as well as to deepen our understanding of defect physics. For this purpose, an artificial neural-network (ANN) interatomic potential [3] trained with data from density-functional-theory (DFT) calculations is developed to reveal formation energies (E_f) and relaxed structures of large-sized V - and I -clusters in Si by varying the number n of I or V up to around 10^3 [4,5]. The ANN potential is demonstrated to outperform empirical potentials in prediction of E_f and defect structures.

For V -clusters [4], E_f and relaxed structures for four typical modes are examined: the fourfold coordinated configuration (FC), hexagonal ring cluster (HRC), spherically shaped cluster (SPC), and [111]-oriented stacking fault (SF). The present ANN potential reasonably predicts E_f values and relaxed structures obtained from DFT calculations for all modes examined. It also predicts that the order of E_f is $\text{HRC} < \text{SPC} \leq \text{SF}$ for $6 < n \lesssim 30$, $\text{HRC} \approx \text{SPC} < \text{SF}$ for $30 \lesssim n \lesssim 300$, and $\text{SPC} \leq \text{HRC} < \text{SF}$ for $300 \lesssim n$, with the prediction of reasonable relaxed structures in all the ranges of n . This indicates that the favorable agglomeration mechanism becomes the SPC mode as V -clusters involve large numbers of vacancies.

For I -clusters [5], E_f of various EIDs in Si is examined. For $n \leq 36$, the compact cluster or (311)-rodlike defect is found to be most stable, depending on n . This trend strongly depends on simulation cell sizes, suggesting the importance of sufficiently large cells. For $36 < n \lesssim 860$, the (311)-rodlike defect is most stable whereas the Frank-loop defect (FLD) becomes most stable for larger n .

By comparing E_f of V -cluster and I -cluster with the same number of V and I , E_f (SPC) is about 190 eV less than E_f (FLD) at $n = 1,000$. This indicates that the V -clusters are more stable than the I -clusters, and corresponds to the fact that V -cluster formation occurs at a higher temperature (at around 1100°C) than I -cluster formation (at around 900°C) during CZ-Si crystal growth if ignoring the difference in their entropy terms.

The results of ANN-MD conducted to investigate the stability of V -clusters and EIDs at high temperatures will be presented at the conference.

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Diffusion and gettering mechanism of critical metals in 300mm silicon substrates

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CMOS image sensors require tight control of metallic contamination to ensure low dark current and avoid white-pixel defects [1]. Among the most critical contaminating species, iron (Fe) is a fast diffuser in silicon and is common in the semiconductor fabrication lines, while tungsten (W) is a slow diffuser, but can strongly impact pixel reliability [2]. This work studies the behavior, diffusion, and gettering mechanisms of Fe and W. It also points out the appropriate combination of innovative techniques to illustrate the efficiency of layer stacks (Fig. 1) that are deposited here in gettering, segregating metals or limiting their diffusion.

A protocol has been developed for studying metallic contamination on 300 mm wafers [3]. Intentional contamination with Fe or W is introduced by spin coating on Si substrates with various layer stacks, followed by O₂ annealing to promote diffusion through the stacks. The investigated layers can act as gettering layers, diffusion barriers, or preferential sites for metals [4]. By comparing the impact of presence of Fe and W under the same thermal budgets and structures, we highlight the contrasting behaviors of these contaminants.

For this analysis, new and complementary characterizations are combined. This gives access to both surface and bulk contamination. Scanning Electron Microscopy (SEM) together with X-ray Photoelectron Spectroscopy (XPS) and other optical techniques enable to identify W precipitation with oxygen at the wafer surface (Fig. 2). On the other hand, Surface Photovoltage (SPV) is used to extract the Fe concentration in the bulk, as illustrated also by macro-photoluminescence (macro-PL) for detection of non-radiative recombination areas [5] (Fig. 3). This set of techniques provides relevant details on the slightly different mechanisms specific to these metals (precipitation vs. oxidation-diffusion). It also emphasizes the specific layer stacks that are promising for gettering in advanced semiconductor process flows.

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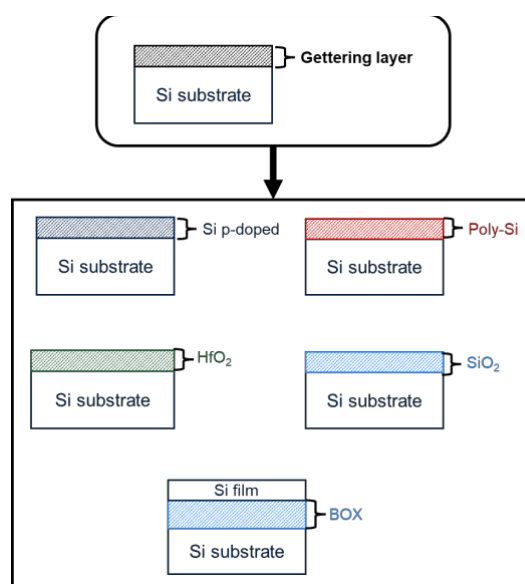


Fig. 1. Schematic of the different layer stacks used as potential gettering layers on Si substrates

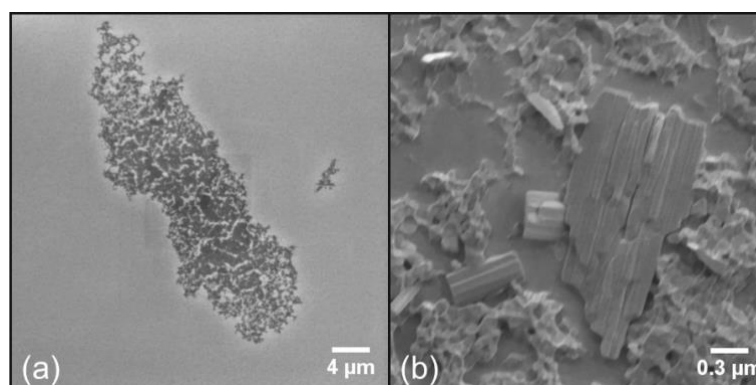


Fig. 2. SEM images of W–O precipitates formed in a 13 nm HfO₂ layer on p-type Si intentionally contaminated with W: (a) overview of a large W–O precipitate cluster; (b) magnified view of the precipitate morphology

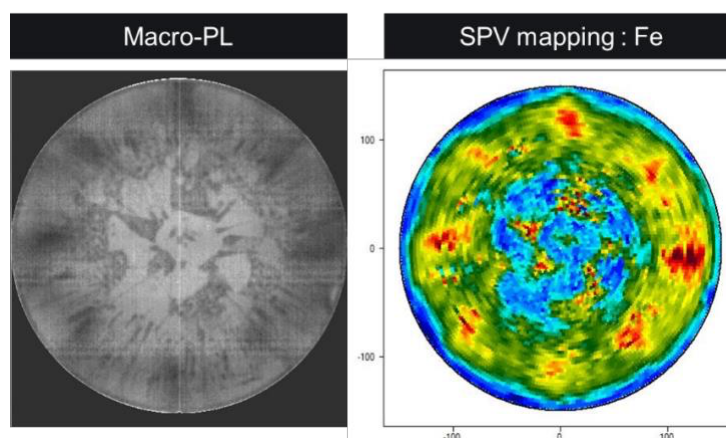


Fig. 3. Correlation between Macro-PL and SPV Fe mapping on a 90 nm p⁻ Si epitaxial layer on p⁻ Si substrate after intentional Fe contamination

TEM analysis of Textured Silicon Polymorph Crystals obtained via Nanoindentation and Annealing

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Silicon polymorphs exhibit unique properties, such as the combination of low thermal conductivity with high thermoelectric efficiency, or high carrier mobility with superconductivity. Some polymorphs are also predicted to possess a direct bandgap. Among these, hexagonal (hd) silicon is particularly attractive due to its potential use as a template for the epitaxial growth of hexagonal SiGe alloys, that can maintain a tunable direct bandgap across a broad compositional range, offering significant flexibility for optoelectronic applications.

Recently, we demonstrated the formation of micrometer-sized, textured hd-Si crystals through nanoindentation followed by rapid annealing [1]. This approach offers a simpler alternative to more complex syntheses, such as those involving nanowires or sophisticated deposition systems. Under mechanical high pressures, diamond cubic silicon (dc-Si) transforms into a metallic β -Sn phase. Upon pressure release, by optimizing nanoindentation unloading, we observed—via Raman spectroscopy—the formation of a mixed body-centered cubic (bc8) and rhombohedral (r8) phase.

In this study, we investigate nanoindented dc-Si (001) pits prior to annealing, gaining deeper crystallographic insights into the intermediate metastable Si phases. The system was analyzed using polarized Raman spectroscopy and transmission electron microscopy (TEM). TEM micrographs revealed extensive regions of r8/bc8 phases, well-aligned with the substrate. As an alternative to rapid annealing for producing hd-Si, we also explored the effects of slow annealing, leading to the formation of other polymorphs, potentially attributable to Si-XIII, a phase with an as-yet unidentified crystal structure.

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Speaker Index

- Abbadie, Alexandra 69 Mo-P21, 206 Fr-O3
Albrecht, Amy 148 Tu-P20
Alvi, Kaynat 35 Mo-O14, 47 Mo-P7
Amoroso, Pejk 103 Tu-O7
Arena, Valentina 143 Tu-P17
Belaid, Walid 106 Tu-O9, 158 Tu-P27
Berencén, Yonder 12 Mo-I2
Besana, Andrea 31 Mo-O12
Beyer, Franziska C. 169 We-I2
Binetti, Simona 164 Tu-P31
Black, Lachlan 3 Su-I2
Bläß, Ulrich 150 Tu-P21
Bougeard, Dominique 97 Tu-I2
Bracht, Hartmut 151 Tu-P22, 177 Th-I2
Buca, Dan 105 Tu-O8
Calogero, Gaetano 138 Tu-P14, 179 Th-O5
Capellini, Giovanni 117 Tu-O15
Cardoso Paz, Bruna 20 Mo-I3
Chang, Guo-En 14 Mo-O5
Chang, Yu-Chen 27 Mo-O11
Chiodi, Francesca 4 Mo-I1
Chretien, Jeremie 133 Tu-P11
Ciavatti, Andrea 172 Th-O1
Coffa, Salvatore 91 Tu-I1
D'Arrigo, Giuseppe 183 Th-O7
de Cerdeira Oliveira, Afonso 7 Mo-O2
Del Conte, Corrado 127 Tu-P8
Demeneghi, Daniele 193 Th-O11
Deretzis, Ioannis 118 Tu-P1
Di Russo, Enrico 5 Mo-O1, 101 Tu-O6,
122 Tu-P3, 162 Tu-P30
Di Sabatino, Marisa 84 Mo-P30, 147 Tu-P19
Dryhailo, Maryna 201 Th-O15
Du, Wei 110 Tu-I4
Durrani, Zahid 185 Th-I3
El Kurdi, Moustapha 109 Tu-O11
Farina, Roberta 53 Mo-P12
Fevrier, Oceane 210 Fr-O5
Finazzi, Lorenzo 115 Tu-O14
Fiscaro, Giuseppe 174 Th-O2
Goulain, Paul 113 Tu-O13
Grant, Nicholas 196 Th-O12
Hazdra, Pavel 129 Tu-P9
Herms, Martin 152 Tu-P23
Hiller, Daniel 181 Th-O6
Hsu, Kuei-Shen 154 Tu-P25
Impelluso, Davide 13 Mo-O4
Kerdiles, Sebastien 71 Mo-P22
Kolkovsky, Vladimir 124 Tu-P5, 125 Tu-P6,
198 Th-O13
Kot, Dawid 57 Mo-P15
Kras'ko, Mykola 73 Mo-P23
Kusunoki, Takuya 39 Mo-P2
La Torraca, Paolo 199 Th-O14
Lauer, Kevin 78 Mo-P26
Leiviskä, Oskari 45 Mo-P6
Lyasota, Alexey 94 Tu-O2, 95 Tu-O3
Markevich, Vladimir 81 Mo-P28
Masoud, Mahsa 137 Tu-P13
Mica, Isabella 194 Th-I4
Migliore, Giorgio 92 Tu-O1
Mio, Antonio Massimiliano 212 Fr-O6
Moutanabbir, Oussama 104 Tu-I3
Mtchedlidze (Mchedlidze), Teimuraz
189 Th-O9
Müller, Matthias 63 Mo-P18
Murphy, John 25 Mo-O10, 87 Mo-P32
Murphy-Armando, Felipe 29 Mo-I4
Nazzari, Daniele 23 Mo-O9
Oehme, Michael 108 Tu-O10
Olikh, Oleg 37 Mo-P1, 135 Tu-P12
Oliver, Rachel 165 We-I1
Ozawa, Koji 89 Mo-P33
Pain, Sophie 85 Mo-P31, 202 Fr-O1
Pannocchia, Matteo 54 Mo-P13
Patelli, Anita 161 Tu-P29
Pavlov, Sergey 67 Mo-P20
Pezzagna, Sébastien 166 We-O1
Pothorszky, Szilard 145 Tu-P18
Puddu, Alessandro 50 Mo-P9
Puggioni, Gianmarco 204 Fr-O2
Pulici, Andrea 33 Mo-O13
Rebohle, Lars 100 Tu-O5
Reboud, Vincent 141 Tu-P16
Ricciarelli, Damiano 191 Th-O10
Saini, Nishant 159 Tu-P28
Scandolara, Benedetta 98 Tu-O4
Scheblykin, Ivan 171 Th-I1
Schiller, Leon 167 We-O2
Schofield, Steven 1 Su-PL1
Schouten, Mette 59 Mo-P16
Seguini, Gabriele 153 Tu-P24, 187 Th-O8
Sgarbossa, Francesco 10 Mo-O3, 80 Mo-P27,
140 Tu-P15
Sinz, Lena-Maria 178 Th-O4
Spataro, Giulia Maria 16 Mo-O6
Stipkovich, Maximilian 21 Mo-O8
Sueoka, Koji 82 Mo-P29, 208 Fr-O4
Sutinen, Kaisla 131 Tu-P10
Takeda, Iori 42 Mo-P4
Terletskaia, Mariia 18 Mo-O7
Tetzner, Henriette 48 Mo-P8

Tomkovic, Jiri 156 Tu-P26
Trifiletti, Vanira 126 Tu-P7, 176 Th-O3
Tröger-Neuhaus 151 Tu-P22
Vacante, Ignazio 56 Mo-P14
Wang, Jinge 65 Mo-P19
Wang, Yilun 51 Mo-P10
Weiss, Charlotte 61 Mo-P17
Wen, Shuyu 75 Mo-P24
Willoquet, Théophile 111 Tu-O12
Wouters, Lennaert 2 Su-I1
Xu, Yanan 76 Mo-P25
Yang, Deren 120 Tu-P2
Yuan, Shuai 41 Mo-P3
Zhou, Shengqiang 44 Mo-P5



		Sunday	Monday	Tuesday	Wednesday	Thursday	Friday		
		27 September, 2026	28 September, 2026	29 September, 2026	30 September, 2026	1 October, 2026	2 October, 2026		
Start	End							Start	End
8:30	10:10		Group IV: Hyperdoping and Defects <i>Auditorium</i> Chiodi (invited), Di Russo, de Cerdeira Oliveira, Sgarbossa	Silicon Carbide <i>Auditorium</i> Coffa (invited), Migliore, Lyasota, Castelletto	Nitride Semiconductors <i>Auditorium</i> Oliver (invited), Pezzagna, Schiller, Beyer (invited)	Perovskites and their Applications <i>Auditorium</i> Scheblykin (invited), Ciavatti, Fiscaro, Trifiletti	Silicon for Photovoltaics and Microelectronics <i>Auditorium</i> Pain, Puggioni, Abbadie, Sueoka, Fevrier, Mio	8:30	10:10
10:10	10:30		Coffee break	Coffee break		Coffee break		10:10	10:30
10:30	10:40		<i>Grecale</i>	<i>Grecale</i>		<i>Grecale</i>	Coffee break	10:30	10:40
10:40	10:50						<i>Grecale</i>	10:40	10:50
10:50	11:00							10:50	11:00
11:00	12:00		Group IV for Photonics <i>Auditorium</i> Berencén (invited), Impelluso, Chang, Spataro, Terletskaia	Silicon, Germanium and their Alloys I <i>Auditorium</i> Bougeard (invited), Scandolara, Rebohle, Di Russo, Amoroso	Social excursion Cultural tour of the Venetian Lagoon	Silicon, Germanium and their Alloys II <i>Auditorium</i> Bracht (invited), Sinz, Calogero, Hiller, D'Arrigo	Awards & closing <i>Auditorium</i> Announcements, YRA and YSA awards, Closing remarks	11:00	12:00
12:00	12:40							12:00	12:40
12:40	13:40		Lunch break	Lunch break		Lunch break	Lunch & departure	12:40	13:40
13:40	14:00		<i>Grecale</i>	<i>Grecale</i>		<i>Grecale</i>		13:40	14:00
14:00	15:00	Registration and Welcome Coffee <i>Grecale</i>	Alternative Semiconductor Devices <i>Auditorium</i> Cardoso Paz (invited), Stipkovich, Nazzari, Murphy, Chang	GeSn Special Session (LASTSTEP) I <i>Auditorium</i> Moutanabbir (invited), Buca, Belaid, Oehme, El Kurdi		Low Dimensional Semiconductors <i>Auditorium</i> Durrani (invited), Seguini, Mtchedlidze, Ricciarelli, Demeneghi		14:00	15:00
15:00	15:40							15:00	15:40
15:40	15:45		Coffee break	Coffee break		Coffee break		15:40	15:45
15:45	16:10	Opening <i>Auditorium</i> Welcome speech	<i>Grecale</i>	<i>Grecale</i>		<i>Grecale</i>		15:45	16:10
16:10	16:15							16:10	16:15
16:15	17:00	Plenary Session <i>Auditorium</i> Schofield (plenary)	Defects for Advanced Semiconductor Applications <i>Auditorium</i> Murphy-Armando (invited), Besana, Pulici, Alvi	GeSn Special Session (LASTSTEP) II <i>Auditorium</i> Du (invited), Willoquet, Goulain, Finazzi, Capellini		Advanced Characterization Techniques <i>Auditorium</i> Mica (invited), Grant, Kolkovsky, La Torraca, Dryhailo		16:15	17:00
17:00	17:50	Defect Engineering and Metrology <i>Auditorium</i>	Industrial session <i>Auditorium</i>					17:00	17:50
17:50	18:00							17:50	18:00
18:00	18:10	Wouters (invited), Black (invited)						18:00	18:10
18:10	18:20							18:10	18:20
18:20	19:00							18:20	19:00
19:00	22:00	Dinner	Poster Session 1 <i>Grecale Hall E</i> 32 posters	Poster Session 2 <i>Grecale Hall E</i> 30 posters	Conference dinner	Dinner		19:00	22:00
		<i>Grecale</i>			<i>Grecale</i>	<i>Grecale</i>			