



LHCb Upgrade of the Tracking and RICH detector

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Group: LHCb



LHCb Upgrade I



The detector challenge high luminosity running of LHC





The detector challenge for upgrade II



Targeting same performance as in Run 3, but with pile-up ~40!

VErtex LOcator (VELO)



Pile-up suppression

Each hit in VELO timestamped with 50 ps resolution \rightarrow 20 ps per track

track density with ~40 interactions $\begin{bmatrix} 5 \\ 0 \\ -5 \\ -5 \\ -5 \\ -5 \\ 0 \end{bmatrix}$ Aligned



20 ps time window applied





Italian lead project to develop of a <u>complete tracking demonstrator</u> capable of copying with extremely <u>high instantaneous luminosities</u> foreseen at HL-LHC (High Luminosity LHC)

Pixel Sensor



Pixel Array



TimeSPOT sensors:

3D Silicon sensors with high space resolution, wolrd's best time resolution, and great radiation hardness

Possible activities in Padova:

Test of complete tracking demonstrator of an array of planes of pixels with particle beam at CERN

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LHCb Particle Identification: RICH





10⁴

0.015

20

10⁵

Momentum (MeV/c)

LHCb Upgrade II - PID

Introduction: upgrade schedule



RICH Upgrade: LS3 enhancements

- During the next shutdown the detector will be equipped with new electronics capable of measuring the time of arrival of photons with 100 ps accuracy
- The Padova group is involved in the characterization of the prototypes of electronics + detectors with a beam of protons at CERN





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LHCb Upgrade II - PID

2.5D and 3D Integration Next-generation development: Backside Illuminated SiPMs

The next-generation of developments, currently being investigated at FBK, is building a *backside-illuminated*. NUV-sensitive SiPM. Several technological challenges should be overcome.

Sensor laver (Custom)

Clear separation between charge collection and multiplication regions.

Potential Advantages: Front Side Readout laver (CMO Up to 100% FF even with small cell pitch $10 - 20 \, \text{um}$ Avalanche Region Ultimate Interconnection density: < 15 um High speed and dynamic range Gurad ring Low gain and external crosstalk Photo-Development Risks: generated **Collection Region** (Uniform) entrance window on the electrons Charge collection time jitter backside, ideal for enhanced optical stack (VUV sensitivity, nanophotonics) Low Gain → SPTR? Trench **Back Side** Local electronics: ultra fast and possibly Effectiveness of the new low-power. entrance window **Light Entrance** New BSI-SiPM structure

Radiation hardness:

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- The SiPM area sensitive to radiation damage, is much smaller than the light sensitive area
- Assumption: the main source of DCR is field-enhanced generation (or tunneling).

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Radiation hardness of the new electronics

- The readout electronics will be subject to radiation damage from neutrons and ionizing particles.
- Radiation resistance will be tested with neutrons sources from a reactor and with protons
- Possible activities:
 - Simulation of radiation damage
 - Development of readout and control board







CMOS 65 nm layers - metallization and passivation layers are on top of Poly-Si gates and critic Silicon dioxide layers (taken from Chin. Phys. B Vol. 26, No. 8 (2017) 088501), modeled with staked layers.



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